An Evaluation of 2-phase Charge Pump Topologies with Charge Transfer Switches for Green Mobile Technology

Yan Chiew Wong[1,2], Nurul H. Noordin[1,2], Ahmed O. El-Rayis[1,2], Nakul Haridas[1,2], Ahmet T. Erdogan[1], Tughrul Arslan[1,2]
[1]Institute of Integrated Micro and Nano Systems, School of Engineering, The University of Edinburgh, EH9 3JL, UK
[2]Advanced Smart Antenna Technologies Research Group, School of Engineering, The University of Edinburgh, EH9 3JL, UK
{Y.Wong, N.Noordin, A.El-Rayis, N.Haridas, A.Erdogan, T.Arslan}@ed.ac.uk

***Abstract*- The development of charge pumps has been motivated by the power supply requirements of portable electronic devices. Charge pumps are inductorless DC-DC converters that are small size and high integration. The quality of the charge pump greatly depends on the effectiveness of switches to turn on and off at the designated clock phases. However, to date, no analysis has been carried out on the overall performance of charge pumps based on switch components in practice. This work demonstrates the characteristics of transistors as charge transfer switches and their effects on the performance of a charge pump. Three most common charge pump topologies are evaluated in terms of voltage drop due to on-resistance and charge loss per switch. Simulations are performed in 0.35 μm Austriamicrosystems (AMS) technology for Dickson, Voltage Doubler and Makowski charge pump topologies in steady and dynamic states. In addition, the effect of switch parameters for different charge pump topologies are compared and analysed. We demonstrate that the Makowski charge pump is the topology for future green mobile technology.**

Keywords –Charge Transfer Switch; Charge pumps; DC-DC Converter; Green Mobile Technology

I. INTRODUCTION

A charge pump is an inductorless DC-DC converter that uses only capacitors and switches without involving amplifiers or transformers to step up or step down the voltage. This approach has the advantages of a simple control method, reduced physical volume, less electromagnetic interference (EMI), low cost and high power density for its design. A charge pump is a device of choice in a portable appliance where the normal range of operating voltages is limited and it provides the ability for System-on-Chip (SoC) integration with various other devices and components when the application dictates. Among various types of charge pumps, the 2-phase charge pump appears as one of the most promising topology due to its simpler switching circuitry when used in mobile technology. Extensive studies of charge pumps have been performed but most of these treat switches as ideal components [1-3]. Understanding the behavior of switches in the respective charge pump topologies is crucial in order to have a greener technology implementation. However, very few papers have discussed the effect of switches and those discussions referred to only one charge pump topology [4-7]. Up till now, no comparison amongst Dickson, Voltage Doubler and Makowski charge pumps has been made from the point of view of the switches. This paper presents a comprehensive study on the behavior and selection of switches, as well as evaluating transistor parameters in a steady and dynamic state for various charge pump topologies.

In section II, the characteristics of switches used in various charge pumps are presented. The challenges of the implementation of *n* channel (nMOS) and *p* channel transistors (pMOS) in charge pumps are discussed in section III. The parameters of transistors are evaluated in steady and dynamic state in section IV. The evaluated equations are validated with the simulation results.

II. SWITCHES USED IN VARIOUS TOPOLOGIES OF 2 PHASE-CHARGE PUMPS

Most topologies of charge pumps are based on three types: The Dickson, cross-connected Voltage Doubler and Makowski. Dickson charge pump is one of the DC-DC converters used in mixed mode circuits to generate the required high voltages through cascade connection of a suitable number of identical stages (*N*) to give an output voltage equal to $(N+1)*V_{DD}$ [8]. High voltage transistors are used in the Dickson charge pump to prevent excessive gate oxide stress [5, 9]. High voltage transistors lead to a large gate area and parasitic capacitance with their high threshold voltage (V_{TH}) compared to low voltage devices.

The cross-connected Voltage Doubler is another type of charge pump which is considered to give higher efficiency when compared to Dickson charge pump [5, 8, 10]. The topology of the Voltage Doubler consists of a pair of cross-connected nMOS and pMOS switches, for charging the storage capacitors and transferring the charges between stages. The topology of the Voltage Doubler allows the use of low voltage transistors and small capacitances in fast switching frequency [9]. However, the gain of the Dickson and the Voltage Doubler is only suitable for low to medium value. If the multiplication factor is more than 10 times of the input voltages, quite a large area of silicon will be required.

Makowski introduced an *N*-stage charge pump with its final voltage gain limited by $(2N+1)^{th}$ Fibonacci number ($F_{(N+1)}$) [2, 3, 6, 11]. This gain is the maximum conversion ratio that can be attained from a 2-phase switch capacitor charge pump by using *N-1* capacitors. However, a high voltage of clock amplitude (V_{CLK}) i.e. *0V* to $F_{(N+1)}*V_{in}$ is used to maintain the voltage gain multiplication per stage. Thus, high voltage transistors must be used in this topology to avoid transistor gate oxide break down.

III. Types of Switches

The first charge pump was designed using diodes as charge transfer switches which had a low voltage gain per stage resulted from the high voltage drop across diode V_D [12-14]. In later stages, MOSFETs which have a better switching feature are used to replace diodes as charge transfer switches in the charge pumps.

In designing the charge pump, MOSFET*s* have to operate in the linear region to transfer a high current with a small on-resistance [6, 15]. An energy efficiency charge pump is determined by the effectiveness of MOSFET*s* in turned on and off at the designated clock phases. However, both nMOS and pMOS have difficulties in switching on and off. nMOS can be easily switched off by applying a gate voltage of 0V or an effective gate to source voltage (V_{GS_eff}) smaller than the V_{TH} [15, 16]. However, to switch on the *nMOS* without suffering from significant voltage drop, the V_{GS_eff} of the nMOS has to be higher than V_{DD} after deducting the V_{TH} [12, 15]. The V_{TH} increases when the bulk's potential, $V_{B,}$ is applied [16]. The performance of nMOS as a charge transfer switch also deteriorates with body effect. In the design of low conversion ratio charge pump, the bulk of the nMOS is grounded. However, with the scaled down gate voltage, a higher conversion ratio is required. The transistor may break down when the potential between the drain or the source or the gate terminal ($V_{D/S/G}$) and V_B is greater than the technology specific voltage. Thus, in the design of higher conversion ratio charge pump, the bulk of the nMOS transistor is connected to the lower terminal between the drain and the source [10]. The voltages of the source and the drain terminal will increase with the increased stages of charge pump. Thus, a higher V_{TH} will be generated at the higher stages. This will lead to body effect [16, 17]. In this condition, the transconductance (g_s) between the source and the bulk as shown in (1) can no longer be ignored. For MOSIS technology 0.8 μm, while the source to bulk voltage (V_{SB}) reaches above 15V with V_{TH0} of 0.08V, the actual V_{TH} exceeds 2.5V [13]. This body effect seriously diminishes the output voltage of the charge pump. As the stage of charge pump increases, the overall V_{TH} increases as well and this decreases the voltage gain per stage. To reduce the V_{TH} dependence on the stages, boosted pump clock schemes were introduced [5, 17].

$$V_{TH} = V_{TH0} - \gamma\sqrt{|2\phi_F|} + \frac{\gamma^2 \mu_{n/p} C_{OXn/p} W_{n/pi} V_{GS\_eff}}{2 g_{si} L_{n/p}} \quad (1)$$

where $V_{TH0n/p}$ is the threshold voltage with zero V_{SB} of nMOS or pMOS, g_s is the transconductance between the source and the bulk, $V_{GS\_eff}=V_{GS\_CLK}-\alpha N V_{TH0n/p}$, V_{GS_CLK} is the amplitude of the switching clock, α is the coefficient proportional to the number of stages of the charge pump with the values between $0<\alpha<1$ and *N* is the number of stages of charge pump

For the charge pump using pMOS switches, this type of transistor can easily be switched on by $V_{GS\_eff} = 0V$. However, they have problems with completely switching off the pMOS switches. To avoid leakage current from the drain or the source to substrate, the bulk of pMOS should be connected to the highest terminal. Normally, it will be tied at the highest potential either the source or the drain. However, while pMOS in charge pump topology, the potentials of the drain and the source of pMOS are not always maintain at the highest. Thus, pMOS switches suffer from determining the highest potential terminal. Auxiliary transistors were used to ensure the bulk of pMOS is always connected to the highest potential between the drain and the source [12, 15, 17, 18].

IV. Analysis of Steady State Switches in Charge Pumps

At steady state, the switches are operating in the linear region. To determine the general on-resistance [16] per switch in charge pumps, V_{GS_eff} plays a significant role as shown in (2). The V_{GS_eff} can be calculated based on the amplitude of switching clock (V_{CLK}) minus the multiply of coefficient (α) and threshold voltage with zero V_{SB} (V_{TH0}). The α is proportional to the number of stages of the charge pump with the values at between 0 and 1.

$$r_{ds} = 1/g_{ds} = \partial I_D / \partial V_{DS} = 2L/[\lambda \mu_n C_{OX} W (V_{GS\_eff})^2] \quad (2)$$

where r_{ds} is the on-resistance in the transistor, g_s is the transconductance, ∂I_D and ∂V_{DS} are differential of drain current and the drain to source voltage, *L* and *W* is the length and the width of the transistor, V_{GS_eff} is the effective gate to source voltage, C_{OX} is the gate oxide of the transistor, λ is the output impedance constant and μ_n is the mobility of electrons.

The V_{GS_eff} limits the number of stages in the charge pump. The amplitude of the switching clock (V_{CLK}) depends on charge pump topologies. For the Dickson and the cross-connected charge pumps, V_{CLK} varies from 0V to V_{DD}. While for the Makowski charge pump, the V_{CLK} swings between 0V to $F_{(N+1)}*V_{DD}$ [4, 6]. The average on-resistance for a Dickson

charge pump with *N+1* nMOS-type switches is shown in (3). While for the Voltage Doubler and Makowski charge pumps, their average on-resistances can be determined from (4) and (5) respectively. *N* numbers of nMOS and *2N+1* pMOS transistors are used in Makowski charge pump. The topology of Voltage Doubler charge pump requires the highest switches with *2N* of nMOS and *2N* of pMOS transistors.

$$R_{avg} = [\sum_{i=1}^{N+1} \frac{2L_{ni}}{\lambda_n \mu_n C_{oxn} W_{ni} (V_{GS\_effni})^2}] \Big/ N+1 \quad (3)$$

$$R_{avg} = \frac{\sum_{i=1}^{2N} \frac{2L_{ni}}{\lambda_n \mu_n C_{oxn} W_{ni} (V_{GS\_effni})^2}}{2N} + \frac{\sum_{i=1}^{2N} \frac{2L_{pi}}{\lambda_n \mu_p C_{oxp} W_{pi} (V_{GS\_effpi})^2}}{2N} \quad (4)$$

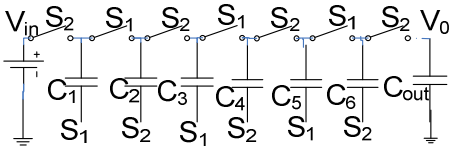
$$R_{avg} = \frac{\sum_{i=1}^{N} \frac{2L_{ni}}{\lambda_n \mu_n C_{oxn} W_{ni} (V_{GS\_effni})^2}}{N} + \frac{\sum_{i=1}^{2N+1} \frac{2L_{pi}}{\lambda_n \mu_p C_{oxp} W_p (V_{GS\_effpi})^2}}{2N+1} \quad (5)$$

where R_{avg} is the average on-resistance, V_{GS_effni} and V_{GS_effpi} are the effective gate to source voltages applied to i_{th} of nMOS and pMOS respectively in the *N* number of stages of charge pump, λ_n is the output impedance constant, $\mu_{n/p}$ is the mobility of electrons/hole, $C_{oxn/p}$, $L_{n/pi}$, $W_{n/pi}$ are the gate oxide capacitance, the length and the width for i_{th} of nMOS and pMOS respectively.

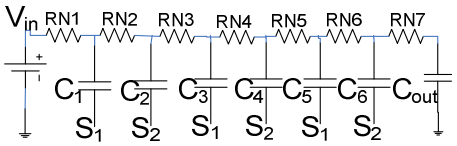
V. SIMULATION RESULTS

Three different charge pump topologies were simulated in Advanced Design System 2009 based on 0.35 μm CMOS technology. To have an equal comparison, all charge pumps were simulated on their best performance setting. Width of nMOS and pMOS, charge storage capacitances (*C*) and output capacitance (C_{out}) were set at their respective optimum values based on previous research works [5, 6, 10, 13], while length of nMOS and pMOS were set slightly higher than the minimum channel length i.e. 0.5 μm. Three of the charge pumps were driving the same load of output impedance. By using similar output impedance for these three charge pumps, their output currents were fixed and the voltages will be evaluated. The charge pumps were switched on and off by two non-overlapping *S1 and S2* with the V_{DD} amplitude of 3.7V. The measurement of the voltage drop across respective switches was performed in steady state, where the dynamic loss can be neglected. The steady state of the switches with an approximately similar number of components used in Dickson, Voltage Doubler [14] and Makowski charge pumps are shown in Fig. 1, 2 and 3 respectively. In the figures, the RN and RP are representing the on-resistance in nMOS and pMOS respectively in steady state.

Fig. 4 shows the simulation results of the average voltage drop due to on-resistance in respective switches of different charge pump topologies. All of the charge pump topologies have half of their total on-resistance switches operated in each clock cycle. In terms of the values of on-resistance per switch, Makowski topology has the lowest on-resistance with its high V_{GS_eff} and *W/L* ratio. For the Voltage Doubler, cross-connected structure leads to transistors operating in the linear to weak region. Low $V_{GS,eff}$ results in slightly higher on-resistance, however, this topology is designed for low voltage transistors [10] with lower V_{TH}, thus in practice a lower voltage drop can be obtained. Dickson charge pump shows the highest voltage drop per switch in the higher stages due to its weaker $V_{GS,eff}$.

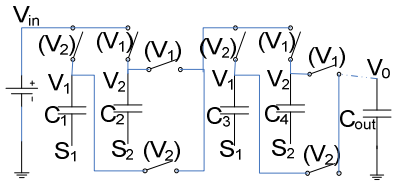


(a)



(b)

Fig. 1 Dickson charge pump (a) Topology (b) Switches in steady state



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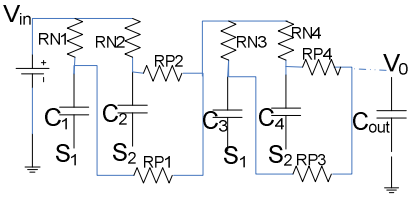
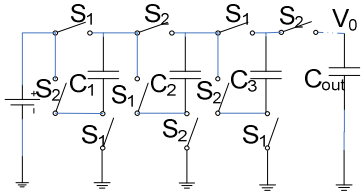
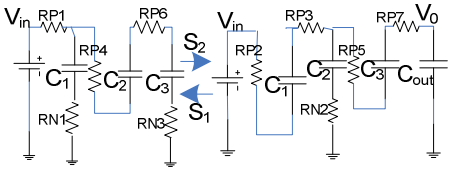


(b)

Fig. 2 Voltage Doubler charge pump (a) Topology (b) Switches in steady state



(a)



(b)

Fig. 3 Makowski charge pump (a) Topology (b) Switches in steady state

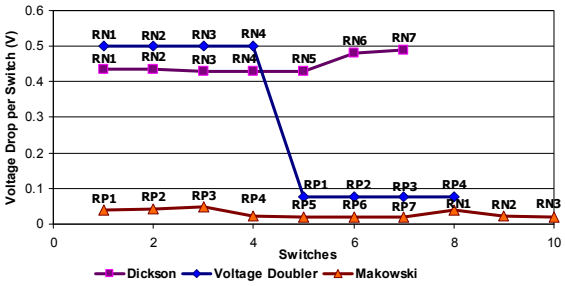


Fig. 4 Voltage drop of 2-phase charge pumps by switches in steady states

VI. Analysis of Dynamic State Switches in Charge Pumps

In a dynamic state, the main charge loss in switches is due to the gate capacitances and drain/source bulk capacitances as shown in (6) and (7).

$$Q_{OX} = C_{ox} V_{GS\_eff} (W_{n/p} L_{n/p}) \tag{6}$$

$$Q_{S/DB} = C_j V_{GS\_eff} W_{n/p} L_{n/p} + 2C_{jSW} V_{GS\_eff} \ (W_{n/p} + L_{n/p}) \tag{7}$$

where Q_{OX} and $Q_{S/DB}$ are the charges consumed by gate oxide and drain/source to bulk capacitances respectively, $W_{n/p}$ and $L_{n/p}$ are the width and length of nMOS and pMOS transistors, C_{OX} is the gate oxide capacitance, C_j and C_{jsw} are the junction capacitances

The $L_{n/p}$, C_j, C_{jsw} and C_{ox} are typically the parameters that can be found in the technology specified. Since $L_{n/p}$ of the transistor in the charge pump is much smaller than $W_{n/p}$, then by simplifying (7) and (6), the total charge loss per switch is developed in (8).

$$Q_{Loss} \approx [C_{ox} L_{n/p} + C_j L_{n/p} + 2C_{jsw}] W_{n/p} V_{GS\_eff} \tag{8}$$

Thus, the total charge loss in switches is proportional to $W_{n/p}$ and the V_{GS_eff} of the transistor.

Fig. 5 shows the total charges consumed by each switch based on different optimized design specifications of charge pump topologies [5, 6, 10, 13]. In these three topologies, the Voltage Doubler shows the lowest charge consumed per cycle due to its narrow channel transistor compared to the others. However, the Voltage Doubler operates at a higher frequency compared to the Dickson and Makowski topologies. Thus, it will eventually accumulate a higher charge loss. Makowski charge pump topology uses higher V_{GS_eff} and greater width of transistor compared with the Dickson charge pump to accommodate the high volume of charge transfer per clock cycle. Thus, higher charge is consumed by switches in Makowski charge pump at dynamic state when compared with Dickson topology as seen in Fig. 5.

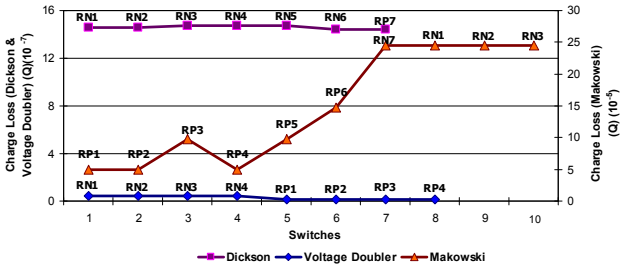


Fig. 5 Total charge loss of charge pumps by switches in dynamic states

VII. Charge Pump for Green Mobile Technology

The Dickson charge pump demonstrates the highest total voltage loss in these three topologies as shown in Fig. 6. High voltage loss is not an option for mobile technology where high energy will be consumed in portable devices. The Voltage Doubler having the intermediate voltage dropped but exhibits the lowest voltage gain in this simulation. More transistors and capacitors are needed to generate the higher conversion ratio. Consequent of using higher stages, higher losses will accumulate in the charge pump. From a green technology point of view, the Makowski charge pump demonstrates the lowest voltage loss in a steady state due to large ratio of W/L.

Even though Makowski topology shows a higher dynamic switches loss, the resulted voltage loss from the dynamic state is relatively low compared to the steady state. Makowski charge pump exhibits the lowest voltage loss either for overall total voltage or voltage dropped per gain in obtaining the highest conversion ratio. Thus, by applying Makowski charge pump topology, a smaller chip area can be achieved for a higher voltage gain without sacrificing the converter size, which is critical for green portable applications.

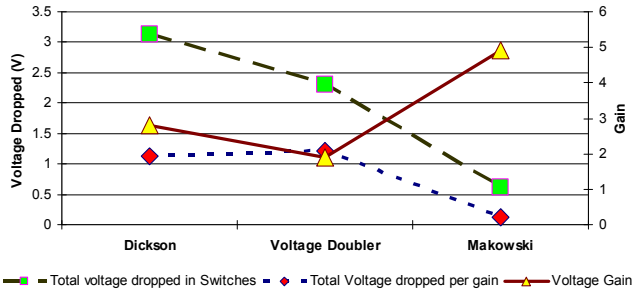


Fig. 6 Comparison of total voltage drop versus conversion ratio amongst various charge pump topologies

VIII. CONCLUSIONS

An analysis on switches applied in different charge pump topologies from the green technology perspective is presented. The nMOS and pMOS require a proper magnitude of V_{GS_eff} for effectively turned on and turned off at the designated clock phases to functions as charge transfer switches. Lower on- resistance at the steady state can be obtained by using higher V_{GS_eff} and W/L ratio. However, greater W of the transistor will cause to higher charge loss in dynamic state. The Dickson charge pump consumes the most voltage loss in a steady state while the Voltage Doubler generates the lowest conversion ratio for an approximately similar number of switches. This work reveals that the Makowski charge pump is the best model for green technology as it provides the lowest voltage dropped in the topology targeting for the highest voltage gain.

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