DEVELOPMENT OF PESONA RISC MICROPROCESSOR ARCHITECTURE IN FPGA

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Sesi Pengajian : 1 3 / 1 4

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Praise be to Allah, His grace, I have been able to perform this project very well. Special dedication to my supervisor, Professor Abdul Hamid Bin Hamidon and a thousand thanks for Encik Sani Irwan Bin Md Salim, a great guidance throughout this project. I would like to take this opportunity to extend my appreciation to everyone who has helped me throughout my final year project especially my research partner, Kartini Binti Zainol Abidin. I express my gratitude and hope that God will repay you well.
ABSTRACT

Pesona is the first Malaysian made 16-bit Microprocessor designed by Malaysian Institute of Microelectronic System (MIMOS). It began when Reduce Instruction Set Computer (RISC) processor was introduced; MIMOS took this as a challenge to produce its own RISC microprocessor in 1994. Since then, there was no attempt to upgrade or continue the Pesona RISC Microprocessor and lead to the idea of implementing this microprocessor in Field Programmable Gate Array (FPGA). With the technological advancement of FPGA, there created a possibility of implementing the Pesona architecture. The objective is to emulate the original Pesona RISC architecture in FPGA platform. To test and verify the architecture Xilinx Virtex-II FPGA was used. The Pesona processor architecture has been design using Verilog HDL. At the end of the project, a processor architecture that emulates the operation of the Pesona processor was developed. Since the architecture is developed using hardware description language, there are a lots of opportunity to improve the processor design.
ABSTRAK

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LIST OF ABBREVIATIONS

FPGA - Field Programmable Gate Array
RISC - Reduced Instruction Sets Computer
ASIC - Application-Specific Integrated Circuit
HDL - Hardware Description Language
SCADA - Supervisory Control and Data Acquisition
ALU - Arithmetic Logic Unit
LUTs - Lookup Tables
RAM - Random Access Memory
AXI - Advanced Extensible Interface
MMU - Memory Management Unit
FPU - Floating Point Unit
ARM - Advanced RISC Machine
PC - Program Counter
RTL - Register Transfer Level
P16 - Pesona 16
IC - Integrated Circuit
COE - Xilinx Coefficient
MUX - Multiplexer
CPU - Central Processing Unit
IDEC - Instruction Decoder
DRAM - Dynamic Random Access Memory
PROM - Programmable Read-Only Memory
SBUS - Source Bus
DBUS - Destination Bus
VHDL - Verilog Hardware Description Language
<table>
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<tr>
<th>Abbreviation</th>
<th>Description</th>
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<tr>
<td>IR</td>
<td>Instruction Register</td>
</tr>
<tr>
<td>ASCII</td>
<td>American Standard Code for Information Interchange</td>
</tr>
<tr>
<td>IP</td>
<td>Intellectual Property</td>
</tr>
<tr>
<td>DMIPS</td>
<td>Dhrystone Million Instructions per Second</td>
</tr>
<tr>
<td>JTAG</td>
<td>Joint Test Action Group</td>
</tr>
<tr>
<td>MMU</td>
<td>Memory Management Unit</td>
</tr>
<tr>
<td>MPU</td>
<td>Memory Protection Unit</td>
</tr>
<tr>
<td>MSB</td>
<td>Most Significant Bit</td>
</tr>
<tr>
<td>LSB</td>
<td>Least Significant Bit</td>
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</table>
CHAPTER I

INTRODUCTION

1.1 Overview

Pesona is a 16-bit Reduced Instruction Set Computer (RISC) Microprocessor fabricated by Mimos Semiconductor which was previously designed in Application-specific integrated circuit (ASIC) environment. Since 1996, it has never been further developed for undisclosed reason. As the first RISC processor designed by a Malaysian company, the rejuvenation of Pesona would motivate processor designer to further developed Malaysia’s own processor.

The purpose of this project is to develop the Pesona RISC Microprocessor architecture in Field Programmable Gate Array (FPGA). The development involves the emulation of Pesona RISC architecture using Verilog HDL in Xilinx ISE environment. The entire original architecture of Pesona such as ALU, stack memory, register array and instruction sets are maintained as originally designed.
1.2 Objectives

The objectives of this project are as follows:

i. To emulate the original Pesona RISC architecture in Hardware Description Language.

ii. To test and verify the architecture using Xilinx Virtex-II FPGA.

1.3 Problem Statement

Since the production of Pesona in late 90’s, there were no attempts or development in upgrading or continuing the Pesona Reduced Instruction Set Computer (RISC) Microprocessor. This could be due to the lack of technological advancement in IC design technology during that particular time and also the competition from the major companies that are already established in this field. Furthermore, the prototype production cost is high and it was not economical to continue the production of this microprocessor especially during the economic recession in the late 90’s.

With the emergence of the Field Programmable Gate Array (FPGA), it opens new opportunities to implement and enhance the performance of the original Pesona architecture. Specifically, Field Programmable Gate Array (FPGA) design could significantly reduce the resource utilization and also improve the clock cycle of the instruction execution time.

1.4 Scope

The scope of this project is to develop a microprocessor in Field Programmable Gate Array (FPGA) by following the original architecture of Pesona Microprocessor. In this project, the reference design based on the 16-bit Reduced Instruction Set Computer (RISC) Pesona original architecture and designed using Verilog HDL. The implementation of the architecture was on Xilinx Virtex-II FPGA.
1.5 Report Structure

Chapter I briefs about the objectives, scope and problem statement of this project.

Chapter II presents in detail the architecture and characteristics of the Pesona Microprocessor. The basic architecture and its origin specification were discussed. It also includes the studies on development and implementation tool in order to implement it in FPGA. Chapter II also contains information regarding the development of microprocessor in FPGA and some examples.

Chapter III gives the methodology requirement on completing the task. All necessary information is included and is supported by flow chart to summarize the method used.

Chapter IV presents the result for this project. All information regarding the results obtained was discussed.

Chapter V concludes all the gathered information and the project itself. Future recommendation for the project is also included.
CHAPTER II

LITERATURE REVIEW

2.1 Pesona Microprocessor

Pesona Microprocessor also known as PI6 is a 16-bit Reduced Instruction Set Computer (RISC) that was designed for high performance with simpler hardware resulting in a high efficient performance. The PI6 is targeted towards embedded applications ranging from controls to communications system including Supervisory Control and Data Acquisition (SCADA), remote monitoring, industrial robotics, home security, appliances, switching equipment and digital set-top boxes [1].

With the RISC architecture, the Pesona Microprocessor operates at 5V DC with maximum clock speed of 20 MHz. The internal architecture is based on Harvard architecture that has 16-bits wide internal data and address buses. Its executes single clock cycle instructions using 4-stages super-pipeline architecture which are fetch, decode, execute and write back as in Figure 2-1.
Refer to figure before, the 4-Stages Super-Pipeline of Pesona which consist of fetch, decode, execute and write back is needed to increase the speed of processing instruction. All the decomposition of the instruction processing as below;

- Fetch – Read the next expected instruction
- Decode – Determine the opcode and the operand
- Execute – Perform the operation and stored in specific destination
- Write Back – Store the result in memory

Pesona Microprocessor has 26 instructions set that support two addressing modes i.e. direct addressing and indirect addressing. The instructions set are divided into five groups like data movement, program and system control, integer and logical arithmetic and data shifting as shown on Table 2-1.
Table 2-1  Instruction Set Summary

<table>
<thead>
<tr>
<th>Instruction Type</th>
<th>Mnemonic</th>
<th>Description</th>
</tr>
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<tbody>
<tr>
<td>Data Movement</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>LB</td>
<td>Load Byte</td>
</tr>
<tr>
<td></td>
<td>LW</td>
<td>Load Word</td>
</tr>
<tr>
<td></td>
<td>SB</td>
<td>Store Byte</td>
</tr>
<tr>
<td></td>
<td>SW</td>
<td>Store Word</td>
</tr>
<tr>
<td></td>
<td>MHI</td>
<td>Move High</td>
</tr>
<tr>
<td></td>
<td>MLO</td>
<td>Move Low</td>
</tr>
<tr>
<td></td>
<td>MFC</td>
<td>Move From Control</td>
</tr>
<tr>
<td></td>
<td>MTC</td>
<td>Move To Control</td>
</tr>
<tr>
<td>Flow Control</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>BEQD</td>
<td>Branch On Equal Zero</td>
</tr>
<tr>
<td></td>
<td>BNED</td>
<td>Branch On NOT Equal Zero</td>
</tr>
<tr>
<td></td>
<td>BSR</td>
<td>Branch To Subroutine</td>
</tr>
<tr>
<td></td>
<td>JMP</td>
<td>Jump Unconditional</td>
</tr>
<tr>
<td></td>
<td>JSR</td>
<td>Jump Subroutine</td>
</tr>
<tr>
<td></td>
<td>TEQD</td>
<td>Trap On Equal Zero</td>
</tr>
<tr>
<td></td>
<td>TNEQD</td>
<td>Trap On Not Equal Zero</td>
</tr>
<tr>
<td></td>
<td>RFE</td>
<td>Return From Exception</td>
</tr>
<tr>
<td>Integer Arithmetic</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>ADD</td>
<td>Add</td>
</tr>
<tr>
<td></td>
<td>SUB</td>
<td>Subtract</td>
</tr>
<tr>
<td></td>
<td>SLO</td>
<td>Set On Lower</td>
</tr>
<tr>
<td></td>
<td>SLL</td>
<td>Set On Less Than</td>
</tr>
<tr>
<td>Logical</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>AND</td>
<td>AND</td>
</tr>
<tr>
<td></td>
<td>OR</td>
<td>OR</td>
</tr>
<tr>
<td></td>
<td>XOR</td>
<td>Exclusive-OR</td>
</tr>
<tr>
<td>Shift</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>SLL</td>
<td>Shift Left Logical</td>
</tr>
<tr>
<td></td>
<td>SRL</td>
<td>Shift Right Logical</td>
</tr>
<tr>
<td></td>
<td>SRA</td>
<td>Shift Right Arithmetic</td>
</tr>
</tbody>
</table>

Table 2-1 bundle the instruction by type which can create more understanding on the instruction set of Pesona. All mnemonic of the instruction set are clearly explained on the description such as MHI which the instruction to move high bit data into register.

PI6 is suitable for used in microcomputer system development with minimum configuration; it is easier to develop and gives more choice to designer for peripherals selection and choosing from different processor family [2].
2.2 Processor in Field Programmable Gate Array (FPGA)

Field Programmable Gate Array (FPGA) is an integrated circuit that has been designed to be configured by user. The configuration of it is exclusively done by using the Hardware Description Language (HDL). The Field Programmable Gate Array (FPGA) is a programmable digital logical chip that can be programmed to do almost any digital function.

The processor consist of a collection of a logic cells called lookup tables (LUTs) that act as a small Random Access Memory (RAM) which can implement any logic function. Each other logic cell can be connected with each other through interconnection resources.

They are two types of FPGA processors which are soft core processor and hard core processor. Soft core processors are implemented or programmed into the FPGA fabric while the hard core one is implemented similar to any integrated circuit as a structure in the FPGA fabric. In this case, a soft core processor have been implemented through instruction sets, arithmetic-logic units, register files, and other features specifically tailored to efficiently use FPGA resources.

A soft core processor can be changed and the code can be modified simply by reprogramming the physical FPGA device with a modified hardware design or upgrading the embedded code in it. So, it could lead to a true field upgradeable hardware and software.

There are a few examples of soft core processor that have been developed such as shown in Figure 2-2, Figure 2-3 and Figure 2-4:-
This soft core processor in Figure 2-2 is based on Xilinx FPGA which uses a 32-bit of Harvard architecture soft processor. Advanced architecture like AXI interface, Memory Management Unit (MMU), instruction and data-side cache, configurable pipeline depth and Floating-Point unit (FPU) are supported by this processor.

MicroBlaze contains over 70 user-configurable options, enabling virtually any processor use case from a very small footprint state machine or microcontroller to a high performance compute-intensive microprocessor-based system running Linux, operating in either 3-stage pipeline mode to optimize size, or 5-stage pipeline mode to optimize speed delivering faster Dhrystone Million Instructions Per Second (DMIPS) performance than any other FPGA-based soft-processing solution.