A Preliminary Study of Characterization Techniques for Reticle ESD Threshold Voltage Measurement

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***Abstract*— Recent studies have revealed that reticle robustness towards electrostatic field is reducing since the feature's critical dimension is getting smaller. Reticle electrostatic damage is seen after the features was subjected at low Electrostatic Discharged (ESD) voltages. This characterization was conducted on a Chrome-on-glass (COG)/Binary reticle metal layer for Complementary Metal-Oxide Semiconductor (CMOS) 250nm technology node. International Technology Roadmap for Semiconductor (ITRS) and Semiconductor Equipment and Materials International (SEMI) uses the results of this reticle electrostatic damaged characterization, extrapolates it and establishes electrostatic field limits for semiconductor industry. Generally, a semiconductor wafer fabrication company will refer to this guideline to set up an Electrostatic Protective Area (EPA) for the expansion of current facilities or new facilities. As CMOS technology node shrinks further to 130nm, the photolithography process becomes more challenging since it requires printing smaller features accurately. A newly advanced reticle, called PSM (Phase-shift Mask) reticle has been introduced. PSM reticle features are made of Molybdenum Silicide (MoSi) material, which is different from the Binary reticle that uses Chromium. Existing guideline for electrostatic control limit from ITRS and SEMI may not be sufficient to protect PSM reticle from ESD damaged due to the different material features and the smaller critical dimension (gap distance between two parallel lines). This paper proposed a future work for characterizing PSM reticle ESD threshold voltage measurement and documented the result in ITRS and SEMI as separate guideline. This study will benefit semiconductor industry to implement more accurate EPA according to reticle type and technology node. The previous characterization techniques will be reviewed and critically compared in order to gain a better understanding of the reticle ESD damaged mechanism and propose new techniques for characterizing reticle that reflect actual production environment, the latest features material and lower technology node.**

***Index Terms*— Characterization, Reticle, ESD, Threshold voltage.**

I. INTRODUCTION

A reticle is like a template/stencil used in photolithography process to project a desired pattern to wafer surface. There are various types of reticle used during semiconductor device fabrication such as poly, metal, via, contact, trench etc and each reticle has distinctive features for patterning each layer on wafer surface. A conventional reticle such as Binary reticle is constructed of a high purity quartz substrate with a thickness approximately 6.35mm that has a nano layer (~100nm) of chrome on the surface which has been etched into patterns called features [1]. Previous studies from researchers in [1-12, 14-16, 18-19] showed reticle could be damaged when it is in close proximity with a charged object.

A charge object emits electrostatic field and polarized the nearby reticle chrome features at different electrostatic force. The nearest chrome features to the electrostatic field will be experiencing greater electrostatic force than the farthest chrome. This creates imbalance of charge levels between chrome features and produced potential difference as long as it is under electrostatic field.

A chrome feature with higher charge will attempt to discharge to the adjacent low charged chrome feature and equalized. The potential difference between the features must exceed the threshold value in order to sustain an air discharge between chrome features. This is called field induced breakdown [1]. Electrostatic reticle damage can result in misprocessing of wafers due to defects on the reticle being projected to wafer surface. This electrostatic reticle damage does not just cause low wafer sort yield but also increases the operational cost associated with repair or remake damaged reticle, which eventually result in a loss of tens of thousands of dollars per reticle. Electrostatic reticle damage becomes an important subject to semiconductor industry in the late 1990s, which resulted in many researchers conducted research on electrostatic reticle damage mechanism and characterizing reticle ESD threshold voltage measurement [8]. In 2003 and 2005, ITRS provided a technology roadmap for maximum allowable electrostatic voltage on reticle for ESD prevention according to technology node from 180nm in year 2000 to 14nm in year 2020 [12]. The maximum allowable electric field voltage on reticle was extrapolated based on the characterization for reticle ESD threshold voltage on older technology node from 375nm to 1000nm [1]. Researchers at that time learned that reticle damaged was due to high voltage discharged between parallel chrome lines align with Paschen law [breakdown voltage, v = pressure (p) * electrode gap distance (d)] for voltage breakdown between two electrodes [13]. In 2004, characterization reticle ESD threshold voltage was carried out on Chrome-on-glass/Binary reticle at 250nm technology node. It was found that damaged observed on chrome lines are cumulative damage mechanisms, in which one of the chrome lines slowly deformed and diffused to the

adjacent line until it developed bridging. This type of electrostatic reticle damage is different from the previous learning, in which ESD occurs as a discrete event once the air breakdown threshold is reached. This electrostatic reticle damage is called Electric Field Induced Migration (EFM) [7]. Reticle EFM damaged happened after extended or repeated low levels electrostatic discharge between electrodes. ITRS 2009 acknowledged the reticle EFM damaged and included remarks for a special guidance needed for EFM prevention, in which these guidelines are available in SEMI standards [12]. In 2012, SEMI established a standard, specifically for EFM prevention (SEMI E163-0212) and recommended a guideline for ambient electric field, field recovery time and maximum transient field [2]. There are a few differences between the previous and recent characterization techniques for reticle ESD threshold voltage measurement that resulted in two different sets of recommendations apart from the lower technology node.

It is essential to establish a practical characterization technique for reticle ESD threshold voltage measurement according to technology node and actual production environment facilities of a factory. The combination of these factors will result in establishing a more realistic value of ambient electric field, field recovery time and maximum transient field. This will help factory to practice cost effective spending by implementing facilities electric field control according to the planned technology node. As the device shrinks further to 130nm, printing smaller features accurately could only be achieved with a new advanced reticle, called PSM (Phase-shift Mask) reticle. PSM features are made of Molybdenum Silicide (MoSi) material, which is different from Binary reticle with Chrome. Thus, a new characterization of reticle ESD threshold is needed to accommodate PSM reticle and further lower technology node and new electrostatic control limit may be established. This paper proposed a future work for characterizing PSM reticle threshold voltage measurement and documented the result in ITRS and SEMI as a separate guideline.

II. Reticle Test Plate

A reticle test plate has been developed for the purpose of characterizing ESD threshold voltage. The reticle test plate is designed according to the current and future technology node. The width of the gap between the line and body determines a technology node. Gap width is a variable factor that determines reticle ESD threshold voltage measurement. The body has a wide area intentionally to interact with the external electric field and to store more energy. The design of the line is long and thin for creating ionization effect at the edge of line. The air surrounding the line slowly becomes ionized, creating conducting bridge between the line and the adjacent body. This situation enables voltage breakdown and electrostatic discharged from the line to the body. Reticle test plate has been used to simulate the actual reticle handling in the production environment. J. Montoya et al., 2001 [1] designed chrome-on-glass reticle test plate for characterizing reticle ESD threshold voltage for 0.38 µm to 1µm technology nodes. The features are laid in 4 sets of 5 strings with 15 test modules in each string. This reticle test plate design is shown in Figure 1.

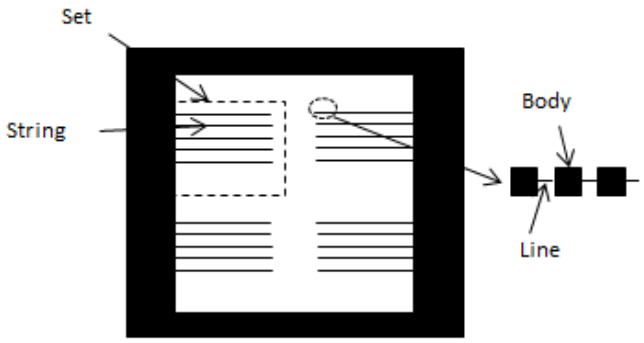

Figure 1: Reticle test plate design from J. Montoya et al, 2001 [1] consists of a single pattern with various line gap widths between line and chrome border in string. There are 4 sets available in this design and each set have 5 strings.

A. Rudack et al., 2002 [3] applied the same methodology as J. Montoya et al., 2001 [1] in reticle test plate design but at a lower technology node. Further, the feature consists of parallel lines without incorporating the body of the study on electric field interaction between the parallel lines and the ionization effect along the side. The voltage breakdown threshold measurement along the line will be different from the measurement at the corners. C. Turley et al., 2013[8] developed reticle features design with cavities that totally different from other researchers. The feature was constructed with multiple cavities along a line. Damages were seen at the bottom of cavities similar to EFM type 1 [6]. The design of this feature is specific for an industry in which the limits of EFM threshold voltage may need to be characterized by the industry considering the ITRS or SEMI standard guideline is referred to [1, 3, 9, 14].

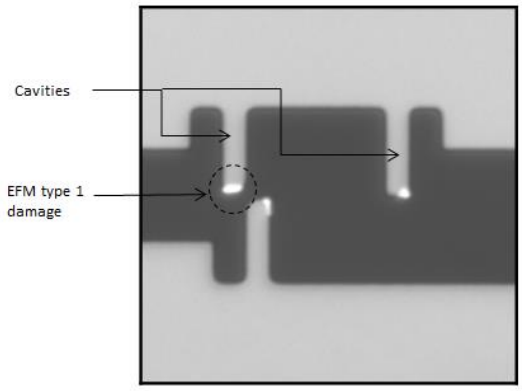

Figure 2: EFM type 1 damaged are seen at bottom corner cavities after reticle test plate inside monopod was expose to ambient electric field. Image was taken with optical microscope [8].

G. Rider et al., 2008 [9] designed a chrome-on-glass reticle with variables for a line length and width and a gap width between the line and the border. The technology nodes are ranged from 0.25µm to 2.5µm for characterizing reticle electrostatic damage at low and high threshold voltage. The features are laid in 8 x 8 columns, which each column consists of 5 x 5 cells. Each cell has a single pattern with a body and a

line. The gap width between the line and the chrome border varies from 0.25µm to 2.5µm. The reticle test plate design is shown in Figure 3 .The author predicts that low discharge voltages will occur at lower technology node as the gap width between the line and the border is narrow, whereas high discharge voltage will happen at a wider gap width between the line and the border. Low discharge voltages between lines will produce milder degree of reticle electrostatic damaged. This type of reticle electrostatic damage is called EFM. High discharge voltages between lines will produce gross reticle electrostatic damage. This type of reticle electrostatic damage is known as ESD.

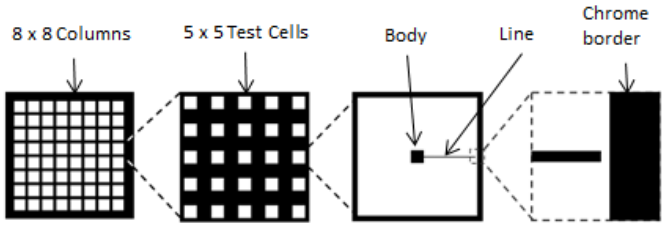

Figure 3: Reticle test plate design from G.Rider, 2007 [9] consists of a single pattern with various gap widths between line and chrome border in 5 x 5 cells. This cell is then repeated in 8 x 8 columns.

A. Englisch, 2003 [14] patented a chrome-on-glass reticle test plate for characterizing reticle ESD threshold voltage for 0.38µm to 3.8µm technology node. The features are laid in 6 sets of 30 strings. Each string consists of single pattern with various body area, line width, line length and gap width between the line and the body. The reticle test plate design is shown in Figure 4.

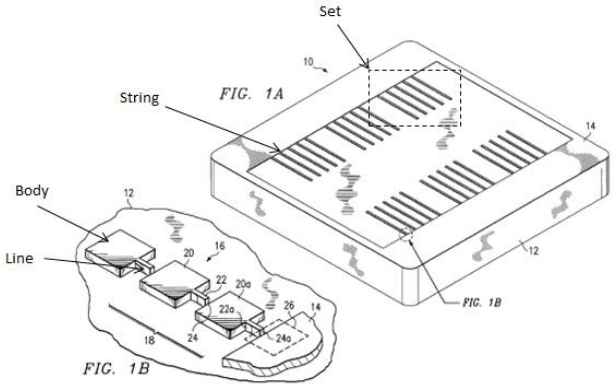

Figure 4: Reticle test plate design from A.Englisch, 2003 [14] consists of a single pattern with various line widths, line lengths and gap widths between line and chrome border in string. There are 6 sets available in this design and each set have 5 strings.

A comparison of the previous research works on reticle test plate design from the earlier technology node until 0.25µm are summarized in Table 1.

Table 1
Comparison of previous research works in developing reticle test plate design

No.	Title/Author/Year	Remarks
1 [1]	A Study of the Mechanisms for ESD Damage to Reticles. J. Montoya et al, 2001	Reticle with features of 4 sets of 5 strings with each string including 15 test modules. Each test module dimension are; i. Body area, square – 6mm^2 ii. Line length –4 um. iii. Line width – 2 µm iv. Gap width between line and body – 1.5µm to 4 µm. v. Distance between test module's line and chrome boarder is 1.5µm. vi. Material – features (chrome), substrate (quartz).
2 [3]	Creating and Measuring Photomask Damage. A. Rudack et al, 2003	Reticle with test module features dimension as follows; i. Line length –10 um. ii. Line width – 4 µm. iii. Gap width between parallel lines (side) – 1µm. iv. Material – features (chrome), substrate (quartz).
3 [8]	Evaluating Electrostatic damage prevention methods for full-scale reticle manufacturing. C. Turley et al, 2013	i. Reticle with test module features of cavities. ii. Material – features (chrome), substrate (quartz).
4 [9]	Experimental quantification of reticle electrostatic damage below the threshold for ESD. G.Rider et al, 2008	Reticle with features of 8 x 8 columns of test cells in groups 5 x 5. Each test cell dimension are; i. Body area, square - 100µm x 100µm. ii. Line length - 1µm to 10µm iii. Line width – 1µm to 10 µm. iv. Gap width line to chrome border – 1µm to 10 µm. v. Border area, square 1mm x 1mm. vi. Material – features (chrome), substrate (quartz).
5[14]	Test Photomask and Method for Investigating ESD-Induced Reticle Defects. A.Englisch, 2003	Reticle with features of 6 sets of 5 strings with each string including 25 test modules. Each test module dimension are; i. Body area, square – 0.1mm x 0.1mm to 4mm x 4mm . ii. Line length – 0.2mm to 0.5mm. iii. Line width - 1.5µm iv. Gap width between line and body – 1.5µm to 15 µm. v. Distance between test module's line and chrome boarder is 1.5µm. vi. Distance between strings is 5mm. vii. Material – features (chrome), substrate (quartz).

Based on the previous research works in reticle test plate the design was up to 0.25µm technology node using chrome-on-

glass reticle. In recent years, the technology node is getting lower than 0.25µm and advanced PSM reticle has been introduced for printing smaller features at 130nm and below critical dimension. The PSM features do not only have smaller gap width, but they are also made of Molybdenum Silicide (MoSi) material. Further, the MoSi melting point is 2,030ºC [18], higher than the Chromium, which is 1863ºC [17]. The high melting point property is an advantage to withstand thermal heating after voltage discharged. Therefore, the effect of reticle ESD threshold voltage based on the combination of MoSi material and lower technology node factor of the new reticle test needs to be studied.

III. RETICLE STRESS TEST

A reticle stress test simulates the approximate condition of reticle that has been exposed to ambient electric field in the production floor. There are three important factors that are taken into account when developing reticle stress test, which are the source of electric field, exposure duration and grounding. The electric field strength will be different from one production site to another because of the different set up of the facilities. It depends on the type of materials and equipment used in the production floor. The method of handling reticle depends on the manufacturing process, in which the reticle will be exposed to ambient at certain duration during preparation, inspection and wafer patterning. Reticle is mobile during each process, and at each step of the process, it will be at a grounded plane or isolated. There will be a difference in electric field distribution when the reticle is in grounded or isolated condition. All these three factors will be determined and used for reticle stress test simulation,

J. Montoya et al., 2001[1] applied field induced and charged device models that represent the actual reticle handling at the production floor. An example of field induced model is when a reticle is being loaded into a stocker, in which the equipment panels are made of plastic. The plastic is a source of charge that could polarize the reticle, when it is in close proximity. The second model described by J. Montoya et al., 2001 [1] is a charged device model, in which an operator handles the reticle with gloved hands when transferring the reticle case into a monopod. The applied voltage is considered high for current Reticle EPA because most industries are equipped with ionization to lower down the ambient of electrostatic voltage. Typically, ambient electric field is controlled at below 300 V/in. Two exposure durations need to be taken into consideration because there are differences in the degree of damage seen on reticle features, which are either catastrophic failure (ESD event, which produces mouse-bite symptom) or latent failure (EFM type 1 and type 2 event, in which the metal is diffused until it becomes a bridging between two lines). J. Montoya et al., 2001[1] characterized the reticle ESD threshold voltage measurement under grounded condition, in which the electric field perturbation influences the EFM effect at the ground point. Less electric field perturbation may occur at features that are far away from the ground point. A. Rudack et al., 2002 [3] applied the same methodology of field induced model but used different type of voltage source, which is repeatable square wave pulse. Field perturbation of isolated reticle was studied besides the grounded reticle. As the device shrinks, a study of lower voltage discharge that causes latent failure and EFM damage was carried out [9]. A low voltage in hundred volts and below is applied directly to the reticle features for a long duration. This method does not consider field perturbation from the external charge source and it may not represent the actual handling of reticle in the production floor. However, this method of testing is more repeatable than the field induced method by A. Rudack et al., 2002 [3] because of less electric field losses due to humidity and field perturbation effects.

Comparisons of previous research works on reticle stress test from characterizing ESD threshold voltage are consolidated into Table 2.

Table 2
Comparison of previous research works in developing reticle stress test

No.	Title/Author/Year	Remarks
1[1]	A Study of the Mechanisms for ESD Damage to Reticles. J. Montoya et al, 2001	Methods, equipment and materials that been used for developing reticle stress test are as follows, i. Field induced and charged device models. ii. Applied voltages 0-7.5kV ramp, 0-10kV ramp and 0-17kV ramp. Using high voltage dual polarity power supply. iii. Exposure duration – single and multiple shot. The duration of each shot depend on ramping time. iv. Reticle test plate sit on grounded plane.
2[3]	Creating and Measuring Photomask Damage. A. Rudack et al, 2003	Methods, equipment and materials that been used for developing reticle stress test are as follows, i. Field induced model. ii. Applied voltages 0-10kV. Using Bertan Series 230 high voltage power supply with an analog programming pulse generator to provide square wave pulse dual polarity. iii. Exposure duration – 20 cycles shot with rise time ~100ms. iv. Reticle test plate sit on grounded and unground plane.
3 [9]	Experimental quantification of reticle electrostatic damage below the threshold for ESD. G.Rider et al, 2008	Methods, equipment and materials that been used for developing reticle stress test are as follows, i. Direct discharge to features using micro-probe electrical test. ii. Applied voltages 1-100V dual polarity. Using HP406 programmable parameter analyzer. iii. Exposure duration – 15 seconds per shot. 20 shots per test module. iv. Reticle test plate sit on grounded and unground plane. v. Room temperature was 70ºF and Relative Humidity was 50%

There have been research works in developing reticle stress test that employed electric field induction and direct discharge at various electrostatic voltages. There are methods that can be further improved in order to develop reticle stress test with higher repeatability and applicable to current actual production floor environment.

IV. CONCLUSION

In this paper, previous research works in characterization techniques for reticle ESD voltage measurement were reviewed. Two significant areas were reviewed in detail, which are the reticle test plate design and the reticle stress test. Researchers developed reticle test plate design and reticle stress test are based on the parameters gathered from the actual production facilities environment and technology node available during that period of time. Guidelines outlined by ITRS and SEMI are based on research works for industry to control ambient electric field to a certain level which prevent ESD or EFM occurrence. However, these guidelines are useful for industry using older technology node, which is the photolithography wafer patterning process using chrome-on-glass reticle. As the device is shrinking further, photolithography process enhancement is needed to achieve wafer patterning at lower critical dimension. This has led to the development of more advanced reticle, such as the PSM to overcome the limitations from the Binary reticle in wafer patterning for lower technology node. Using the current guidelines from ITRS and SEMI for the setup of the production facilities may not be sufficient to protect PSM reticle from EFM damage since the characterization of EFM threshold was based on chrome-on-glass and older technology node. PSM reticle is using MoSi-on-glass, in which its material properties are different from the chrome-on-glass. Therefore, an accurate electric field threshold voltage measurement is essential to be established for PSM reticle at lower technology node. By establishing a new guideline for PSM reticle using actual reticle handling environment, it will help industry in setting up production facilities in cost effective manner by implementing electric field voltage control according to current and future needs. Apart from this, it will help the industry to prevent losses from remake or make a new set of reticle due to EFM damaged. Future characterization techniques for reticle ESD threshold voltage should be continued and aligned with the photolithography advancement for upgrading current production facilities or installing new facilities for ESD or EFM prevention.

ACKNOWLEDGMENT

Authors sincerely to express their gratitude and appreciation to Universiti Teknikal Malaysia Melaka (UTeM), Silterra Malaysia Sdn. Bhd and Ministry of Higher Education (MOHE) for research guidance and scholarship.

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