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DESIGN AND CHARACTERIZATION OF 20NM SOI MOSFET DOPING ABRUPTNESS DEPENDENT

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ABSTRACT

SOI MOSFET has currently become a trend for low power devices such as palmtops, cell phone, and other devices because it has a lot of advantage in terms of speed, density, and performance gain. Various efforts have been done to continue the progress in shrinking dimensions and higher-frequency performance will be driven by the market application. Reducing the size of SOI MOSFET will reduce the power, body effect, and parasitic capacitance, and increase the density and so on. This project focused mainly on the source/drain doping abruptness of SOI MOSFET. The doping abruptness was varied to find the best doping profile since the device was shrinking. In order to vary the source/drain doping abruptness, there were several problems to be encountered, which were increase in resistance, increase in threshold voltage, small sub-threshold slope, and others. The purpose of this project was to design the SOI MOSFET with an ideal doping profile and to investigate the impact on threshold voltage, current, and sub-threshold slope due to the variation of source/drain doping abruptness of SOI MOSFET. This project was designed using Silvaco Athena and Silvaco Atlas. Silvaco Athena was used to simulate the device structure and Silvaco Atlas was used to obtain the device characteristics of SOI MOSFET. This whole project was implemented on an SOI MOSFET doping abruptness dependent with a gate length of 21 nm.

Keywords: technology SOI, fully-depleted SOI MOSFET, source/drain doping abruptness, and Silvaco software.

INTRODUCTION

In the VLSI (very large scale integration) era, reducing power consumption become the most important issue. Lots of techniques have been done to solve these issues until the bulk technology reaches its limits. For example, they the size of MOSFET has been reduced, the material has been changed, the doping has been increased, etc. Silicon on insulator (SOI) is also introduced as one of the alternatives to solve the problem occurs at bulk MOSFET. SOI technology features low capacitance, which enables high-speed operation. So, the supply voltage can be lowered to cut the power consumption while adequate speed is provided. SOI is not only limited to power and speed, but it also has other advantages in terms of isolation, density, and performance gain in low power electronics. Due to those advantages, the demand is continuing and drawing the force towards further downscaling the device feature size. However, continuing scaling down the device continues to improve but the parasitic component of the device such as the series resistance in the source/drain region starts to limit the device performance. This project focuses on the impact of source/drain doping abruptness of SOI MOSFET since the size of the SOI MOSFET is scaled down. The concentration of SOI MOSFET doping is varied and the gate control of the channel potential is enhanced. In order to vary the doping abruptness of SOI MOSFET, there are several problems to be encountered, which are the increase in resistance, small sub-threshold slope, degrades the device on-current, etc. The purpose of this project is to design the SOI MOSFET with the best source/drain doping abruptness and to investigate the impact on voltage, current, and sub-threshold slope of the SOI MOSFET due to the varied doping abruptness of SOI MOSFET. This whole project is implemented in a 20 nm SOI MOSFET gate length.

DEVICE DESIGN

Through The structure of SOI MOSFET was designed by referring to the standard parameter of low operating power (LOP) technology requirements of SOI MOSFET from ITRS 2013. Table-1 shows the values and the dimension of the device parameters.

Table-1. The values and the dimension of the device parameters.

Parameters	**Doping abruptness** (nm/dec)		
	3.3	**3.5**	**3.8**
Channel Length (nm)	100 nm	100 nm	100 nm
Bulk (Handler) Thickness (nm)	22 nm	22 nm	22 nm
Buried Oxide (nm)	18 nm	18 nm	18 nm
Body Thickness (nm)	16 nm	16 nm	16 nm
Gate Length (nm)	20 nm	20 nm	20 nm
EOT (nm)	0.8 nm	0.8 nm	0.8 nm
Channel Doping (/cm^3)	3×10^{20}	2×10^{20}	1×10^{20}
Drain Voltage (high voltage, V)	1	1	1
Drain Voltage (low voltage, V)	50 mV	50 mV	50 mV

From the Table-1, all parameters for the three designs were fixed except the channel doping concentration of the device. The channel length used was 100 nm. The bulk thickness or handler was 22 nm. The body thickness was 16 nm. EOT or the thin layer of the device was 0.8 nm. The channel doping concentrations of the three structures were 3.3 nm/dec for 3×10^{20}, 3.5 nm/dec for 2×10^{20}, and for 3.8 nm/dec for 1×10^{20}. The drain voltage applied to this device was 1 V for high voltage and 50 mV for low voltage.

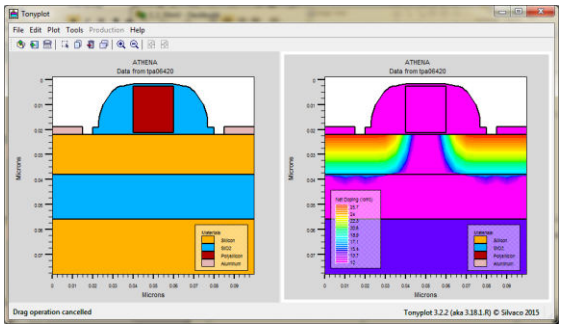

Figure-1. Complete design of the device with doping.

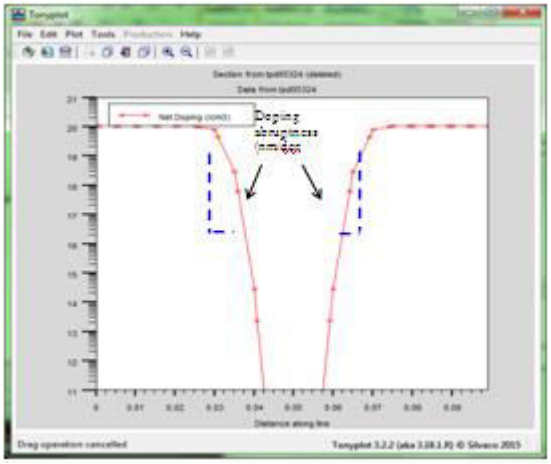

Figure-2. Doping concentration graph.

Doping Abruptness, σ

$$= \left|\frac{log\ y_1 - log\ y_2}{x_1 - x_2}\right|^{-1}(nm/dec)$$

To complete this project, the TCAD (the technology-aided design) software by Silvaco was used. Silvaco Athena was used to integrate the process simulation of the framework. The structure of the SOI MOSFET was designed by using Athena. Silvaco Atlas was used to do the device simulation framework. The characteristics of the device such as electrical, optical, and thermal behaviour of the semiconductor device can be simulated by Atlas.

SIMULATION RESULTS

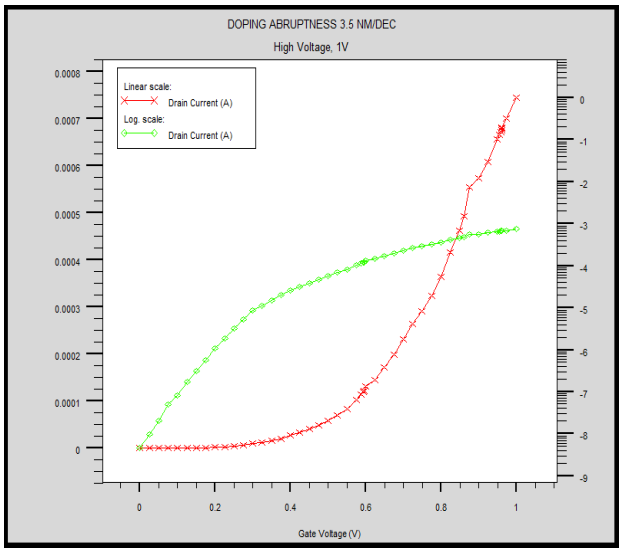

Figure-3. Linear graph and log graph Id versus Vgs for 3.3 nm/dec doping abruptness (Vds = 1V).

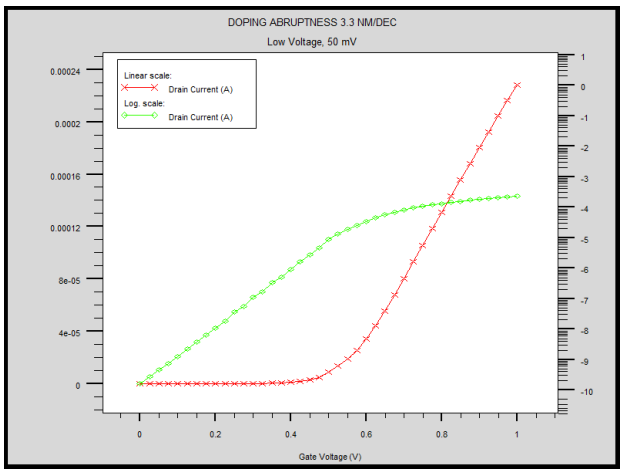

Figure-4. Linear graph and log graph Id versus Vgs for 3.3 nm/dec doping abruptness (Vds = 50mV).

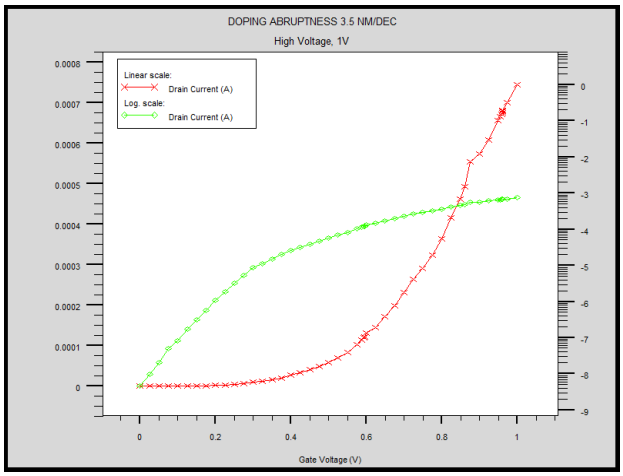

Figure-5. Linear graph and log graph Id versus Vgs for 3.5 nm/dec doping abruptness (Vds = 1V).

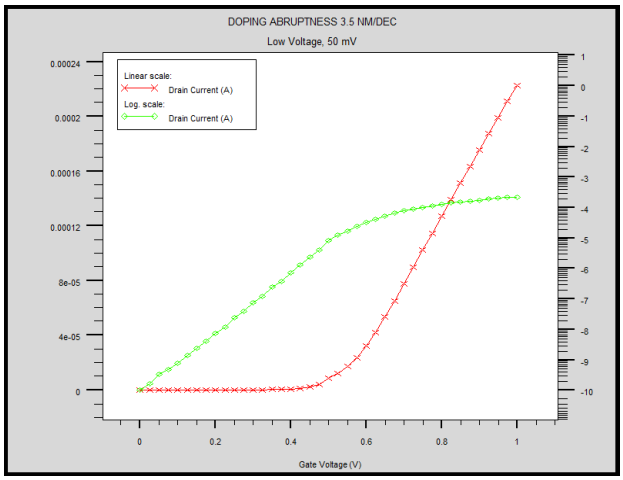

Figure-6. Linear graph and log graph Id versus Vgs for 3.5 nm/dec doping abruptness (Vds = 50mV).

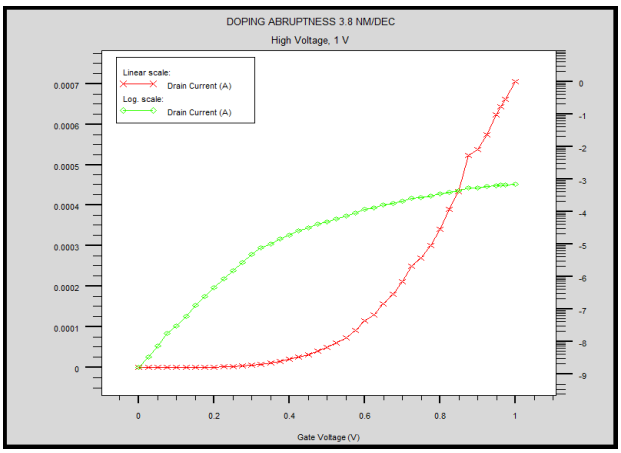

Figure-7. Linear graph and log graph Id versus Vgs for 3.8 nm/dec doping abruptness (Vds = 1V).

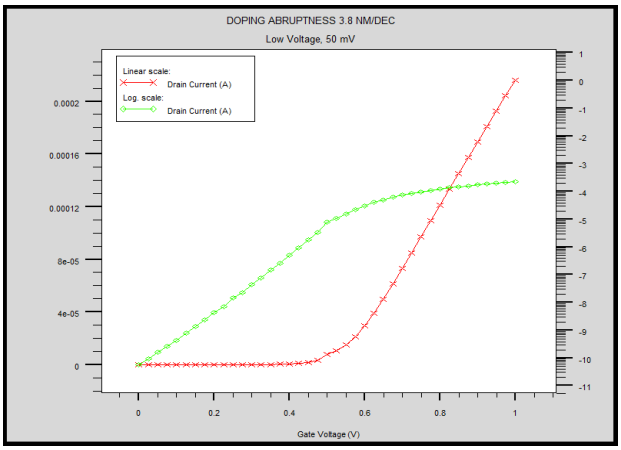

Figure-8. Linear graph and log graph Id versus Vgs for 3.8 nm/dec doping abruptness (Vds = 50mV).

i) Drain current

Comparing the three source/drain doping abruptness (3.3 nm/dec, 3.5 nm/dec and 3.8 nm/dec), the structure with 3.3 nm/dec showed highest drain current which was 769 µA compared to 3.5 nm/dec and 3.8 nm/dec which were 744 µA and 705 µA respectively with high drain voltage, 1 V. When low drain voltage (50 mV) was applied, the value of drain current decrease as the doping abruptness increase. The value of drain current obtained was 228 µA, 222 µA, and 215 µA for 3.3 nm/dec, 3.5 nm/dec, and 3.8 nm/dec doping abruptness respectively.

ii) Leakage current

Even though the drain current improved as the value of source/drain doping abruptness decreased, the current leakage of the device become worse but it was still acceptable. When 1V drain voltage was applied, the leakage current of 3.3 nm/dec doping abruptness was 10.4 nA which was 0.00135% of the drain current. For 3.5 nm/dec doping abruptness, the leakage current was 4.67 nA which was 0.00063% of the drain current, and for 3.8 nm/dec, the leakage current was 1.5 nA which was 0.00021% of the drain current. For 50mV drain voltage,

the leakage current for 3.3 nm/dec doping abruptness was 0.16 nA which was 0.00007 % of the drain current, for 3.5 nm/dec doping abruptness the leakage current was 0.10 nA which was 0.00004% of the drain current, and for 3.8 nm/dec the value of leakage current was 0.056 nA which as 0.00002% of the drain current.

iii) Sub-threshold slope

Since the value of the concentration of doping profile ncreased as the value of doping abruptness decreased, the carrier mobility was reduced due to impurity scattering and will increase the sub-threshold slope. When 1V drain current was applied to the device, the value of sub-threshold slope of 3.3 nm/dec doping abruptness was 74 nm/dec, but for 3.5 nm/dec doping abruptness the value of sub-threshold slope was 62 nm/dec, and for 3.8 nm/dec doping abruptness, the value of sub-threshold slope was 61 nm/dec. When low drain voltage (50 mV) was applied, the value of sub-threshold slope of 3.3 nm/dec, 3.5 nm/dec, and 3.8 nm/dec doping abruptness was 81 nm/dec, 82 nm/dec and 66 nm/dec respectively.

iv) The threshold voltage

In comparison of the threshold voltage, the device with 3.3 nm/dec doping abruptness showed the best result with the lowest value of V_{th} which was 631 mV, and for 3.5 nm/dec and 3.8 nm/dec doping abruptness, the V_{th} values were 818 mV and 677 mV respectively, when high value of drain voltage (1V) was applied. When low value of drain voltage (50mV) was applied, the value of threshold voltage for 3.3 nm/dec doping abruptness was 539 mV, for 3.5 nm/dec doping abruptness was 542 nm/dec, and for 3.8 nm/dec doping abruptness was 547 mV.

Table-2. The electrical characteristics for 3.3, 3.5, and 3.8 nm/dec doping abruptness.

Using × 10^{20}				
Drain voltage	**Electrical characteristic**	**Doping Abruptness** (nm/dec)		
		3.3	**3.5**	**3.8**
1 V	Drain Current (µA)	769	744	705
	Leakage Current (nA)	10.4	4.67	1.5
	Sub-threshold Slope (mV/dec)	74	62	61
	Threshold Voltage (mV)	631	818	677
50 mV	Drain Current (µA)	228	222	215
	Leakage Current (nA)	0.16	0.10	0.056
	Sub-threshold Slope (mV/dec)	81	82	66
	Threshold Voltage (mV)	539	542	547

CONCLUSIONS

Based on the comparison of 3.3 nm/dec, 3.5 nm/dec, and 2.5 nm source/drain doping abruptness of SOI MOSFET, the device with 3.3 nm/dec delivered the best result performance than the others. Even though its leakage current was high than the devices with 3.5 nm/dec and 3.8 nm/dec doping abruptness, it has the most advantage in terms of drain current, sub-threshold voltage, and threshold slope.

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