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# ELECTRICAL CHARACTERISTICS OF PMOS BULK MOSFET AND PMOS SILICON-ON-INSULATOR (SOI) MOSFET DEVICE

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**ABSTRACT**

Nowadays, conventional Metal Oxide Semiconductor Field Effect Transistor (MOSFET) has been undergoing major improvement. This improvement is about the introduction of technique that buries the Buried Oxide layer in an MOSFET. This method is known as Silicon-on-insulator (SOI) and it is believed to be able to suppress the Short channel effect (SCE). The SCE is a trigger to diminish the electrical characteristics of a MOSFET device and by introducing this buried oxide layer, it can suppress this SCE. With SCE suppressed by buried oxide layer, electrical characteristics of an MOSFET can be improved; thus the performance of the device can increase tremendously. In this paper, Silvaco ATLAS and Silvaco ATHENA modules have been used. ATHENA module is used to design the structure layout of SOI MOSFET device. Meanwhile, ATLAS module is employed to extract electrical characteristics of design structure of the device. Conventional PMOS Bulk MOSFET and SOI PMOS was designed and constructed. These two electrical results have been observed and analyzed. As a conclusion, the SOI PMOS device is clearly superior compared to the bulk PMOS device.

**Keywords:** Athena, Atlas, PMOS, SOI, MOSFET.

## INTRODUCTION

Complementary Metal-oxide Semiconductor (CMOS) consists of two parts, which are N-type and P-type MOSFET, or also known as NMOS and PMOS. This NMOS is slightly different from PMOS. NMOS transistor is made up of n-type source and drain and a p-type substrate. When a voltage is applied to the gate, holes in the body (p-type substrate) are driven away from the gate. This allows the formation of an n-type channel between the source and the drain, and a current is carried by electrons from source to the drain through an induced n-type channel while a PMOS transistor is made up of p-type source and drain and an n-type substrate. When a positive voltage is applied between the source and the gate, a p-type channel is formed between the source and the drain with opposite polarities.

The current is carried by holes from source to the drain through an induced p-type channel. These two NMOS and PMOS transistor also operate in different situations. A high voltage enables NMOS to operate while a high voltage on the gate will cause a PMOS not to conduct, while a low voltage on the gate will cause it to conduct. PMOS device has a lot of advantages such as highly controlable, low cost process, good yield and high noise immunity [1]. This PMOS then will provide buried oxide layer that is Silicon on insulator (SOI) MOSFET technology to increase its performance and thus limiting the short channel effect (SCE). This dependency enables the superior control of drain biases, carrier velocity saturation and channel length modulation. It affects out conductance, as well as device degradation due to channel effect immunity to SOI MOSFETS. One of the advantages of SOI MOSFET over their bulk silicon counter parts is its ability to operate in a very high-speed switching due to its lower parasitic capacitances [2].

In this paper, the overall structure was developed using Technology Computer Aided Design (TCAD) tools, which is known as SILVACO intentionally. The structure of SOI MOSFET and Conventional Bulk MOSFET were constructed using SILVACO TCAD Tools. These two structures were developed by using Athena module, while electrical characteristic analysis used Athena module [3,4]. The electrical characteristics of these structures were compared and analyzed. The results show that SOI PMOS device is clearly superior compared to the bulk PMOS device.

## DESIGN STAGE OF PMOS SOI MOSFET

Firstly, the main substrate, which is P-type silicon with <100> orientation was used, followed by Buried Oxide Layer (BOX) formation. 200Å oxide layer was grown on top of silicon bulk. This oxide layer is significant as it has been employed as a mask during N-well implantation process. Buried Oxide Layer (BOX) was deposited. Later on, when the doping process was completed, the oxide layer was engraved and it was followed by annealing process. The purpose of annealing process was to beef up the device's structure. Afterwards, shallow trench isolation (STI) was taken in parliamentary procedure to isolate the neighbor transistor. A 130Å stress buffer was used on the wafers with 25 min diffusion processes. LPCVD process, or known as Low-Pressure Chemical Vapor Deposition, was used to deposit a 1350Å nitride layer. The use of nitride layer was to behave as a mask when silicon was etched to expose the STI area. Photo resistor layer was then banked on the wafer layer and any unwanted parts were etched away using the Reactive Ion Etching (RIE) process. The primary function of oxide layer grown on the trench sides was to get rid of impurity from entering the silicon substrate [5].

After that, to eliminate extra oxide on the wafer, chemical Mechanical polishing (CMP) was applied. A sacrificial oxide layer was then grown and etched to eliminate any defects on the surface. The gate oxide must

be produced before the Boron Difluoride (BF2) threshold-adjustment procedure. The polysilicon gate was then deposited and followed by halo implantation. To achieve a better and optimum performance for MOSFET device, indium was doped. Sidewall spacer was then deposited to a mask for source/drain implantation. Boron was implanted with an appropriate value of concentration to get smooth current flow in PMOS device. After that, the silicide layer has been grown and annealed at the top of polysilicon.

The next phase is to deposit Boron Phospor Silicate Glass (BPPG) layer. This layer was a Premetal dielectric (PMD), which is the first layer deposited on the wafer surface when transistor produced. The transistor was then linked to aluminum metal. After that, the second aluminum layer was deposited on top of the intel-Metal Dielectric (IMD) and unwanted aluminium was etched to make the contacts. The step was completed when etching and metallization was performed for electrode formation and bonding pads were opened [4].

## RESULT AND DISCUSSIONS

There are a few main characteristics that will be important for this research toward the conventional bulk PMOS MOSFET and SOI PMOS MOSFET. The main characteristics of these devices are leakage current ($I_{OFF}$), Drive current ($I_{ON}$) and Subthreshold voltage (Ss). These electrical characteristics are important to this research to identify the device performance based on the SCE's suppression, switching speed and driving capability [6, 7].

## STRUCTURE OF BULK AND SOI PMOS MOSFET

Figure-1 shows the structure of Bulk MOSFET without SOI. Meanwhile, Figure-2 indicated clearly the structure of SOI PMOS MOSFET. The buried oxide layer with 10nm thickness is form in this structure.

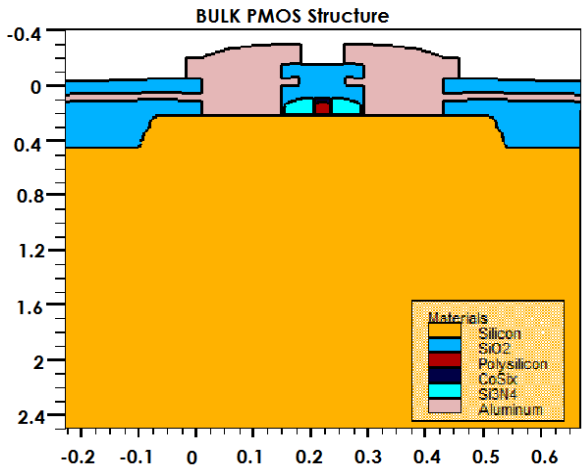


**Figure-1.** Structure of PMOS bulk MOSFET device.

This MOSFET structure contains Silicon, Silicon dioxide, polysilicon, silicon nitride, and cobalt nitride and lastly the aluminium [5]. The study indicated that doping concentration effecting the electrical characteristics of a MOSFET.

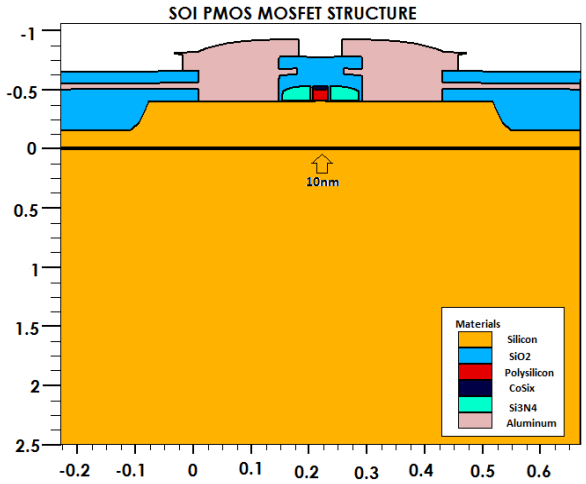


**Figure-2.** Structure of SOI PMOS MOSFET device.

## ELECTRICAL CHARACTERISTICS OF DESIGN STRUCTURES

Figure-3 shows the graph Drain current ($I_D$) versus Gate Voltage ($V_G$) for Bulk PMOS MOSFET. The value of threshold voltage for this structure is 0.2883V and this value is closer to the value of ITRS 2011 [8]. Figure-4 shows the drive current ($I_{ON}$) and leakage current ($I_{OFF}$) of Bulk PMOS MOSFET device. The value of $I_{ON}$ is 239.79µA/µm while for the $I_{OFF}$ is 26.284pA/µm.

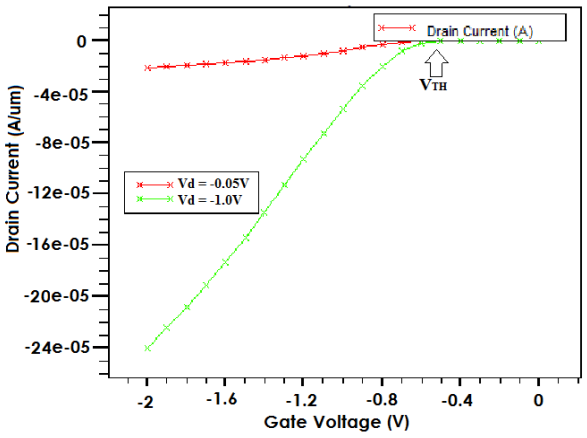


**Figure-3.** $I_D$-$V_G$ graph bulk PMOS.

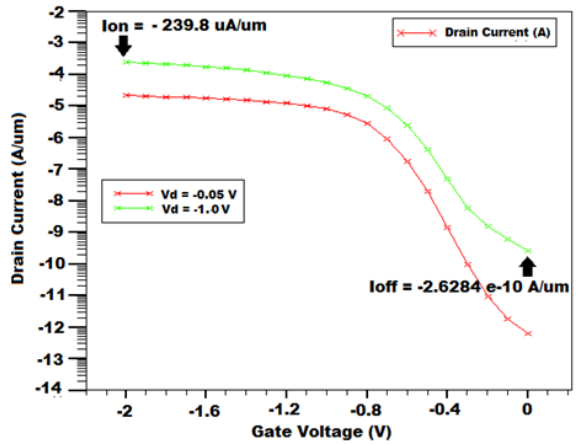


**Figure-4.** $I_{ON}$ and $I_{OFF}$ value for PMOS BULK.

High-performance MOSFET device requires the highest value of drive current ($I_{ON}$) and the lowest value of leakage current ($I_{OFF}$). With these values, the ratio of $I_{ON}/I_{OFF}$ will be increased, thus lowers the power consumption [6]. The electrical characteristics of SOI PMOS MOSFET device can be seen in Figure-5. The result output shows that the $V_{TH}$ for SOI PMOS MOSFET device is 0.2893V. This value is closer to the value of ITRS 2011 [8] and also closer to the value of Bulk PMOS that will be compared later.

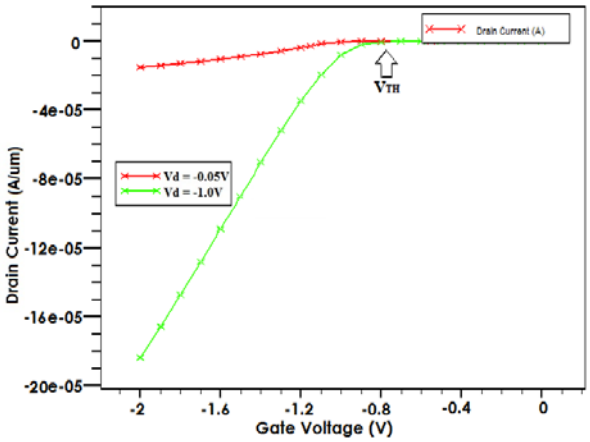


**Figure-5.** $I_D$-$V_G$ graph of SOI PMOS MOSFET.

Figure-6 shows the two output responses of SOI PMOS MOSFET, which are drive current and leakage current. The value of $I_{ON}$ is 183.81µA/µm while the value of $I_{OFF}$ is approximately 0.934fA/µm.

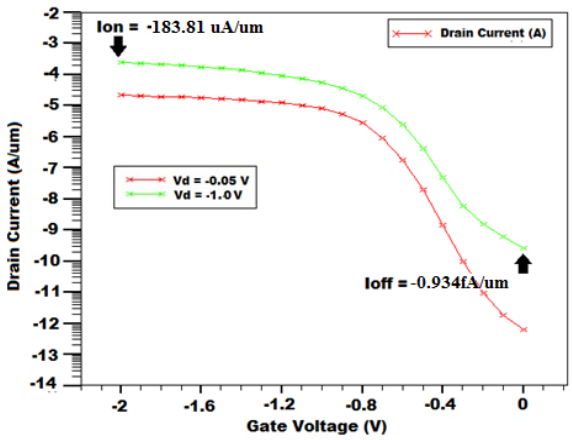


**Figure-6.** $I_{ON}$ and $I_{OFF}$ value for SOI PMOS.

## COMPARISON OF ELECTRICAL CHARACTERISTICS BETWEEN BULK PMOS AND SOI PMOS DEVICES

In this research, there are three electrical characteristics of MOSFET device that will be compared. The overall performance of the MOSFET and electrical characteristics such as $I_{ON}$, $I_{OFF}$ and Ss will be indicated. Table-1 shows the value of each three electrical characteristic for both design structure. These values were extracted from Silvaco Athena module. The value of SOI PMOS is extremely better than conventional bulk MOSFET. This support the theory that the presence of buried oxide layer on an MOSFET device can specifically enhance the electrical characteristics of a MOSFET [6].

**Table-1.** Values of electrical characteristics for both devices.

| Electrical characteristics | Bulk PMOS | SOI PMOS |
|---|---|---|
| $I_{ON}$ | 239.79 µA/µm | 183.81µA/µm |
| $I_{OFF}$ | 26.284pA/µm | 0.934fA/ µm |
| $S_S$ | 106.77mV/dec | 90.64mV/dece |
| Ratio $I_{ON}/I_{OFF}$ | $9.123x10^6$ | $1.968x10^{12}$ |

The value of sub threshold swing needs to be lower so that the switching speed between on to off state MOSFET can be increased [3], thus this SOI PMOS succeeds when these designs exceed tremendously the value of bulk PMOS [6]. The result shows that SOI PMOS surpassed all the characterization compared to bulk PMOS device.

## CONCLUSIONS

This paper is mainly about the investigation and comparison of electrical characteristics between Bulk PMOS and Silicon on insulator PMOS MOSFET. After thorough design and analysis, it shows that the electrical characteristics for SOI PMOS were better than the characteristics of Bulk PMOS. Buried oxide layer in this

SOI PMOS structure enables the reduction of the charge sharing between source region and drain region, thereby increasing the drive current ($I_{ON}$). It is observed that SOI PMOS MOSFET has superior value of electrical characteristics either leakage current or sub threshold swing. With this value it is confirmed that this SOI PMOS is the better device than bulk MOSFET with low power consumption.

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