Faculty Of Electronics and Computer Engineering

FAULT ANALYSIS AND TEST FOR BRIDGE DEFECT IN RESISTIVE RANDOM ACCESS MEMORY

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DECLARATION

I declare that this entitled “Fault Analysis and Test for Bridge Defect In Resistive Random Access Memory” is the result of my own research except as cited in the references. The thesis has not been accepted for any degree and is not concurrently submitted in candidature of any other degree.

Signature :.....

Name :.....

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APPROVAL

I hereby declare that I have read this thesis and my opinion this thesis is sufficient in term of scope and quality for the award of Master of Science in Electronic Engineering.

Signature :.....

Supervisor Name :.....

Date :.....

DEDICATION

To my charming husband

To my beloved mother, father and sister

To my supportive late supervisor

ABSTRACT

Resistive Random-Access Memory (ReRAM) is one of the potential candidates of emerging semiconductor memory to replace the conventional memory technologies. Besides, ReRAM offers many attractive advantages, such as non-volatile, scalable, low power consumption, and fast data access. Due to the infancy stage of this emerging memory, ReRAM is prone to have bridge defects that could lead to test escape and reliability issues. Moreover, with the lack of electrical model for ReRAM, this research presents an electrical ReRAM model that was designed with SILVACO Electronic Design Automation (EDA) software. All ReRAM elements designed used 22nm Complementary Metal Oxide Semiconductor (CMOS) transistors and a novel non-CMOS device, known as memristor, as the memory cell array. The optimal memristor model that had been proposed by D. Biolek was chosen among three published memristor SPICE models. The selection was made based on the performance analysis. Furthermore, simulation of 2x2 cell ReRAM was executed in order to prove the functionality of the design. The designed ReRAM model functioned as desired based on the simulation results. In addition, the defective behaviors of the faulty ReRAM that were impacted by the three types of bridge defects, (bridge between wordlines; BW, bridge between bitlines; BB and bridge between bitlines and wordlines; BBW) had been studied in this work. The faulty ReRAM model was established by injecting the defects into the designed electrical ReRAM model. As this ReRAM employed a non-CMOS device as its memory cells, the defect that occurred might behave differently than that happens in conventional memories. This could cause the faulty ReRAM to escape from the available memory test. The simulation of the faulty ReRAM model showed that the bridge defects had been due to the Undefined State Faults (USFs) during reading operation. Besides, any faulty in ReRAM caused by USF makes setting the cell to the desired logical value a challenging task, and this fault is difficult to be detected. Hence, a new Design-for-Testability (DfT) technique was proposed to detect these USFs. This technique, known as Adaptive Sensing Read Voltage (ASRV), had been developed based on the mechanism of memristor, as well as the function of sense amplifier. Apart from that, a slight circuit modification was done to implement the DfT circuitry. Based on the simulation results during the DfT implementation, the proposed DfT technique successfully detects the USFs that occurred when $0\Omega \leq R_{BW} \leq 50\Omega$ for BW injection, $36\Omega \leq R_{BB} \leq 372\Omega$ for BB injection and $140\Omega \leq R_{BBW} \leq 210\Omega$ for BBW injection. However, this DfT technique might not suitable for BBW injection as it might kill the healthy cell.

ABSTRAK

Memori rintangan Random Access (ReRAM) adalah salah satu calon potensi memori semikonduktor baru yang muncul untuk menggantikan teknologi memori konvensional. ReRAM menawarkan banyak kelebihan menarik seperti tidak meruap, boleh skala, penggunaan tenaga yang rendah, dan akses data yang cepat. Oleh kerana memori baru ini masih di peringkat awal, ReRAM ini mempunyai kecacatan jambatan yang boleh memyebabkannya terlepas daripada ujian dan masalah kebolehpercayaan. Disebabkan oleh kekurangan model elektrik untuk ReRAM, kajian ini membentangkan model ReRAM elektrik yang direka menggunakan perisian SILVACO Elektronik Design Automation (EDA). Semua unsur-unsur ReRAM direka menggunakan transistor 22nm Oksida Logam Pelengkap Semiconductor transistor dan peranti baru yang bukan CMOS dikenali sebagai memristor pelbagai sel memori. Optimum model memristor yang dicadangkan oleh D. Biolek dipilih daripada tiga memristor model SPICE yang telah diterbitkan. Pemilihan dibuat berdasarkan analisis prestasi. Simulasi sel 2x2 ReRAM dilaksanakan untuk membuktikan fungsi rekabentuk. Model ReRAM yang direka berfungsi seperti yang dikehendaki berdasarkan keputusan simulasi. Tingkah laku yang cacat bagi ReRAM cacat yang terkesan oleh tiga jenis kecacatan jambatan (jambatan antara wordlines; BW, jambatan antara bitline; BB, dan jambatan antara bitlines dan wordlines; BBW) dikaji dalam kerja-kerja ini. Model ReRAM cacat ditubuhkan dengan menyuntik kecacatan dalam model ReRAM elektrik yang direka. Memandangkan ReRAM ini menggunakan alat bukan CMOS sebagai sel-sel ingatan, kecacatan yang berlaku mungkin berkelakuan berbeza daripada yang berlaku dalam memori konvensional. Ini boleh menyebabkan terlepasnya ReRAM cacat dari ujian memori yang tersedia. Simulasi untuk model ReRAM yang cacat menunjukkan bahawa kecacatan jambatan menyebabkan timbulnya Kerosakan Keadaan Tidak Ditakrif (USFs) semasa operasi dibaca. USFs akan menyebabkan sel ReRAM yang cacat sukar untuk ditetapkan kepada nilai logik yang dikehendaki dan kerosakan ini adalah sukar untuk dikesan. Oleh itu, rekabentuk untuk kebolehujian teknik (DfT) yang baru dicadangkan untuk mengesan USFs ini. Teknik ini dinamakan sebagai Penyesuaian Penderiaan Bacaan Voltan (ASRV) yang dibangunkan berdasarkan mekanisme memristor dan fungsi pengesan penguat. Sedikit pengubahsuaian litar dilakukan untuk melaksanakan litar DfT. Berdasarkan keputusan simulasi semasa pelaksanaan DfT, teknik DfT yang dicadangkan berjaya mengesan USFs apabila $0\Omega \leq R_{BW} \leq 50\Omega$ untuk suntikan BW, $36\Omega \leq R_{BB} \leq 372\Omega$ untuk suntikan BB dan $140\Omega \leq R_{BBW} \leq 210\Omega$ untuk suntikan BBW. Walau bagaimanapun, teknik DfT ini mungkin tidak sesuai untuk suntikan BBW kerana ia mungkin membunuh sel yang sihat.

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LIST OF ABBREVIATIONS

RAM	-	Random Access Memory
ReRAM	-	Resistive Random Access Memory
CMOS	-	Complementary Metal-Oxide Semiconductor
GND	-	Ground
DfT	-	Design-for-Testability
EDA	-	Electronic Design Automation
USFs	-	Undefined State Faults
SAF	-	Stuck-at-Faults
BL	-	Bitlines
WL	-	Wordlines
NBL	-	Nano bitlines
NWL	-	Nano wordlines
W/R	-	Write/read
w1	-	Write 1 operation
w0	-	Write 0 operation
r1	-	Read 1 operation
r0	-	Read 0 operation
SA	-	Sense Amplifier
OC	-	Open in cell
OW	-	Open in wordlines
OB	-	Open in bitlines
BB	-	Bridge between NBLs
BW	-	Bridge between NWLs
BBW	-	Bridge between NBLs and NWLs
ASRV	-	Adaptive Sensing Read Voltage
LWV	-	Low Write Voltage

LIST OF PUBLICATIONS

1. Arshad, N., Salehuddin, F., Salim, S. I. and Soin, N., 2015. Defect-oriented Test and Design-for-Testability Technique for Resistive Random Access Memory. *Journal of Telecommunication, Electronic and Computer Engineering (JTEC)*, will be published in vol 8. *(Scopus)*
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CHAPTER 1

INTRODUCTION

1.1 Research Background

Nowadays, almost all electronic systems use memories for data storage. The speed of the changing technology that has led to existing of several emerging memory technologies in replacing conventional semiconductor memories, such as Static Random Access Memory (RAM), Dynamic RAM, and Flash, in future computer and embedded systems. The emerging memory technologies such as ferroelectric RAM (FRAM), magnetic RAM (MRAM), spin-torque transfer RAM (STTRAM), phase-change RAM (PCRAM), resistive RAM (ReRAM), and organic RAM (ORAM) (Chung et al. 2010).

In addition, Chung *et al*. (2010) identified that ReRAM has the densest data storage, non-volatility, and fast data access features. Compared to the conventional semiconductor memories and other emerging memory technologies, ReRAM cells can be fabricated without access transistors. Moreover, Crossbar Inc. (Anonymous, 2014) mentioned that the simple structure enables ReRAM to be integrated in crossbar arrays and stacked in multiple layers to form three-dimension (3D) memories. With such novel devices and advanced circuit architecture, ReRAM offers attractive potentials, such as an enormous storage capacity, low power consumption, and simple fabrication, for memory cell array. In fact, the academic researchers at UC Santa Barbara (Lastras-Montano *et al*., 2015), Imperial College (Vallace, 2012), and TU Delft (Zaidi, 2012) have been intensively studying this emerging memory. On top of that, semiconductor

companies, such as Hewlett-Packard (HP) at USA, Crossbar Inc. in California, Hynix in South Africa, and Interuniversity Microelectronics Centre (IMEC) in Belgium, have been expected to market ReRAM as a product in the next few years.

1.2 Problem Statement

Based on Moore's Law, the number of transistors in a chip was roughly become double per two years. As a result of this downscaling of complementary metal-oxide semiconductor (CMOS) transistor technology, Haron *et al.* (2007) mentioned that CMOS was prone to have several challenges that include physical, material, power-thermal, technological, and economic challenges. Hence, the quality and the reliability of CMOS memories were affected. Figure 1.1 displayed some problems that have been found in conventional memory technologies that have paved way to the existence of the emerging memory technologies. Besides, it cannot be denied that based on Moore's Law, conventional memories have become denser and downscaling overtime, but their quality and reliability have been affected due to the rapid changes of technology development.

Figure 1.1 also reflected the relationship between the conventional memory technology and the emerging memory technology, where the problems inherent in the conventional memory technology have led to the existence of the emerging memory technology like ReRAM. Thus, it is believed that the target memory, ReRAM, is expected to suffer from quality problems. In general, these problems arise due to the size of the components used to form the memory, which was very tiny and closely structured. At the same time, fabricating such tiny and dense structure requires very precise and mature fabrication techniques. Furthermore, the fundamental operation and the types of memristors used as ReRAM cells have not been fully understood and are

still debatable. Moreover, in the perspective of quality improvement of ReRAM, very limited work has been published so far. Apart from that, understanding the faulty behavior of the memory devices in the presence of defects enables the development of appropriate faulty models and efficient test schemes; thus, improve the quality of outgoing product.

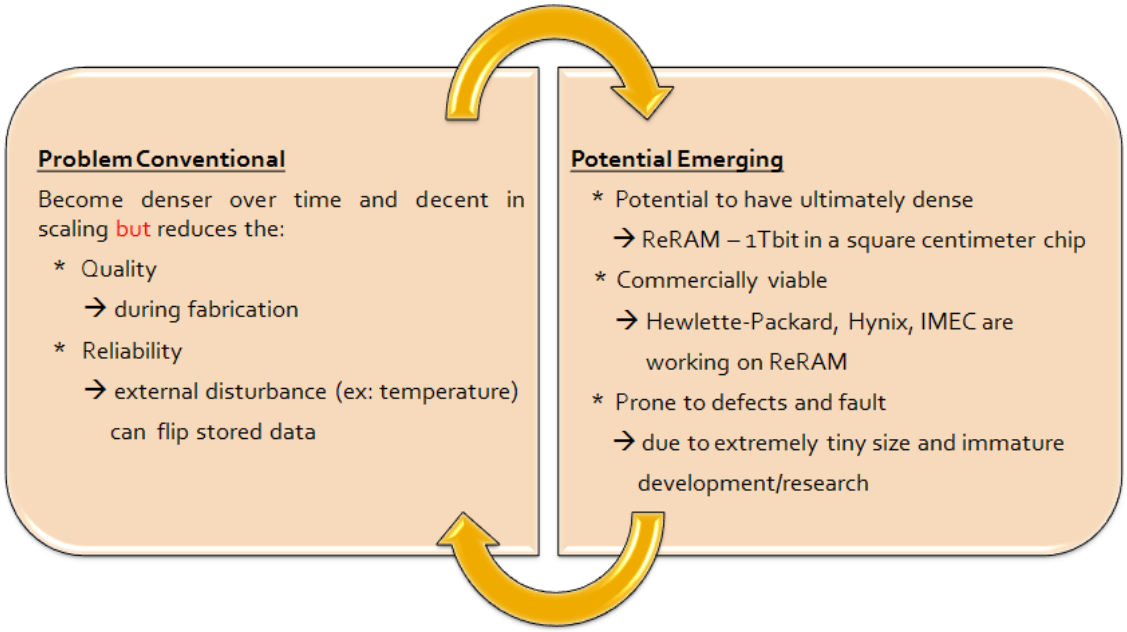

Figure 1.1: Problems in conventional and potential in emerging memories.

Furthermore, it has been proven by Hamdioui (2001) that fast analysis of quality improvement can be eased by using electrical model. However, ReRAM electrical models are still not reliable as this memory technology is still in infancy stage. Therefore, developing an electrical model for ReRAM had been necessary in this research. This model serves as the starting points for faulty ReRAM electrical model development and quality testing for bridge defect development.

In addition, previous work published by Haron *et al.* (2011) revealed that when ReRAM cells were impacted by resistive open defects (due to insufficient dopant), the

write operation might fail. For example, writing logic 1 to an impacted ReRAM cell that stores logic 0 will set the cell to an undefined state; when a read operation is performed to this faulty cell, an arbitrary logic output will be returned. Nevertheless, such faulty behavior is hard to be detected by the existing test schemes, which are based on either logic 1 (V_{dd}) or 0 (GND). Therefore, defective ReRAMs might escape the manufacturing test and cause computers, as well as embedded systems installed with such memories, fail to function properly.

1.3 Objectives

The main goal of this research was to propose a new design-for-Testability (DfT) technique in detecting a unique fault that could occur in faulty ReRAM cell. The following were specific objectives for this research.

i. To design an electrical model of ReRAM.

ii. To establish electrical faulty models for bridge defects between ReRAM cells.

iii. To develop DfT technique to test the bridge defects that had an impact on ReRAM cell.

1.4 Scope of Research

Several limitations of this research need to be acknowledged. This research was conducted by running simulation using a simulation tool known as SILVACO Electronic Design Automation (EDA) software. During the ReRAM modeling stage, the memristor model that was considered for this device only consisted of the memristor SPICE model. In addition, the ReRAM model that was developed had been based on

electrical level. The design of memory array for this ReRAM only involved 2x2 array. The 2x2 ReRAM array had been sufficient for this simulation as there was high potential for bridge defects to occur between two adjacent ReRAM cells.

Besides, this research had focused on testing the faulty ReRAM that was induced by bridge defect that occurred in the memory array. During simulation, the data collections for the simulation results concentrated on the values of output voltage that were measured at sense amplifier. Lastly, the most important scope in this research is the proposed DfT technique, which was developed to detect Undefined State Faults (USFs) that occur during bridge injection.

1.5 Contributions

This research is motivated by some potential characteristics and challenges in this emerging memory technology of ReRAM. Hence, it is believed that this research can improve the quality and the reliability of ReRAM. The outcomes of this research are summarized in several contributions, which are ReRAM electrical model, faulty models for bridge defect in ReRAM, and DfT technique for bridge defect in ReRAM.

1.5.1 ReRAM Electrical Model

The modeling for ReRAM electrical model had been based on the functional model of memory technology. The optimal memristor model that was published in Jurnal Teknologi publication played an important role in modelling this ReRAM. Furthermore, the simulation of defect-free ReRAM model ensured its functionality. In fact, this modeling was presented in International Conference on Internet Services Technology and Information Engineering (ISTIE 2014) and published in Advanced Science Letters publication.

1.5.2 Faulty Models for Bridge Defect in ReRAM

The development of the defect-free ReRAM model was adopted to model the faulty models. The faulty models that were comprised of bridge defect had been important for defect analysis and testing. Besides, this work was presented in the Malaysian Technical Universities Conference on Engineering and Technology (MUCET 2014).

1.5.3 DfT Technique for Bridge Defect in ReRAM

The DfT technique was introduced to detect the faulty models. The technique was developed by adopting the idea on how sense amplifier works and the concept of memristor operation. The DfT technique that namely as Adaptive Sensing Read Voltage (ASRV) technique could be applied for off-line and on-line tests at the manufacturing plant in order to improve the product quality and reliability. The proposed DfT technique was accepted for Journal of Telecommunication, Electronic, and Computer Engineering (JTEC) publication.

1.6 Thesis Organization

This thesis was organized in five chapters: introduction, literature review, methodology, results and discussion, conclusion and future work. Chapter 1 presented the introductory for understanding the research background. It provided the research background, the problem statement, the objectives, the scope of research, the methodology, and the contributions of this research.

Chapter 2 reviewed the research background of the study. Firstly, it presented a review on memory technologies for memory concept, memory technology classification, conventional memory technologies, and emerging memory technologies.