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HARMONIC REDUCTION COMPARISON IN MULTILEVEL INVERTERS FOR INDUSTRIAL APPLICATION

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ABSTRACT

This paper presents the simulation studies adapters' type of multi-level consists of H-bridge cascade imposed to reduce harmonic for high power applications. Applications of multilevel converters are able to reduce the number of harmonics contained in the system of low-voltage electrical distribution. This study deals with a comparative analysis between the three stages of imposed multilevel inverter circuits cascaded H-bridge inverter with sinusoidal pulse width modulation (SPWM) strategies. Used five to nine levels SPWM inverter with the functions of the switching of the principles of mitigation of harmonic components of the output voltage of the multilevel converters operation. The simulation results show that the total harmonic distortion of the effort (THDV) adapters for multiple outputs levels and decreased both realized on the basis of the content of the low standard IEC.
Keywords: *Multilevel inverter, H-Bridge inverter (CHB), SPWM.*

1. INTRODUCTION

Multilevel converters provide more than two voltage levels. And general topology of the multi-level inverter can achieve a balance between the level of effort in itself, regardless of the drive control and load characteristics. The concept was introduced multi-level inverters since 1975. The applications are diverse and affect a wide field of electrical engineering from a few watts to several hundred megawatts. They are devoted to medium and high-voltage for current applications. The output quality of the current and voltage of multilevel inverter can be determined by high frequency switching techniques. The semiconductor power (e.g. GTO or IGBT high caliber) usually operate at relatively low frequencies. Multilevel inverters have three topologies.

- Cascaded H-bridge (CHB)
- Diode–Clamped (NPC)
- Flying Capacitors (FC)

Cells with separated DC sources shown in figure.1. [4]. Diode-clamped multilevel inverters this method is to use a more complex converter topology, Generates the PWM signals necessary to inverter control the switching voltage is reduced to the step value of the converter. The Control structure and operation of cascaded H-bridge multilevel inverter is better than the other inverters [3]. Our job is to the implementation of technical SPWM which is to minimize the rate harmonics (THD) of the output wave [4]. The performance of the inverter, for any what control strategy related to content harmonics of its output voltage. A lot of techniques have been studied to reduce harmonics. pulse width modulation (PWM) technique gives the effect on the switching losses inverter, harmonic contents in the output waveform, and overall performance of the inverter. Sinusoidal PWM (SPWM) is an effective method to reduce lower order harmonics while varying the output voltage. In contrast, Phase Disposition (PD) modulation of a NPC is harmonically high quality due to direct harmonic energy altogether with carrier harmonic. In case of the three-phase inverter, the ratio of the fundamental component of the utmost line-to-line voltage to the direct supply voltage is 86.6%[5]. Another way of realizing is use CAS-SPWM method [6]. The topologies of multilevel inverter can be described as shown in Figure. 1. The aim of this study is to implement the carrier frequency parameter with modulation index for achieving the low harmonic distortion. The simulation was implemented by using MATLAB/SIMULINK toolbox environment. Each inverter was integrated with sinusoidal pulse width modulation (SPWM) strategies. Five-Nine (odd) levels SPWM inverter

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with switching functions were used for the operating principles [7].

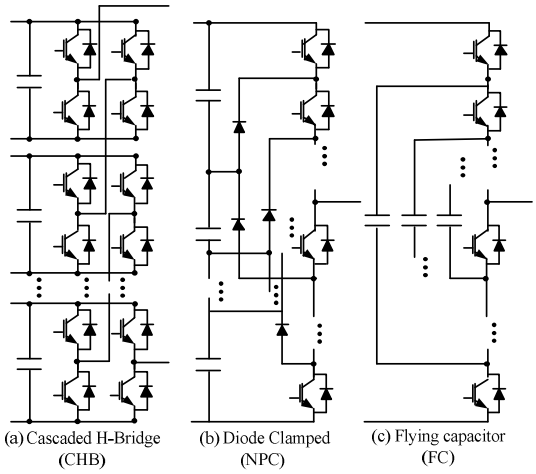

Figure 1: Topologies of Multilevel Inverter, (a) Cascaded H-Bridge (CHB), (b) Diode Clamped (NPC) (c) Flying Capacitor (FC).

2. MULTILEVEL INVERTER

The Concepts of multilevel inverters (MLI) depends not only on two voltage levels to create the AC signal. Instead, it is added to most levels of voltage to the other to create a form of reinforced smooth wave, show Figure 2, with a low dv/dt and less harmonic distortion. With more in the inverter voltage levels it creates a smoother waveform becomes, but with many levels of design becomes more complex, with more components and must be more complex controller for inverter [8].

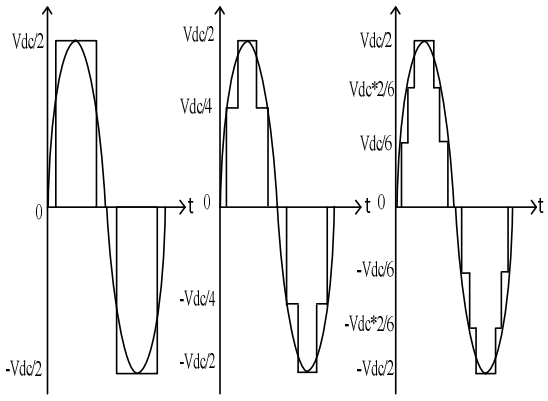

Figure 2: A three-level waveform, a five-level waveform and a seven-level multilevel.

3. PULSE WIDTH MODULATION (PWM) TECHNIQUES

In the early 1970s, the majority of PWM inverters using techniques based on the sampling method. Sinusoidal pulse width modulation of the primitive techniques, which are used to suppress the harmonics, present in a quasi-square wave. Over the years, he has developed technical PWM where the objectives were to improve performance, simplify PWM strategies and applications of microprocessors later, to produce a reduction of harmonic distortion and reduce switching losses [8]. Has been extended to several principles support levels based PWM technology as a means of controlling the active devices in a multilevel converter. PWM three techniques commonly used are- the sinusoidal PWM technology [9].

(l)- High-qualify utilization of a DC power supply that is to deliver a higher output voltage with the same DC supply.

(2)- Good linearity in voltage and/ or current control.

(3)- Low harmonic contents in the output voltage and/ or currents, especially in the low-frequency region.

(4)- Low switching losses.

3.1. Sinusoidal Pulse-Width Modulation

Control technology is the most popular method of pulse width modulation sine adapter's two traditional levels. The tem sinusoidal PWM reference is made to the production of the PWM output signal with a sine wave as a modulation signal [10]. The on and off instants of a PWM signal ill this case, can be determined by comparing the sinusoidal signal (wave modulation) with a triangular wave frequency (carrier wave), as shown in Figure 3sinusoidal PWM technology is commonly used in industrial applications and abbreviated here as SPWM [11]. Frequency of the modulating wave determines the frequency of the output voltage. The enlargement of the height of the modulation index of the waveform and determines the composition turn control the RMS value of the output voltage [12].

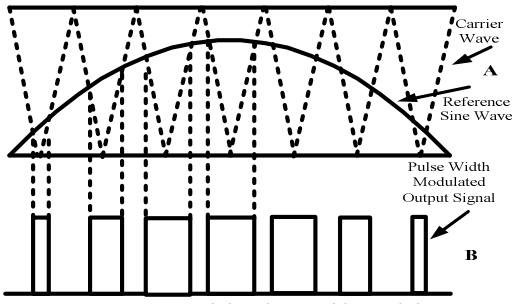

Figure 3: Sinusoidal Pulse-Width Modulations.

The RMS value of the output voltage can be varied by changing the modulation index. The output voltage of the inverter contains harmonics.

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However, to be paid for the harmonics of the band around the carrier frequency and its complications [13]. To perform sinusoidal PWM using analog circuit, use a series of bricks:

(1) High-frequency triangular wave generator.
(2) Sine wave generator.
(3) Comparator.
(4) Inverter circuits with dead-band generator to generate complimentary driving Signals with required dead band.

4. TOPOLOGIESMULTILEVELINVERTER

4.1. Cascaded H- Bridge Multilevel Inverter

A cascaded H-bridge multi-level (CHBMLI) differs in several respects from NPCMLI CCMLI in and how to achieve voltage waveform at several levels. It uses cascaded inverters H-bridge DC-separated sources in the preparation of units, create escalating waveform. In Figure 4, is the only one to get rid of the leg at five-cascaded H-bridge inverter is shown table 1 [14]. And can see the entire module H-bridge and only units that accumulate CHBMLI topology. H-bridge unit itself is CHBMLI three levels, each additional unit cascaded to be extended with two levels of voltage inverter. In Figure 4, there are two H-bridge modules to create five variation voltage levels are available. Suitable for CHBMLI applications are, for example, where the use of photovoltaic cells, battery or fuel cells. An example of what may power electric vehicles in many cells [15-16].

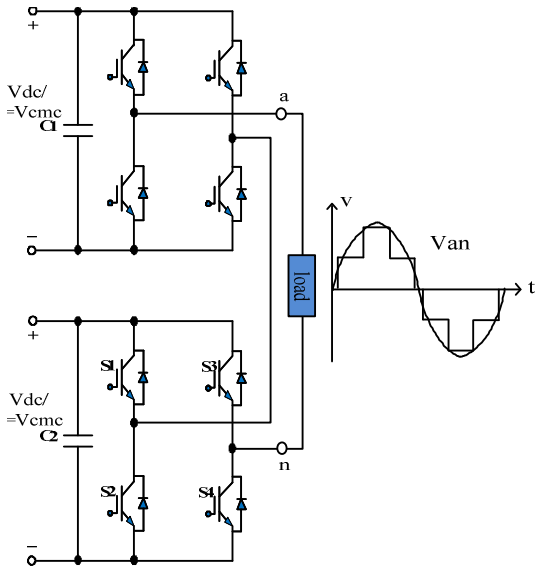

Figure 4: A five-level Cascaded Multilevel Inverter.

5. STUDY OF MUTLILEVEL INVERTER BASED ON MATLAB/ SIMULINK MODELING

This paper describes the research in the comparative study between the multi-level inverter cascading H-bridge using MATLAB/SIMULINK. It describes the layout to simulate the step-by-step procedure to build the simulation model. MATLAB /Simulink are a program five to nine level for modeling, simulation and analysis. It supports of systems, as in the time of linear time samples and non-linear, constant. For modeling, Simulink provides construction models and diagrams. Control block generates a PWM signal is given to the new level inverters for reduce total harmonic distortion can be calculated using equations (3.1, 3.2, 3.3).

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} H_{(n)}^2}}{H_2} \quad (1)$$

Where: H_1 is the amplitudes of the fundamental component, whose frequency is w0 and H_n is the amplitudes of the nth harmonics at frequency nw0

$$h_n = \frac{4E}{n\pi}\sum_{k=1}^{s}\cos(n\alpha_k) \quad (2)$$

$$h_n = \frac{4E}{n\pi}\sum_{k=1}^{s}\cos(n\alpha_k) let H_{(n)} = h_n and H_1 = h$$

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty}\left(\frac{1}{n}\sum_{k=1}^{s}\cos(n\alpha)\right)^2}}{\sum_{k=1}^{s}\cos(n\alpha_k)} \quad (3)$$

5.1. Sinusoidal Pulse Width Modulation SPWM

The generations of gating signals with sinusoidal Pulse Width Modulation SPWM are shown in Figure a. there are sinusoidal reference waves ($\upsilon_{ra}, \upsilon_{rb}$ and υ_{rc}) each shifted by 120^0. A carrier wave is compared with the reference signal corresponding to a phase to generate the gating signal for that phase. Comparing the carrier signal with the reference phase $\upsilon_{ra}, \upsilon_{rb}$ and υ_{rc} produces g_1, g_2 and g_5 respectively as shown in Figure b. the instantaneous line-to-line output voltage is $\upsilon_{ab} = Vs\left(g_1 - g_3\right)$ the output voltage as shown in Figure c, is generated by eliminating the condition that two switching

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devices in the same arm cannot conduct at the same time. The normalized carrier frequency cf should be odd multiple of three. Thus, all phase-voltage ($\upsilon_{aN}, \upsilon_{bN}$ *and* υ_{cN}) are identical, but 120^0 out of phase without even harmonics; moreover harmonics at frequency multiple of three are identical in amplitude and phase in all phase. For instance, if the ninth harmonics voltage in phase *a* is

$$\upsilon_{aN9}(t) = \upsilon \tilde{} 9\sin(9wt) \quad (4)$$

The corresponding ninth harmonics in phase *b* will be,

$$\upsilon_{aN9}(t) = \upsilon \tilde{} 9\sin(9wt - 120)) = \upsilon \tilde{} 9\sin(9wt - 1080)) = \upsilon \tilde{} 9\sin(9wt) \quad (5)$$

Thus, the ac output line voltage $\upsilon_{ab} = \upsilon_{aN} - \upsilon_{bN}$ does not contain the ninth harmonics. Therefore, for odd multiples of three times the normalized carrier frequency mf, the harmonics in the ac output voltage appear at normalized frequency fh centered around mf and its multiple, specifically, at

$$n = jmf \pm k \quad (6)$$

$$n = jmf \pm k \pm 1 \quad (7)$$

The considered a good quality of the output voltage if the modulation index (MI) in the range of 0 to 0.95. In the case of MI is greater than 0.95, there is a direct correlation between the anti-wave quality and amplitude of the output voltage if the quality decreases and then increases the output voltage wave size. SPWM technology has its limitations regarding the maximum voltage that can be achieved, and the transfer of power. In the case of a three-phase inverter, the proportion of the main ingredient to the line of maximum possible line voltage to a DC supply voltage is 86.6% and this indicates the use of poor the DC power supply. Sinusoidal (SPWM) is an effective way to reduce the lower harmonics of the system while varied output voltage. However, the low-frequency harmonic content is a minimum value.

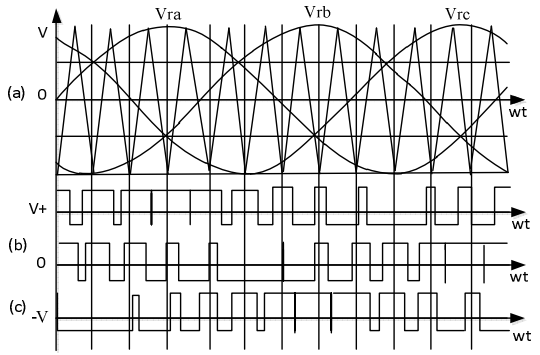

Figure 5: Sinusoidal Pulse Width Modulation for three-phase inverter.

5.2. Modeling Cascaded H-Bridge Multilevel Inverter

The simulation study has performed and carried out three-phase Multilevel inverters behavior based on a three-phase Cascaded H-Bridge Multilevel inverters were developed and its parameters as show above Table 2. The five levels that build a multilevel inverters model is exposed out in MATLAB/SIMULINK as shown in Figure 6. Moreover, the simulation diagrams for the seven and nine level similarly are shown in one block. In this simulation, the constant SPWM was used. Each block consists of 4 switches GTO in Cascaded H-Bridge (CHB) Thyristor as shown in Figure 7. The value of carrier frequency (fc) used in this designed is about 2500 Hz.

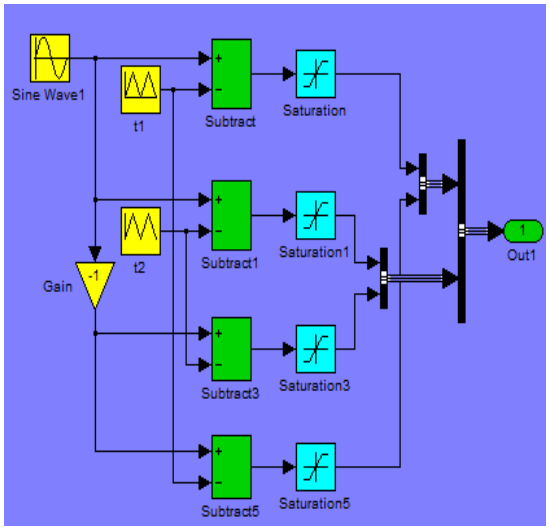

Figure 6: Simulink Five Level of control signal Cascaded H-Bridge Multilevel Inverter.

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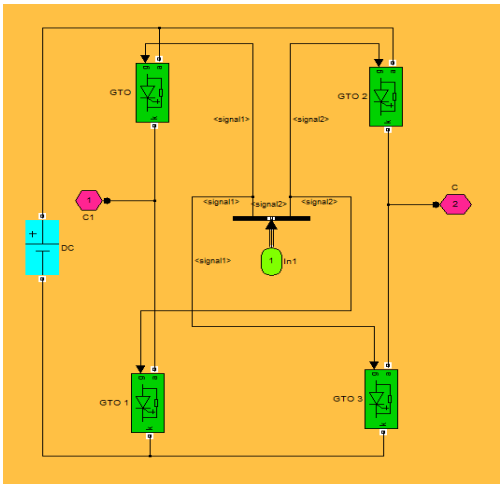

Figure 7: Switching GTO Thruster for Nine Levels Cascaded H-Bridge Multilevel Inverter.

6. HARMONIC REDUCTION BY INCREASING THE NUMBER OF VOLTAGE LEVEL IN MULTILEVEL INVERTERS

Multilevel inverters are capable of producing waveforms generated in the phases (staircase waveform); the higher the numbers of levels are included in the output voltage the more pure the waveform is which leads in alleviating the harmonic distortion at output load. On other hand, increasing the number of levels requires additional voltage sources (inverter) which leads many loads to be liable to higher levels of complexity and additional losses and additional costs.
The Fourier series of a 5-level unity DC source is shown in (9).

$$f(t) = f_{\theta 1}(t) + f_{\theta 2}(t) = \frac{2V_{dc}}{\pi}\sum_{h=1}^{\infty}[\cos(h\theta_1) + \cos(h\theta_2)] \quad (8)$$

$$= \frac{2V_{dc}}{\pi}\sum_{h=1}^{\infty}\left[\sum_{i=1}^{2}[\cos(h\theta_1)\right]\frac{\sin(hwt)}{h}] \quad (9)$$

7. SIMULATION RESULTS

In this paper will present data and result gathered from discussed in preceding chapters. In this work of multilevel inverter cascaded H-Bright (CHB) three phase based are using on sinusoidal pulse width modulation (SPWM) control inverter, a simulation module by MATLAB/SIMULINK three phase multilevel inverters, Based on the simulation results, a Five-level to Nine level (odd levels) SPWM inverter is presented to alleviate harmonic components of output voltage. Multilevel inverters are applied a GTO Thyristor inverter which is generating 50 Hz. Selected to carrier frequency 2500 Hz and modulation index equals to 0.8 and 0.95.

7.1 Cascaded H-Bridge Multilevel Inverter Results

The output voltage line to neutral (V_{L-N}) waveform of the five-level cascaded H-Bridge multilevel inverters with modulation index (MI) equals to 0.95, is in RMS value as shown in Figure 8. In contrast, the inverter output RMS voltage value is shown in Figure 9, once the Modulation Index decreased to 0.8. The number of steps for both Figures 8 & 9 are 5 (n=5) for the quarter wave and in the case of the full wave the number of steps is 10 ($2n$=10, n=5).

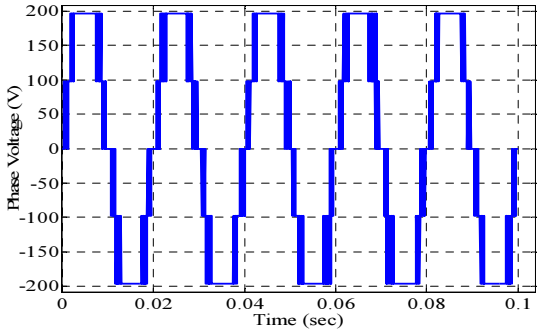

Figure 8: Phase Voltage MI=0.95.

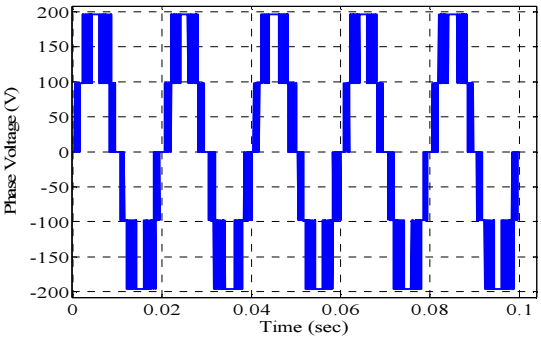

Figure 9: Phase Voltage MI=0.8.

On other hand, the simulation results for the five-level cascaded H-Bridge multilevel inverter output voltage line to line (V_{L-L}) waveform, in case of level steps numbers has increased to 10 for the quarter wave as shown in Figure 10 with modulation index (MI) equals to 0.95 and 20 steps level for the full wave with modulation index (MI) equals to 0.8 as shown in Figure 11. The output voltage produced RMS value. The number of steps level used is similar.

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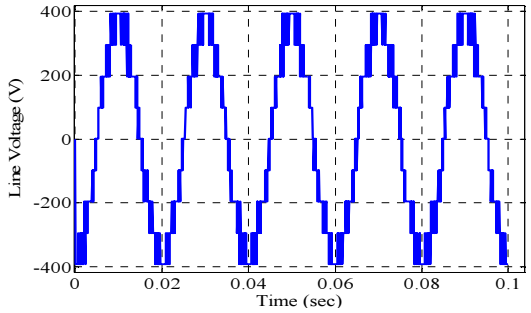

Figure 10: Line Voltage MI=0.95.

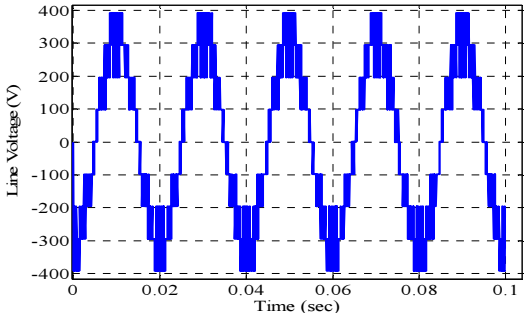

Figure 11: Line Voltage MI=0.8.

FFT analysis of the five levels cascaded H-Bridge multilevel inverter output are shown in Figure 12 & 13 continuously. The THD_V for voltage obtained of the output diode clamped multilevel inverter when modulation index equals to 0.8 is higher when the modulation index equals to 0.95.

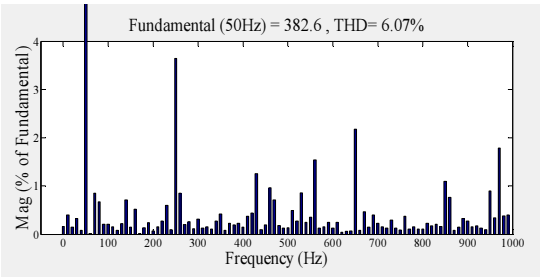

Figure 12: Harmonic Voltage MI=0.95.

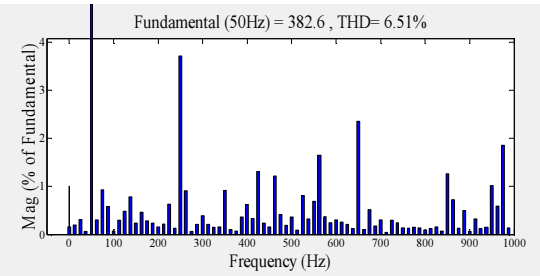

Figure 13: Harmonic Voltage MI=0.8.

Similarly, the output voltage line to neutral (V_{L-N}) waveform of the seven-level cascaded H-Bridge multilevel inverters with modulation index (MI) equals to 0.95, is in RMS value as shown in Figure 14. In contrast, the inverter output RMS voltage value is shown in Figure 15, when the Modulation Index value decreased to 0.8. The number of steps for both Figures 14 & 15 are 7 (n=7) for the quarter wave and in the case of the full wave the number of steps is 14 ($2n$=14, n=7).

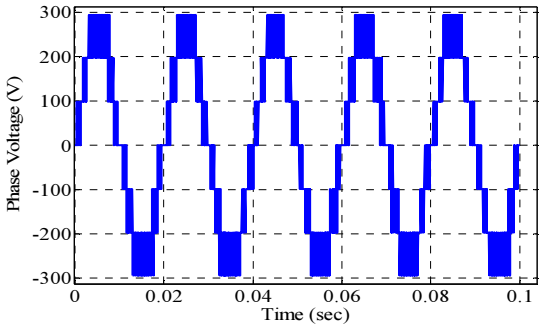

Figure 14: Phase Voltage MI=0.95.

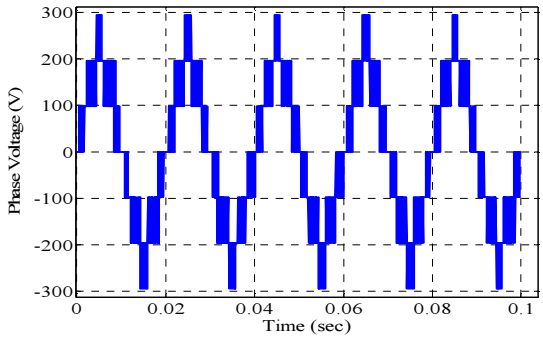

Figure 15: Phase Voltage MI=0.8.

The simulation results for the seven-level cascaded H-Bridge multilevel inverter output voltage line to line (V_{L-L}) waveform, in case of level steps numbers has increased to 14 for the quarter wave as shown in Figure 16 with modulation index (MI) equals to 0.95 and 28 steps level for the full wave with modulation index (MI) equals to 0.8 as shown in Figure 17. The output voltage produced is about 373.6 V RMS value. The number of steps level used is similar.

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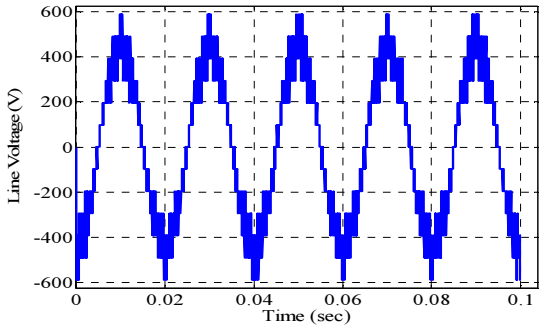

Figure 16: Line Voltage MI=0.95.

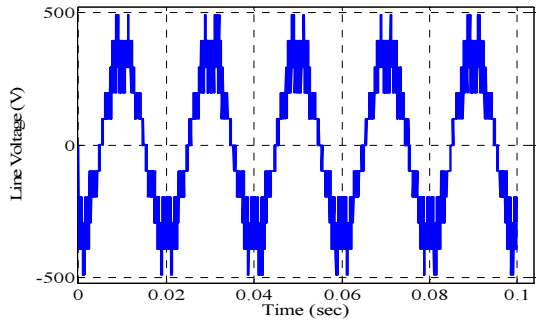

Figure 17: Line Voltage MI=0.8.

THD_V for voltage of the seven level output cascaded H-Bridge multilevel inverter has been measured when Modulation Index equal to 1and 0.8 as shown in Figure 18 & 19 respectively. It is found that the value of THD_V once the modulation index equals 0.8 is higher than once the modulation index equals to 0.95.

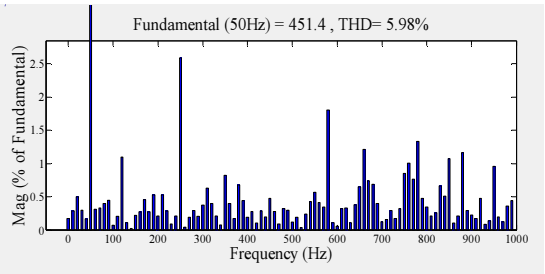

Figure 18: Harmonic Voltage MI=0.95.

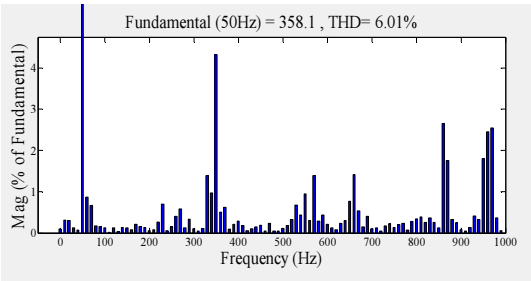

Figure 19: Harmonic Voltage MI=0.8.

Similarly, the output voltage line to neutral (V_{L-N}) waveform of the nine-level cascaded H-Bridge multilevel inverters with modulation index (MI) equals to 0.95, is in RMS value as shown in Figure 20. In contrast, the inverter output RMS voltage value is shown in Figure 21, when the Modulation Index value decreased to 0.8. The number of steps for both Figures 20 & 21 are 9 (n=9) for the quarter wave and in the case of the full wave the number of steps is 14 ($2n$=18, n=9).

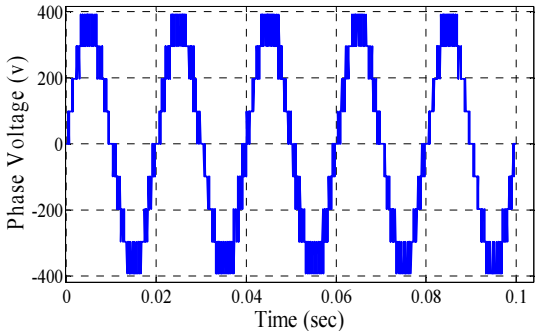

Figure 20: Phase Voltage MI=0.95.

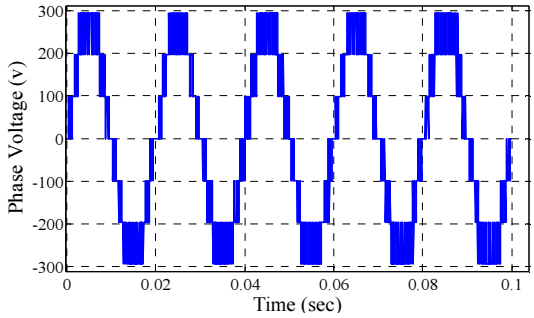

Figure 21: Phase Voltage MI=0.8.

The simulation results for the Nine-level cascaded H-Bridge multilevel inverter output voltage line to line (V_{L-L}) waveform, in case of level steps numbers has increased to 18 for the quarter wave as shown in Figure 22 with modulation index (MI) equals to 0.95 and 36 steps level for the full wave with modulation index (MI) equals to 0.8 as shown in Figure 23. The output voltage produced is in RMS value. The number of steps level used is similar.

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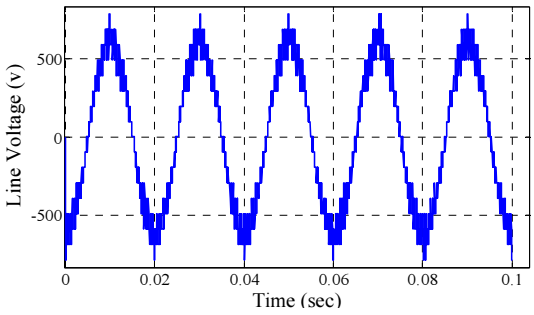

Figure 22: Line Voltage MI=0.95.

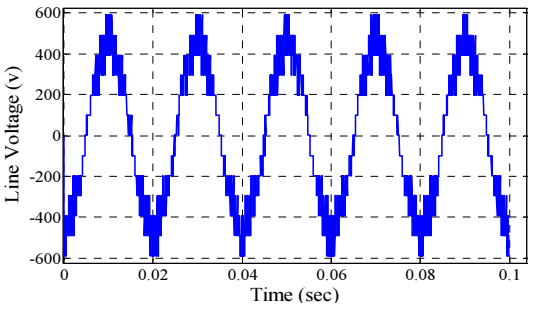

Figure 23: Line Voltage MI=0.8.

THD_V for voltage of the nine level output cascaded H-Bridge multilevel inverter has been measured when Modulation Index equal to 0.95 and 0.8 as shown in Figure 24 & 25 respectively. It is found that the value of THD_V once the modulation index equals 0.8 is higher than once the modulation index equals to 0.95.

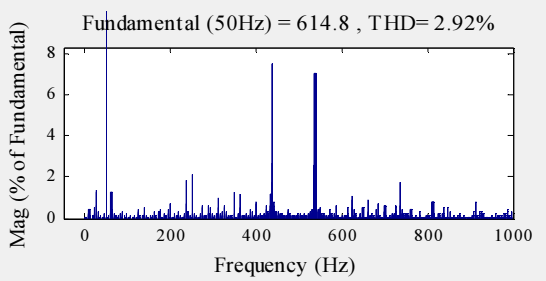

Figure 24: Harmonic Voltage MI=0.95.

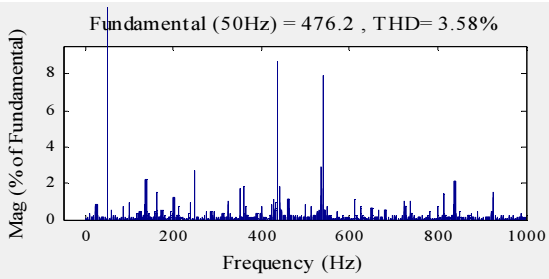

Figure 25: Harmonic Voltage M=0.8.

Table 1: COMPARISON OF FIVE TO NINE LEVELS CASCADED H-BRIDGE INVERTERS WITH DIFFERENT MODULATION INDEX (M=0.95, M=0.8).

Level(N) Index(M)		Phase Voltage RMS	Line Voltage RMS	THD
		H-Bridge	H-Bridge	H-Bridge
Five	MI= 0.95	159.6	271.9	6.07%
	MI= 0.8	144.3	246	6.51%
Seven	MI= 0.95	194.5	333.8	5.98%
	MI= 0.8	152.7	260.9	6.01%
Nine	MI= 0.95	262.2	452.8	2.92%
	MI= 0.8	202.8	349.7	3.58%

8. CONCLUSION

In these work comparative studies between five to nine levels cascaded H-bridge (CHB) multilevel inverters the choice should be based on the topology of each inverter is that the use of the inverter. Each topology has advantages and disadvantages. By increasing the number of levels, THDv will be dropped, but the cost on the other hand will be overweight as well. The cascaded H-bridge multilevel inverter topology that requires only a single DC power source. Subject to certain limitations, it has been shown that the level of effort capacitors can be controlled by choosing the angles at the same time shift to achieve the specific modulation index and the reduce of harmonics in the form of output wave.

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