Praise Worthy Prize

International Review of Automatic Control (I.RE.A.CO.), Vol. 6, N. 5
ISSN 1974-6059 September 2013

Fundamental Studies of a Three Phase Cascaded H-Bridge and Diode Clamped Multilevel Inverters Using Matlab/Simulink

Rosli Omar[1], Mohammed Rasheed[2], Marizan Sulaiman[3]

Abstract – *This paper presents a fundamental study of two type's multilevel inverters comprising of Cascaded H-Bridge and Diode Clamped for harmonic reduction for high power applications. The application of multilevel inverters is capable to minimize the number of harmonic contents in low voltage electrical distribution system. This study discusses a three phase comparative analysis between multi-level circuits diode clamped inverter and cascaded H-Bridge inverter with sinusoidal pulse width modulation (SPWM) strategies. Nine levels SPWM inverter with switching functions are used for the operating principles to alleviate harmonic components of the output voltage of multilevel inverters. Simulation results show that the Total Harmonics Distortion for voltage (THD_V) of the output for the both multilevel inverters are decreased and have been achieved lower contents based on IEC standard.*

Keywords: *Multilevel Inverter, Diode Clamped (NPC), H-Bridge Inverter (CHB), SPWM*

Nomenclature

SPWM	Sinusoidal Pulse Width Modulation
THD_V	Total Harmonics Distortion for voltage
THD	Total Harmonic Distortion
NPC	Diode Clamped Inverter
CHB	Cascaded H- Bridge Inverter

I. Introduction

The concept of multilevel inverter was introduced by Nabae in 1981, and currently it is widely used for electricity and high power distribution applications.

In multilevel inverter the output voltage and current with various levels can be generated using voltage inverters and the quality of output current and voltage of multilevel inverter can be determined by high frequency switching techniques and lower switching frequency at semiconductor and reduced harmonic content [1],[2].

Two-level inverters have disadvantages for high frequency operation because the losses of switching and device ratings constraints [3]. Multilevel inverter topologies are comprising of flying capacitors (FC), diode–clamped (NPC) and cascaded H-bridge cells with separated DC sources (CHB) [4].The main disadvantages of diode-clamped multilevel inverters with operated at complex PWM controller in order to generate the output of cascaded H-bridge multilevel inverter and its module has its own DC voltage source. The Control structure and operation of this inverter is better than the other inverters [3]. The aim of this study is to investigate the performance of two types multilevel inverters comprises of diode clamp and H-Bridge for harmonics reduction especially for industrial application.

Multilevel inverter has been presented for the formula of phase Voltage [4]. The Total Harmonic Distortion (THD) for voltage and current can be calculated by using Eqs. (1)-(3):

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} H_{(n)}^2}}{H_2} \tag{1}$$

where, H_n represents the equals of the nth harmonics at frequency nw_0 and H_1= is the equals of the fundamental component, which frequency is w_0:

$$h_n = \frac{4E}{n\pi}\sum_{k=1}^{s} cos(n\alpha_k) \tag{2}$$

$$h_n = \frac{4E}{n\pi}\sum_{k=1}^{s} cos(n\alpha_k) \text{ let } H_{(n)} = h_n \text{ and } H_1 = h$$

$$\text{let } H_{(n)} = h_n \text{ and } H_1 = h_1$$

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty}\left(\frac{1}{n}\sum_{k=1}^{s} cos(n\alpha)\right)^2}}{\sum_{k=1}^{s} cos(n\alpha_k)} \tag{3}$$

Several switching methods have been employed in static converter for reducing the output of harmonic content. Pulse width modulation (PWM) techniques have been developed for multi-level inverter so extensively in recent years.

Manuscript received and revised August 2013, accepted September 2013

More sinusoidal PWM (SPWM) techniques for inverters are advanced from the inverter on two levels.

In contrast, Phase Disposition (PD) modulation of a NPC is harmonically high quality due to direct harmonic energy altogether with carrier harmonic. It is depend on harmonic cancelation across the two phases (line-to-line voltage). Several PWM-procedures for multilevel inverters are available in [5]. In this study, we present the comparative analysis between multi-level circuits diode clamped inverter and cascaded H-Bridge inverter with (SPWM) strategies to mitigate total harmonic distortion nine (odd) levels. Another way of realizing is use CAS-SPWM method [6]. The topologies of multilevel inverter can be described as shown in Fig. 1.

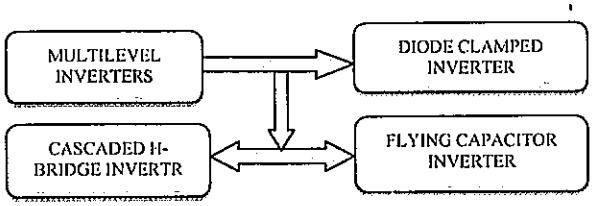


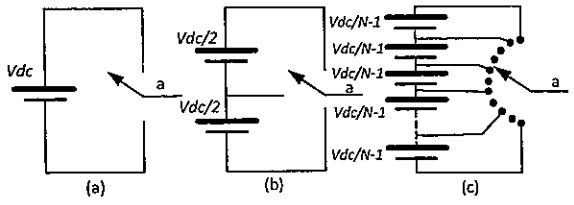
Fig. 1. Multilevel Inverter Topologies

The aim of this study is to implement the carrier frequency parameter with modulation index for achieving the low harmonic distortion. The simulation was implemented by using MATLAB/SIMULINK toolbox environment.

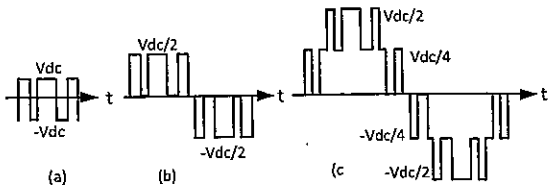
Each inverter was integrated with sinusoidal pulse width modulation (SPWM) strategies. Nine (odd) levels SPWM inverter with switching functions were used for the operating principles.

II. Multilevel Inverter

The schematic diagrams of the two-level inverter, three levels inverter, and the N-level inverter can be described in Figs. 2. All the capacitors comprises to a voltage of V_{dc}. The output voltage of a 2, 3 and N-level inverter illustrate in Figs. 3(a), (b), and (c) respectively.



Figs. 2. The inverter diagram of electronic schematic of (a) 2-levels (b) 3-levels (c) N-levels(Rodríguez et al., 2002)



Figs. 3. Output Voltage of (a) 2-levels (b) 3-levels (c) N-levels

III. Multilevel Inverter with PWM Methods

There are two basic approaches that can be used to generate the PWM signals for multilevel inverters as follows [7]:

1. *Sinusoidal or "Sub harmonic" Natural Pulse Width Modulation (SPWM).*
2. *PWM-space vector modulation which is based on rotated vector in multilevel space. It can be used to extend two-level control strategies to higher levels.*

There are several strengths in PWM inverters in comparison to square-wave inverter [8] such as: (i) it can reduce undesired harmonic voltages, (ii) it can control the output voltage, (iii) it has higher quality power factor.

By choosing suitable pulses number per half cycle, it is possible to eliminate the lowest order harmonic. On the other hand, Carrera considered several approaches for carrier bands required in multilevel PWM [9].

The techniques of the carrier PWM approaches with several variant of phase relationships for a (MLI) [10] are given as follows:

1) The carriers are in phase disposition (IPD).
2) Phase opposition disposition (POD), the carriers are in phase if these carriers are above the zero reference, but they shifted by 180^0 from those carriers if they are below the zero reference.
3) Phase Disposition (PD), each of the carriers is shifted by $2\pi/$ (N-1) radians.

III.1. Sinusoidal or "Sub harmonic" Natural Pulse Width Modulation (SPWM)

In SPWM algorithms, the quality of the output voltage is being considered good if the modulation index (MI) to be in the range of less or equal to 1.0. In case of MI is greater than 1, if the cost quality of output wave is decreased then the voltage magnitude increases. The maximum voltage Normally SPWM inverter is capable to generate maximum voltage around 79%. The maximum voltage is generated by square wave inverter.

The advantages of the inverter is the highest output voltage that can be produced from the given dc voltage of the input [7]. The effect of carrier frequency will produce a sinusoidal fundamental output and its harmonic contents are considerably high at high frequency level. However its low frequency harmonics content is minimal, the modulation approach is shown in Fig. 4.

IV. Topologies Multilevel Inverter

IV.1. Topology of Neutral Point Clamped Inverter (NPC)

The diode clamped topology is also known as neutral point clamped topology.

The main merit of the NPC topology is that it requires only one DC source similar to two-level inverter and gives better performance.

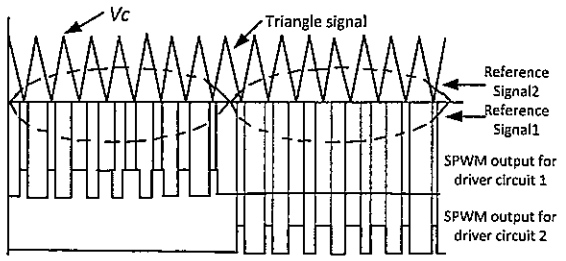


Fig. 4. Modulation techniques SPWM

However, with the increment in level n, not only the number of clamping diodes increases, but also the problem of ensuring the DC-link balance becomes more severe [11].

In Fig. 5, we show three-phases of nine-level diode-clamped inverter. The nine-level can be achieved by using 16 switches for each phase is constituted (8 switches for high leg and 8 switches for bottom leg). The three-phase shares common dc bus. The clamping diode can be used to restrict safe working level for the voltage across each capacitor.

Fig. 6 depicts the 3 line-line output voltage wave for 9-level multilevel inverters. The output voltage is a 9-level staircase wave. Therefore, the m-level diode-clamped inverter has a (2m-1)-level output voltage and an m-level output phase voltage [12].

IV.2. Topology of Cascaded H-bright Inverter (CHB)

Multilevel inverters consist of a series of connected H-bridge inverters to produce sinusoidal wave voltage.

Each cell contributes for the output voltage as summation [13]. The output has $2n+1$ number whereas the n is the cell's number.

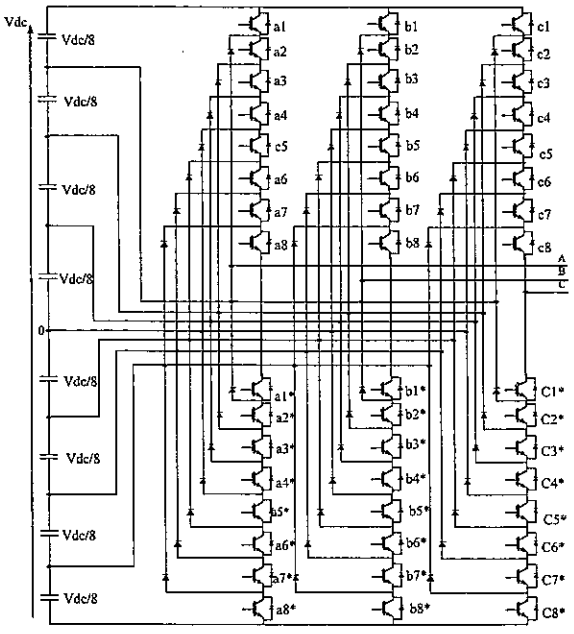


Fig. 5. Three-phase nine-level diode clamped inverter

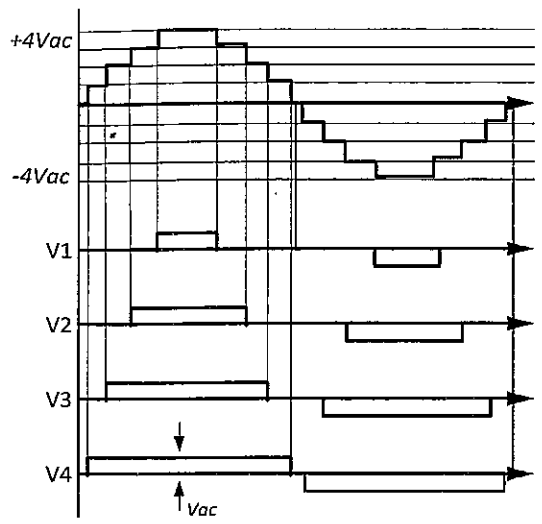


Fig. 6. Output voltage of a 9-level multilevel inverter

Total harmonic mitigation can be optimized by adjusting the switching angles [14]. In comparison to diode clamped or flying capacitor, the development of inverter is cheaper. This is because the multilevel inverters very little number of components.

The three-phase nine-level cascaded H-bridge can be seen in Fig. 7. In cascaded H-bridge, each low voltage H-bridge portion has its own DC-link voltage source. The Control structure of this inverter is better than the other inverters [7]. Similarly to previous inverters, this inverter has nine levels. This inverter includes 4 H-bridge inverters that are connected in one lag cascaded form.

The 9-level cascaded H-bridge has been built using 16 switching devices [15].

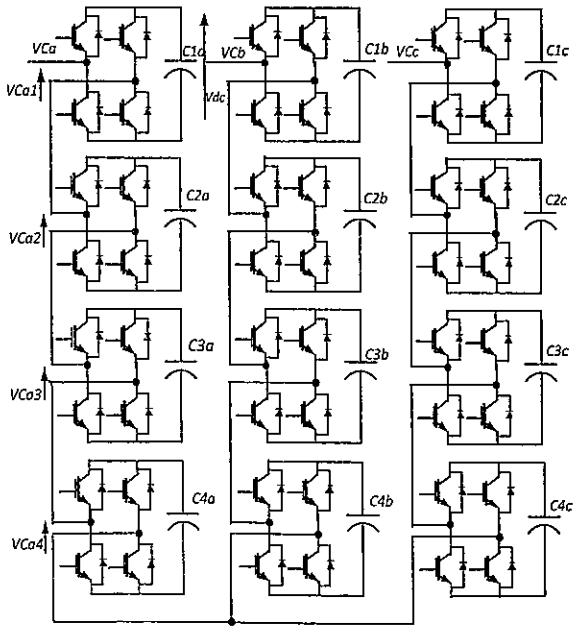


Fig. 7. Three-phase connection structure of 9-level cascade inverter

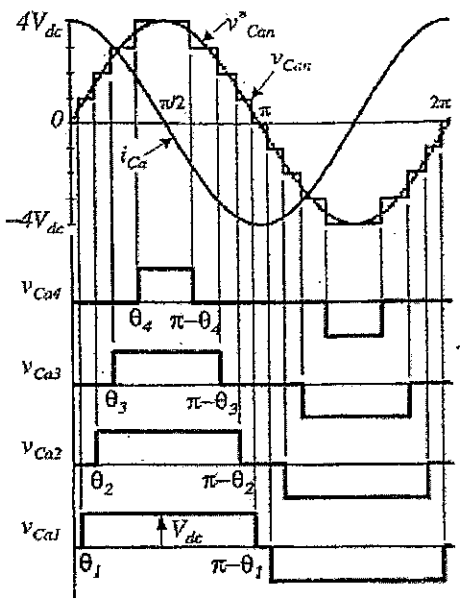


Fig. 8. Waveforms of the 9-level cascade inverter that is shown in Fig. 7

V. Simulation Results

In order to validate the performance of the proposed schemes, a simulation model for a three-phase diode clamped and Cascaded H-Bridge Multilevel inverters were developed and its parameters as shown in Table I.

Figs. 9-10 show the MATLAB/SIMULINK simulation diagrams of a three-phase diode clamped and cascaded H-Bridge multilevel inverter. In this simulation the constant SPWM was used.

In diode clamped configuration it using 8 switches GTO thruster while in Cascaded H-Bridge requires 48 switches GTO thruster.

The carrier frequency used in this designed is about 2500.

V.1. Diode Clamped Multilevel Inverter Results

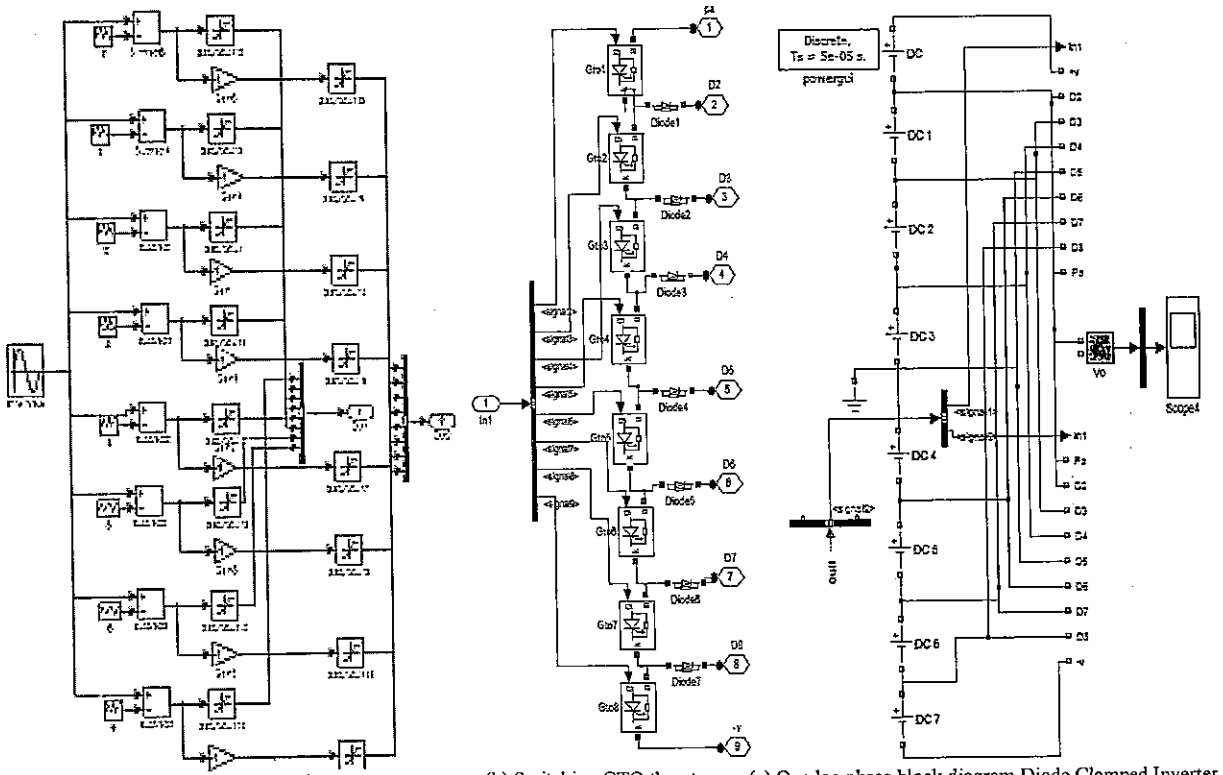
The simulation result shows in Fig. 11. The 9-level diode clamped multilevel inverter output voltage waveform for line to neutral with MI is equal to 1, Output voltage 315.5 V rms value.

When the MI decreased to 0.8 as shown in Fig.12, the inverter output voltage equal to 285.4 V rms value.

The number of steps for both figures are 9 (n=9) for the quarter wave and in the case of the full wave the number of steps is 18 ($2n$=18,n=9).

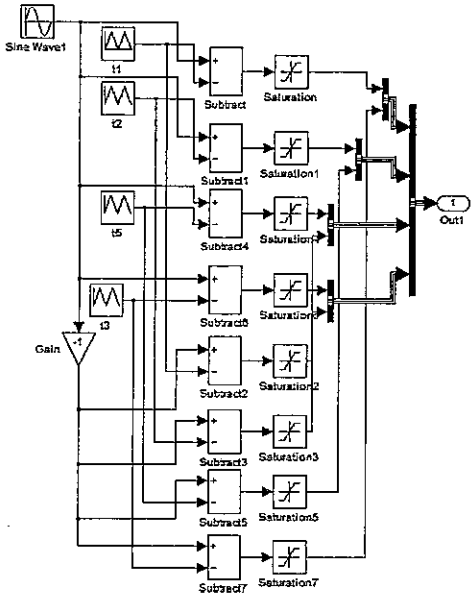
TABLE I
DIODE CLAMPED AND CASCADED H-BRIDGE PARAMETERS

Parameter	Value
Modulation Index	M =1, 0.8
DC Voltage	Vdc =100V
Output Frequency	50 Hz
Carrier Frequency	2500
GTO thruster	8 and 48 switches

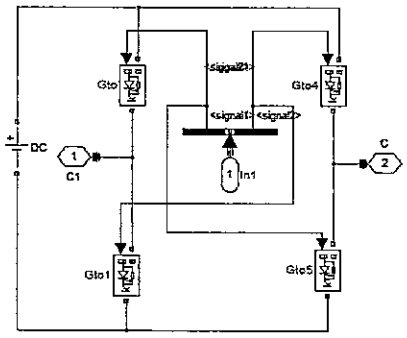


(a) Control signal SPWM (b) Switching GTO thruster (c) One lag phase block diagram Diode Clamped Inverter

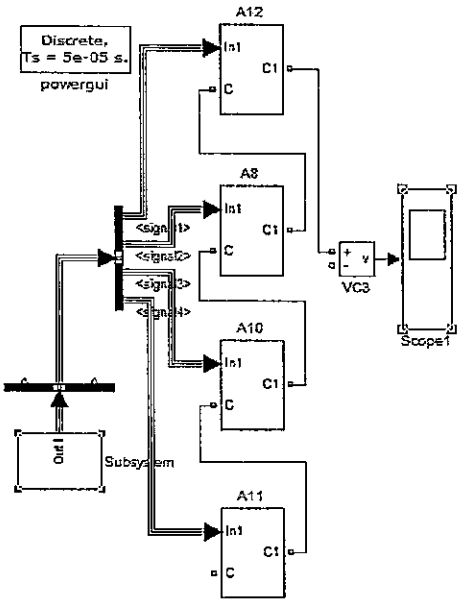
Figs. 9. Block diagram for Diode Clamped



(a) Control signal SPWM



(b) Switching GTO thruster



(c) One lag phase block diagram Diode Clamped Inverter

Figs. 10. Block diagram for Cascade H-Bridge

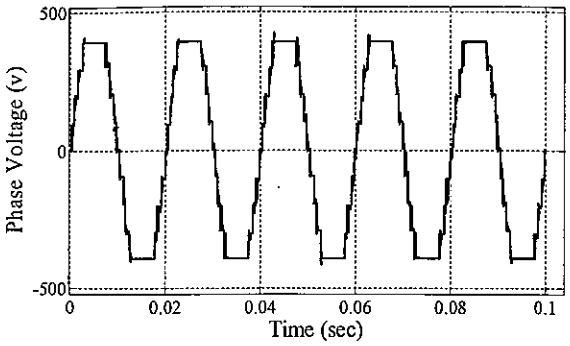


Fig. 11. Phase Voltage MI=1

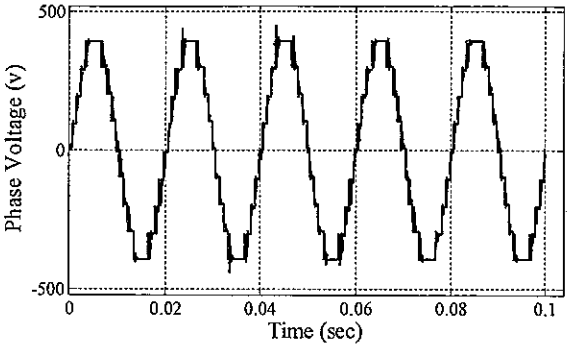


Fig. 12. Phase Voltage MI=0.8

The simulation result are shown in Fig. 13 for the 9-level diode clamped multilevel inverter output voltage waveform for line to line in case of number of steps level has increased to 18 for the quarter wave and 36 steps level for the full wave with MI = 1.

The output voltage produced is about 542.7 V rms value. When MI decreased to 0.8 the output voltage value is equal to 492.9 V rms as shown in Fig. 14. The number of steps level used is similar as in Fig. 13.

THD_V for voltage of the output diode clamped multilevel inverter has been measured when MI=1. It is found that the value of THD_v for voltage is around 3.9% as shown in Fig. 15. FFT analysis is shown in Fig. 16 that is the Diode clamped multilevel inverter output. The THD_v for voltage obtained of the output diode clamped multilevel inverter when MI=0.8 is lower than MI=1 and its value is 3.07%.

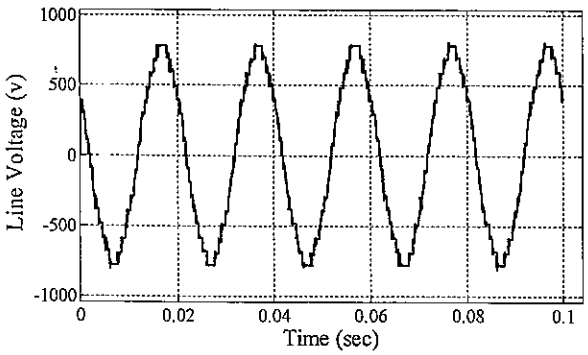


Fig. 13. Line Voltage MI=1

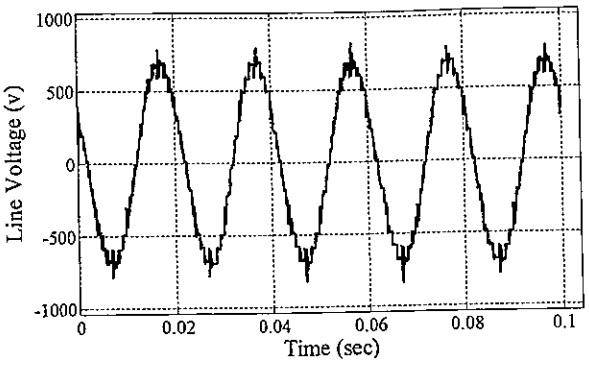


Fig. 14. Line Voltage MI=0.8

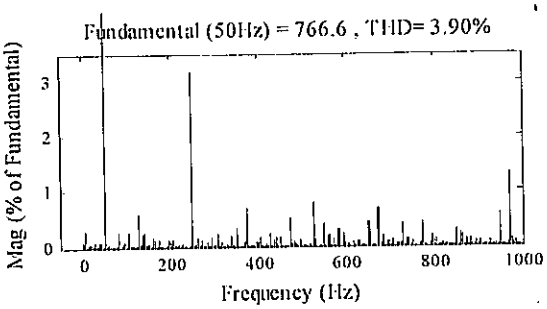


Fig. 15. Harmonic Voltage M=1

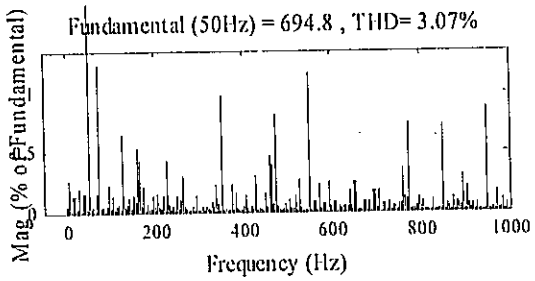


Fig. 16. Harmonic Voltage M=0.8

V.2. Cascaded H-Bridge Multilevel Inverter Results

The simulation result shows Fig. 17 that the 9-level Cascaded H-Bridge multilevel inverter output voltage waveform for line to neutral with MI is equal 1. The output voltage produced is about 262.2 V rms value.

When the MI decreased to 0.8 as shown in Fig. 18, the inverter output voltage is equal to 202.8V rms.

The number of steps for both figures are 9 (n=9) for the quarter wave and in the case of the full wave the number of steps is 18 ($2n$=18,n=9).

The simulation results are shown in Fig.19. for 9-level Cascaded H-Bridge multilevel inverter output voltage waveform for line to line in case of number of steps level has increased to 18 for the quarter wave and 36 steps level for the full wave with MI = 1. The output voltage produced is about 452.8 V rms value. When MI decreased to 0.8 the output voltage has equal to 349.7 V rms value in Fig. 20. The number of steps level used is similar as in Fig. 19.

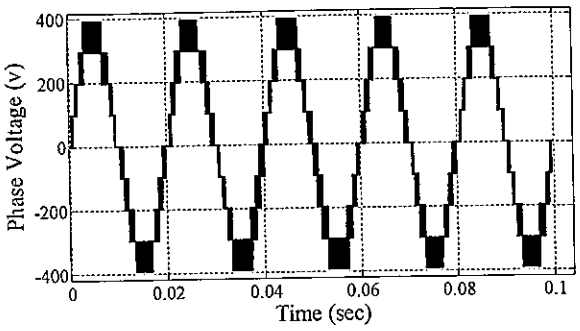


Fig. 17. Phase Voltage MI=1

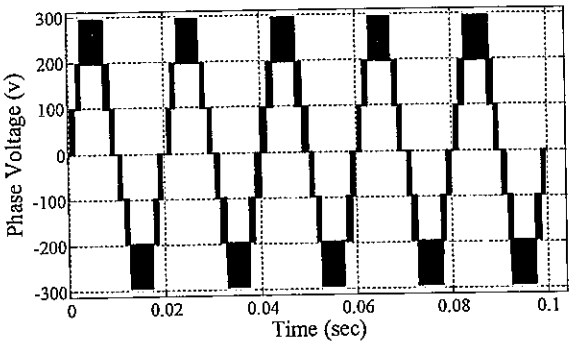


Fig. 18. Phase Voltage MI=0.8

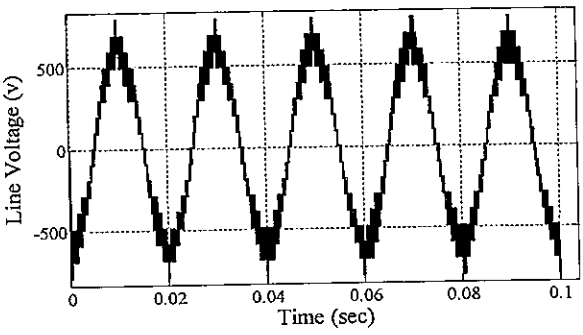


Fig. 19. Line Voltage MI=1

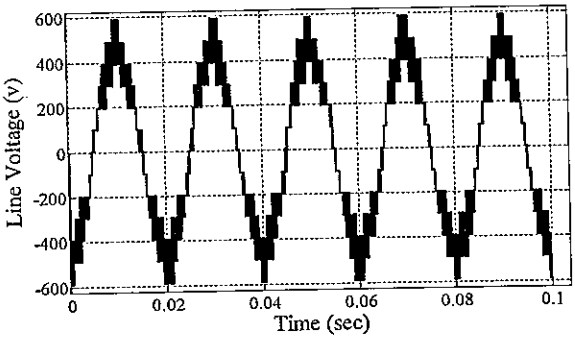


Fig. 20. Line Voltage MI=0.8

THD_V for voltage of the output Cascaded H-Bridge multilevel inverter has been measured when MI=1. It is found that the value of THD_v for voltage is around 2.92% as shown in Fig. 21. FFT analysis shows Fig. 22 that the

Cascaded H-Bridge multilevel inverter output.

The THD_v for voltage obtained of the output Cascaded H-Bridge multilevel inverter when MI=0.8 the value equal to 3.58%.

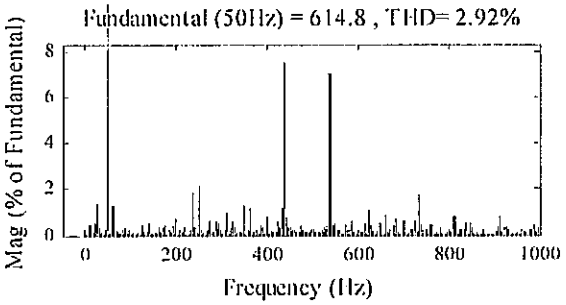


Fig. 21. Harmonic Voltage M=1

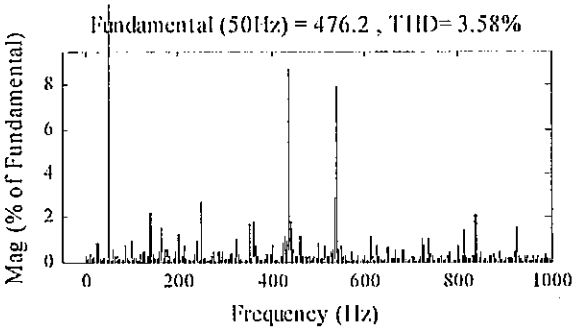


Fig. 22. Harmonic Voltage M=0.8

TABLE II
COMPARISON NINE LEVEL OF DIODE CLAMP AND CASCADED H-BRIDGE INVERTERS WITH DIFFERENT MODULATION INDEX (M=1, M=0.8)

	M	*1*	*0.8*
Phase Voltage	Diode Clamped	315.5	285.4
	Cascaded H-Bridge	262.2	202.8
Line Voltage	Diode Clamped	542.7	492.9
	Cascaded H-Bridge	452.8	349.7
THD	Diode Clamped	3.90%.	3.07%.
	Cascaded H-Bridge	2.92%	3.58%

VI. Conclusion

The fundamental study of a three-phase multi-level circuit diode clamped (NPC) and Cascaded H-Bridge (CHB) multilevel inverter has been done. The analysis of both types multilevel inverter show that the line voltage of the output diode clamped is higher than Cascaded H-Bridge due to losses available in diode clamped multilevel inverter.

However it is found that the THD_v for voltage of both multilevel inverters are capable to reduce harmonic at acceptable level based on IEC standard.

References

[1] J. Rodriguez, S. Member, and J. Lai, "Multilevel Inverters: A Survey of Topologies , Controls , and Applications," *IEEE Transactions on Industrial Electronics*, vol. 49, no. 4, pp. 724–738, 2002.

[2] Wanjekeche, T., Jimoh, A.A., Nicolae, D.V., A Novel 9-level multilevel inverter based on 3-level NPC/H-bridge topology for photovoltaic applications, (2009) *International Review of Electrical Engineering (IREE)*, 4 (5), pp. 769-777.

[3] Hosseini, S.H.; Ahmadi, M.; Zadeh, S.G., "Reducing the output harmonics of cascaded H-bridge multilevel inverter for Electric Vehicle applications," *Electrical Engineering/Electronics, Computer, Telecommunications and Information Technology (ECTI-CON), 2011 8th International Conference on* , vol., no., pp.752,755, 17-19 May 2011

[4] Farokhnia, N., Vadizadeh, H., Anvariasl, F., Line voltage THD calculation of cascaded multilevel inverter's stepped waveform with equal DC sources, (2011) *International Review of Electrical Engineering (IREE)*, 6 (3), pp. 1094-1108.

[5] D. P. Duggapu and S. Nulakajodu, "Comparison between Diode Clamped and H-Bridge Multilevel Inverter (5 to 15 odd levels)," (2012) VSRD-IJEECE, 2 (5), pp. 228–256.

[6] Gong, B., Cheng, S., Cai, K., Qin, Y., Simple three-level neutral point potential balance control scheme based on SPWM, (2012) *International Review of Electrical Engineering (IREE)*, 7 (4), pp. 4663-4671.

[7] G. Carrara, S. Gardella, M. Marchesoni, R. Salutari, and G. Sciutto, "A new multilevel PWM method: A theoretical analysis," *Power Electronics, IEEE Transactions on*, vol. 7, no. 3, pp. 497–505, 1992.

[8] L. Tolbert and T. Habetler, "Novel multilevel inverter carrier-based PWM method," *Industry Applications, IEEE*, 1999.

[9] Tolbert, L.M.; Peng, F.Z.; Habetler, T.G., "Multilevel PWM methods at low modulation indices," *Applied Power Electronics Conference and Exposition, 1999. APEC '99.* Fourteenth Annual , vol.2, no., pp.1032,1038 vol.2, 14-18 Mar 1999

[10] Urmila Bandaru, Subba D. Rayudu, Harmonic orientation of pulse width modulation in multilevel inverters, (2011) Power Engineering and Electrical Engineering, 9 (1), pp. 29–34.

[11] Aarthi, G.; Porselvi, T., "Modeling and simulation of Single Phase Matrix Converter using PWM," *Computing, Electronics and Electrical Technologies (ICCEET), 2012 International Conference on* , vol., no., pp.168,173, 21-22 March 2012.

[12] T. Prathiba, P. Renuga, A comparative study of Total Harmonic Distortion in Multi level inverter topologies, (2012) Journal of Information Engineering and Applications, 2 (3), pp. 26–37.

[13] S. Kiruthika, S. Sudarsan, M. Murugesan, and B. Jayamanikandan, High Efficiency Three Phase Nine Level Diode Clamped Multilevel Inverter, (2012) International Journal of Science and Research (IJSR), 1 (3), pp. 120–123.

[14] M. Derakhshanfar, *Analysis of different topologies of multilevel inverters*, Master of Science Thesis 2010.

[15] F. Z. Peng, J.-S. Lai, J. W. McKeever, and J. VanCoevering, A Multilevel Voltage-Source Inverter with Separate DC Sources for Static Var Generation, *IEEE Trans. Indus. Applicat.*, vol. 32, no. 5, pp. 1130-1138, Sep./Oct. 1996.

Authors' information

[1]Department of Industrial Power Engineering, Faculty of Electrical Engineering, University Technical Malaysia Melaka, Hang Tuah Jaya, 76100 Durian Tunggal, Melaka, Malaysia. Phone: +606 555 2201/2224 Fax: +606 555 2222,
E-mail: rosliomar@utem.edu.my

[2]Department of Industrial Power Engineering, Faculty of Electrical Engineering, University Technical Malaysia Melaka, Hang Tuah Jaya, 76100 Durian Tunggal, Melaka, Malaysia.
Phone: +60102694105,
E-mail: mohamed_tchno@yahoo.com

[3]Department of Industrial Power Engineering, Faculty of Electrical Engineering, University Technical Malaysia Melaka, Hang Tuah Jaya, 76100 Durian Tunggal, Melaka, Malaysia. Phone: +606 555 2209
Fax: +606 555 2222
E-mail: marizan@utem.edu.my

Rosli Omar received the degree in electrical & electronics engineering from University Technology Malaysia in 1991, M.Eng from University Of Science Malaysia in 2001 and Ph.D. in Electrical from University of Malaya in 2011.He is currently an associate professor of Faculty of Electrical Engineering, Technical University of Malaysia Melaka, Malaysia. He interests include power electronic, power quality and renewable energy.

Mohammed Rasheed was born in Bagdad, Iraq on July 1982 his degrees in Electrical Engineering from University of Electrical and Electronic Techniques, Bagdad, Iraq in 2008; He is currently working toward the M.S. degree in the department of Electrical Engineering University Technical of Malaysia Melaka Malaysia (UTEM). His research interests include Power Electronic, Multilevel Inverter.

Marizan bin Sulaiman was born in April 16, 1962 in Kuala Besut, Terengganu. Obtained his B.Sc., M.E.E. and Ph.D. in Electrical from University Of Missouri-Columbia (UMC), USA in 1984, 1985 and 1989. He is currently a professor of Faculty of Electrical Engineering, Technical University of Malaysia Melaka, Malaysia. His research interests including all area of power systems, energy efficient systems, control and instrumentation and e-learning.