Australian Journal of Basic and Applied Sciences, 8(16) October 2014, Pages: 25-33

AENSI Journals

Australian Journal of Basic and Applied Sciences

ISSN:1991-8178

Journal home page: www.ajbasweb.com

Compatibility Analysis of Silicon Nitride and Silicon Dioxide on HCI induced LDD MOSFET

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ARTICLE INFO

Article history:
Received 8 August 2014
Received in revised form
12 September 2014
Accepted 25 September 2014
Available online 1 November 2014

Keywords:
Hot-carrier-injection, HCI, LDD, MOSFET, Threshold voltage

ABSTRACT

Background: Hot-carrier-injection (HCI) is one of important reliability issue under short-channel effect in modern MOSFET devices especially in nano-scaled CMOS technology circuits. The effect of the hot carrier can be reduced by introducing Lightly-Doped-Drain (LDD) structure on the device. The objective of this project is to study the effect of hot carrier in the LDD n-MOSFET. The LDD n-MOSFET is stressed with bias voltage at intervals of stressing time to determine the degradation model in the threshold voltage and drain current. From the parametrical analysis, it shows that the shift in threshold voltage and degradation in the drain current occurred after the MOSFET device is stressed with hot carrier stress test. The rate of threshold voltage shift and degradation of the drain current are dependence to the stressing time applied to the MOSFET device. The hot carrier stress test shows that the device with Si_3N_4 has smaller voltage shift compared to SiO_2 material.

To Cite This Article: H.H.M. Yusof, N. Soin, Nissar M. K., M. Sufyan and Faiz Arith, Compatibility Analysis of Silicon Nitride and Silicon Dioxide on HCI induced LDD MOSFET. ***Aust. J. Basic & Appl. Sci.,*** *8(16): 25-33, 2014*

INTRODUCTION

Since the invention of CMOS technology, the dimensions of the electronic devices are shrinking day by day. The demand for small area and low power are the main reasons behind the miniaturization of CMOS transistor up to nano level. The higher number of transistors is required in order to produce higher performance chip at smaller packaging size (Faiz, A. *et al*.,2013) (Idzdihar, M.I. *et al*., 2012). As transistor size is shrinking, many reliability issues have been raised as critical constraints which adversely affect the performance of a system. Since the evolution of CMOS miniaturization technology, Hot Carrier Injection (HCI) has been raised as one of the critical issues. This problem occur due to the aggressive scaling of transistors in nano-scale which cause the high electrical field at drain region, therefore HCI instability takes place in the n-channel MOSFETs which leads to the degradation of device performance. Since the key factor of hot carrier generation is due to high electric field at the drain, the hot carrier effect can be minimized by reducing the electric field strength at the channel (An, H. *et al*., 2013) (Bae, J. *et al*., 2009). The purpose of reducing the electric field strength at the drain is to separate the maximum current path away from the maximum electric field. This can be done by introducing the lightly-doped-drain (LDD) structure on MOSFET devices.

The LDD structure is used to separate out the strong electric field between heavily doped drain/source and channel [5]. High *k* dielectric is necessary to reduce the leakage current but Ta_2O_5, Al_2O_3, La_2O_3, ZrO_2, HfO_2 (Yoshio, O. and P. J. Tobin, 1994) (Polishchuk, I. *et al*., 2001) (Park, D. *et al*., 1998) (Chin, A. *et al*., 2000) (Ma, Y. *et al*., 1999) (Klang, L. *et al*., 2000) and many other silicates have problems with sustainability of the device. Si_3N_4 also can be used in this study since it has higher relative dielectric constant compared to SiO_2 (Lu, Q., 1999).

Equation (1) and (2) shows that by using a material with high dielectric constant, it increases the drain current hence reduce the threshold voltage (Pomper, M. *et al*., 1982).

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$$I_{ds} = \beta \left[(V_{gs} - V_t)\, V_{ds} - \frac{V_{ds}^{2}}{2} \right] \quad (1)$$

which shows that $I_{ds} \propto \beta$ where,

$$\beta = \frac{\mu\varepsilon}{t_{ox}} \left[\frac{W}{L} \right] \quad (2)$$

It has been explained that the distribution of the lateral electric field in LDD-MOSFETs is different if compared to conventional MOSFET devices (Muhammad, M. *et al*., 2009). Silver nitride has been used as the spacer for the LDD MOSFET in the past but it causes the large degradation. It has been found that this degradation is due to the HCI effect in the side-wall spacer of LDD MOSFET (Tomohisa M. *et al*., 2010). The main objective of this paper is to study the HCI effect on sub-nanometer LDD n-MOSFET and its impact on the threshold voltage V_{TH} and drain current I_D for two oxide materials, SiO_2 and Si_3N_4.

Experimental Design:

TCAD device simulator is used to virtually fabricate the implemented device and device electrical characterizations on the hot carrier analysis. First, the device is virtually fabricated by using Silvaco ATHENA software. In order to check the electrical behavior, Silvaco ATLAS software is used to characterize the basic electrical information such as threshold voltage and drain current of the structural created by ATHENA. Besides that, the hot carrier stress test is also done by using this software where the device is stressed with stressing condition to obtain the electrical parameter degradation due to hot carrier effect. By using this software, all the aspect of device simulation can be characterized not only for CMOS technology but with wide range of integrated circuit design application (Muzalifah, M. S. *et al*., 2013). Geometrical dimensions and process parameters of the device are shown in Table 1.

The substrate of LDD n-MOSFET was developed by starting with initial silicon in 2D <100> orientation and boron impurities. The gate oxide was growth by depositing the oxide with specified thickness of 2 nm. Threshold voltage was then implanted by depositing boron and poly-silicon gate is deposited on oxide. LDD structure having light doping concentration was implanted with phosphorus at concentration of 4 x 10^{13} cm^{-3}. To secure the LDD area before doing the source/drain channel high doped implant, spacer oxide sidewall was created. At this point, the source/drain can now be implanted with arsenic having high dose of 2 x 10^{16} cm^{-3}. Oxide layer is still remaining on the structure at this point. Aluminium needs to be deposited as a contact for source and drain. The oxide layer needs to be etched first before depositing the aluminium layer. Fig. 1 shows the cross section of full structure of LDD n-MOSFET in which the parameters and dimensions have been taken from Table 1.

Table 1: Process parameters of the device

Geometrical Dimension	Process Parameter	Material / Impurities	Value
Device Length		-	1.2 µm
Device Height		-	0.7 µm
Gate Length		Polysilicon	90 nm
Gate Width		Polysilicon	1.2 µm
	Oxide Thickness	SiO_2	2 nm, 2.5 nm, 5.9 nm
	Spacer	SiO_2	72 nm
	Substrate	Boron	7.51 x 10^{17} cm^{-3}
	Threshold Voltage Implant	Boron	9.5 x 10^{9} cm^{-3}
Lightly-Doped Area		Phosphorus	4 x 10^{13} cm^{-3}
	Source/Drain	Arsenic	2 x 10^{16} cm^{-3}

The LDD n-MOSFET structure was loaded into the simulation file followed by the simulation model. The characterization was first done based on the default structure at default bias condition without stressing time. This purposely is to make the comparison in the graph between non-stressed behaviour and stressed behaviour. After non-stressed characteristic was done, the device is now stressed at bias condition at interval period. These stress conditions were based on the default temperature condition which is at 300 K. Table 2 shows the stressed biased conditions for the simulation (Chen, C. *et al*, 2001).

The I_D versus V_{GS} curves were plotted for different oxide. The shift in threshold voltage and degradation on drain current can be observed. In order to further the degradation study, the characterizations were also performed on the various process parameters to see the effect of the process parameters in the threshold voltage and drain current degradation. The process parameter which involved in this characterization was on different gate insulator such as SiO_2 and Si_3N_4 and different substrate doping concentration.

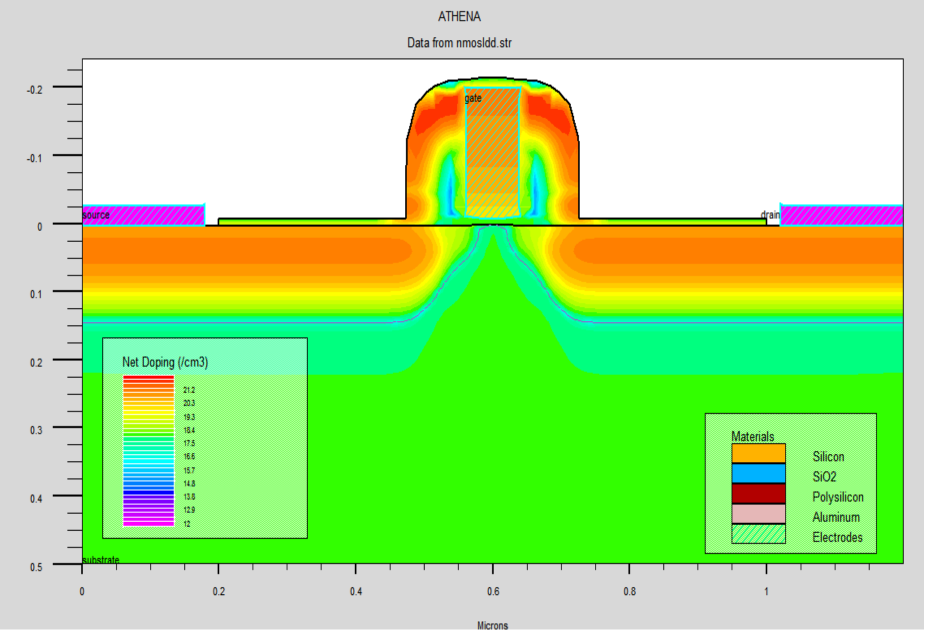

Fig. 1: Full LDD n-MOSFET structure

Table 2: Stressed biased conditions

Stress Condition	Value
Gate Voltage	0.2553 V
Drain Voltage	2.5 V
Time	10 s, 30 s, 100 s, 300 s, 1000 s
Temperature	300K

RESULTS AND DISCUSSION

Comparison of Threshold Voltage between Si_3N_4 and SiO_2:

Fig. 2 shows the I_D versus V_G curves for Si_3N_4 and SiO_2 across the oxide thickness of 2 nm, 2.5 nm and 5.9 nm. The graph shows that Si_3N_4 the material has lower threshold voltage compared to SiO_2 across all the oxide thickness. From the result, the higher dielectric constant produced lower threshold voltage. It is also shows that the thicker the dielectric the higher the threshold voltage level.

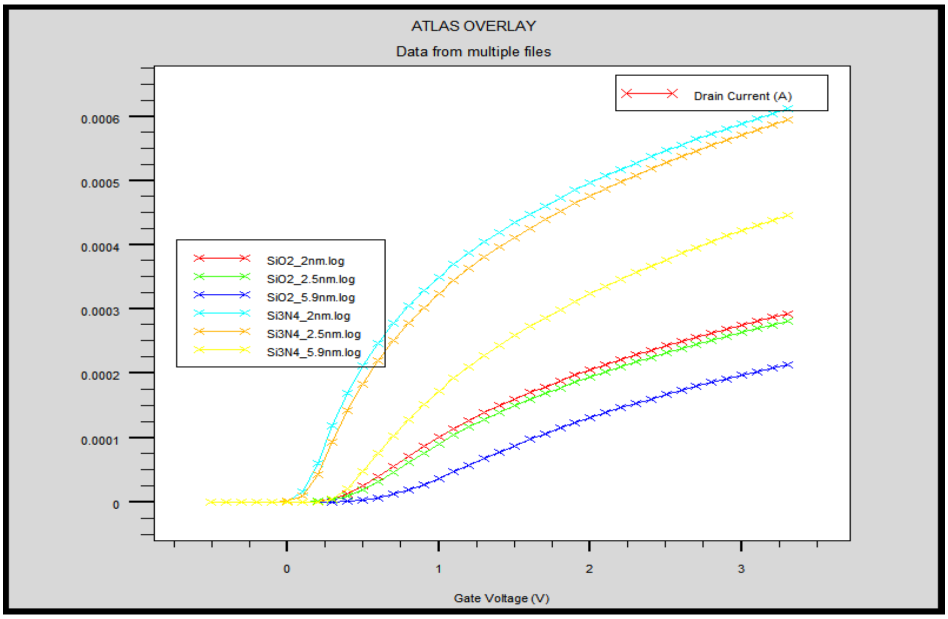

Fig. 2: *I_D versus V_G* - Comparison between SiO_2 and Si_3N_4 dielectric material across thickness.

From the data in Fig. 3 and Table 3, the percentage of the threshold voltage different between SiO_2 and $S_{i3}N_4$ is 76% for 2 nm, 77% for 2.5 nm and 54% for 5.9 nm thickness of oxide. This is shows that the higher the dielectric constant the lower the threshold voltage.

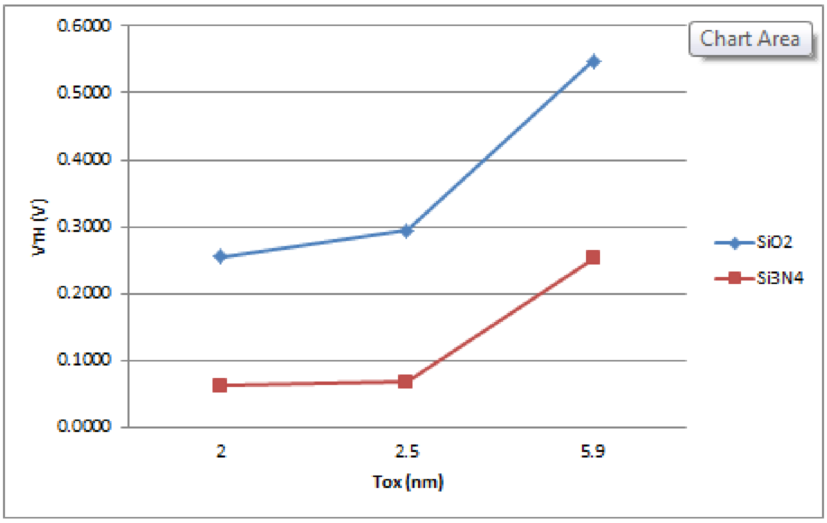

Fig. 3: V_{TH} versus t_{ox} - Comparison between SiO_2 and Si_3N_4 dielectric material across thickness.

Table 3: Comparison on threshold voltage between SiO_2 and Si_3N_4 dielectric material across thickness.

Tox (nm)	V_{TH} (V) S_iO_2	V_{TH} (V) $S_{i3}N_4$	ΔV_{TH} (V)	ΔV_{TH} (%)
2	0.2553	0.0625	0.1928	76%
2.5	0.2939	0.0688	0.2251	77%
5.9	0.5478	0.2525	0.2953	54%

Comparison of Drain Current between Si_3N_4 and SiO_2:

Fig. 4 shows the I_D versus V_D curves for Si_3N_4 and SiO_2 across the oxide thickness of 2 nm, 2.5 nm and 5.9 nm. The graph shows that the material of Si_3N_4 produced higher drain current compared to SiO_2 material. The trends are same for all the oxide thickness size. By comparing side by side, for all 2 nm, 2.5 nm and 5.9 nm thicknesses had shown the similar behavior which is reduction in drain current.

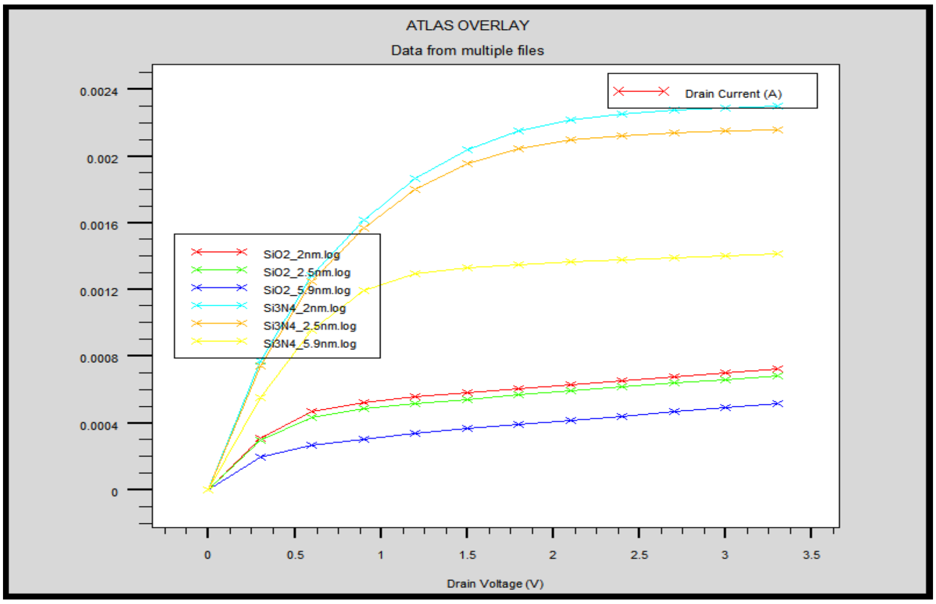

Fig. 4: I_D *versus* V_G – Comparison between SiO_2 and Si_3N_4 dielectric material across thickness.

Refer to the simulation data is shown in Fig. 5 and Table 4, percentage of reduction in drain current between SiO_2 and Si_3N_4 material for 3 different thicknesses are laid in between 175 % to 219%. At 2nm oxide thickness, the drain current value for Si_3N_4 is reduced about 219% compared to SiO_2 material. The 2.5 nm and 5.9 nm oxide thicknesses also experienced the same behaviour where the reductions of the drain current are 216% and 175% respectively.

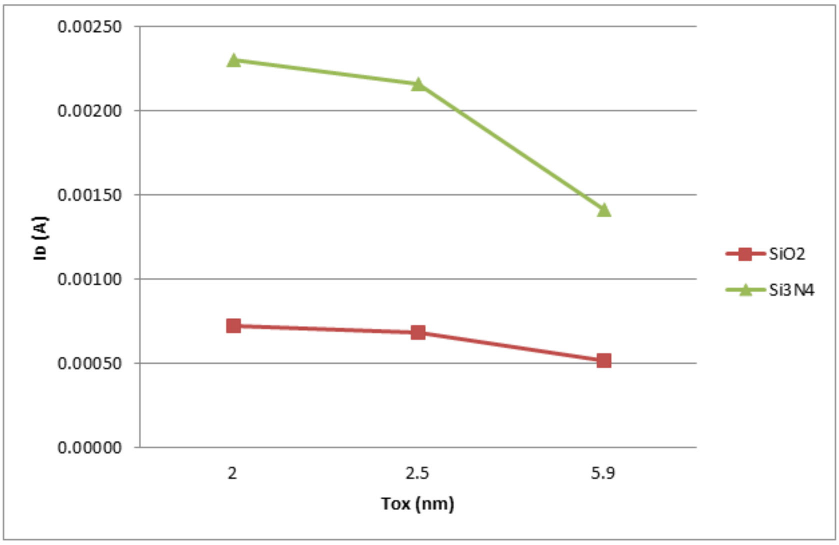

Fig. 5: *I_D versus t_{ox}* – Comparison between SiO_2 and Si_3N_4 dielectric material across thickness.

Table 4: Comparison on drain current between SiO_2 and $S_{i3}N_4$ dielectric material across thickness.

Tox (nm)	I_D (A) S_iO_2	I_D (A) $S_{i3}N_4$	ΔI_D (A)	ΔI_D (%)
2	0.00072	0.00230	0.00158	219%
2.5	0.00068	0.00216	0.00148	216%
5.9	0.00051	0.00141	0.00090	175%

Hot Carrier Injection (HCI) analysis on LDD nMOSFET:

Fig. 6 shows that the threshold voltage was shifted to right side which means in incremental value across the stressing time. The threshold voltage shift can cause a delay in operating frequency (Fakhruddin, M. *et al*., 2007).

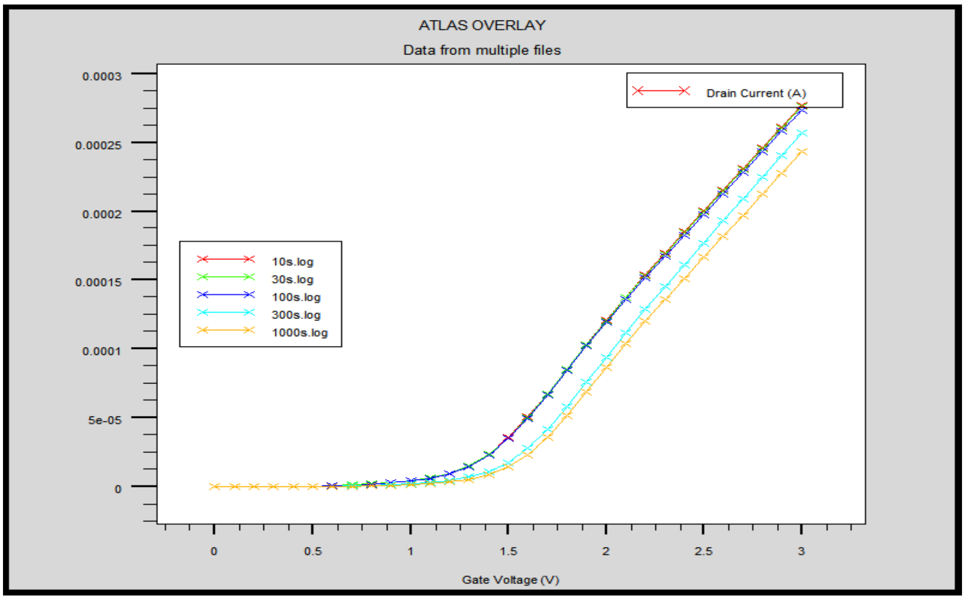

Fig. 6: *I_D versus V_G* - Threshold voltage shift across stressing time

The data shown in Fig. 7 and Table 5 representing the threshold voltage shift across the stressing time. Averagely, the threshold voltage for all the stressing time shifted about 223% to 295% from its non-stress condition. The first shift at 10 s shows high shift in threshold voltage at 223% of its original value. The subsequent shift between the stressing time were considered small with the highest shift with reference to initial condition was at 1000 s stressing time.

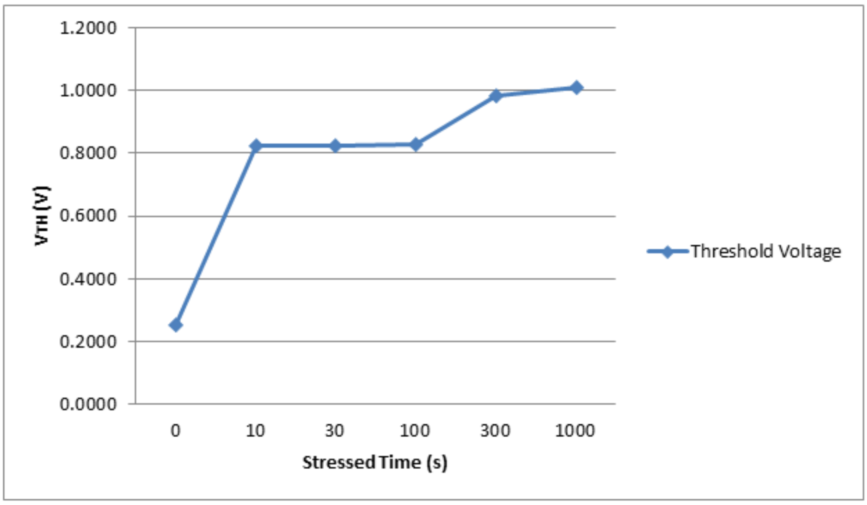

Fig. 7: V_{TH} versus stress time.

Table 5: Threshold voltage shift data.

Stress Time (s)	V_{TH} (V)	ΔV_{TH} (V)	ΔV_{TH} (%)
0	0.2553	Reference	
10	0.8250	0.5697	223%
30	0.8254	0.5701	223%
100	0.8273	0.5720	224%
300	0.9825	0.7273	285%
1000	1.0072	0.7519	295%

The drain current characteristic during hot carrier effect is shown in Fig. 8. The I_D versus V_D curve was taken at V_G = 2.2 V for all the stressing time and the curve shows the drain currents were slightly reduced at every setting of stressing time.

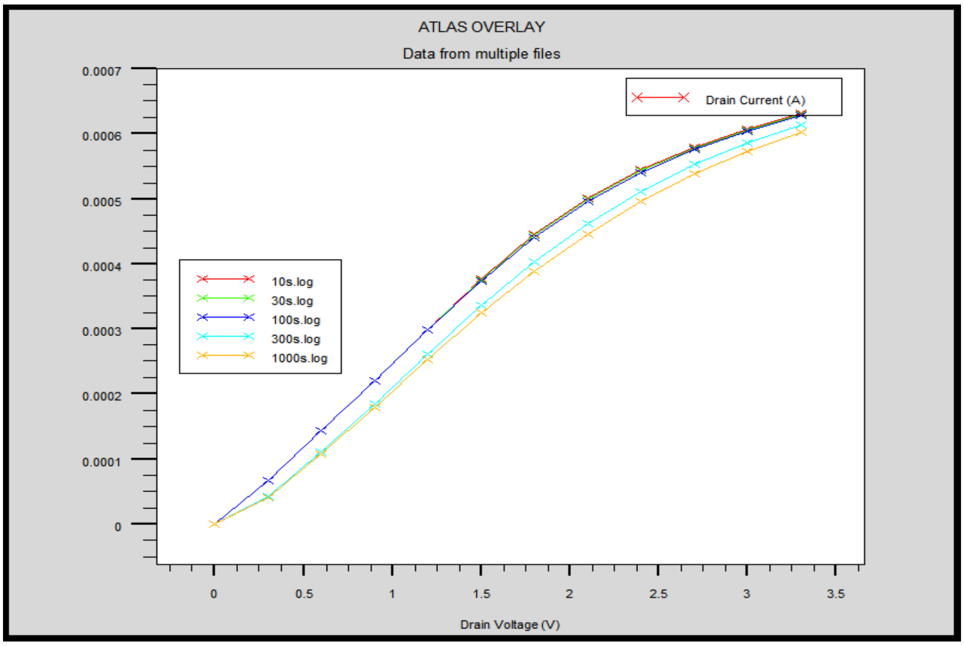

Fig. 8: I_D versus V_D – Drain current degradation.

The measurement data in the Fig. 9 and Table 6 were taken at V_D = 3.3 V. It clearly shows that the drain current is reduce along the stressing time. This is because after the device was stressed; the threshold voltage was shifted further which cause the value of threshold voltage increase.

The drain current shift about 12.55% from non-stress condition to stressed condition at 10 s. This is about 0.0906 mA reduction in drain current. The highest reduction of drain current is at 1000 s stressing time where the reduction is about 0.1207 mA or 16.72%. This proved that the relationship between the shift of threshold voltage and drain current graph. The degradation of drain current between 10 s and 1000 s is considered small.

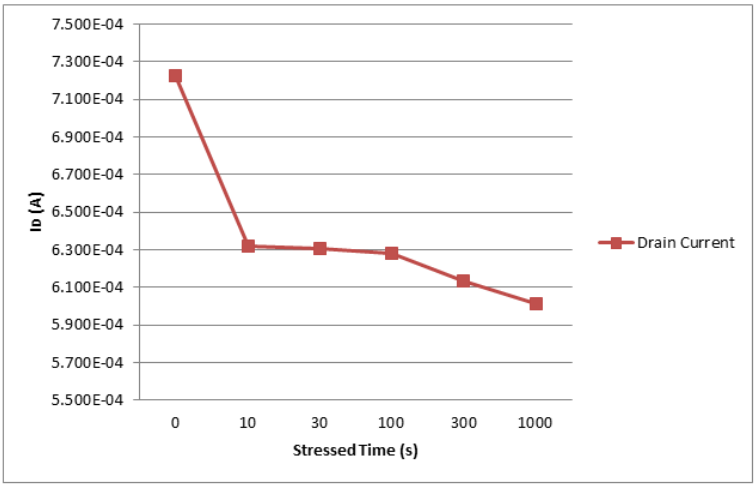

Fig. 9: I_D versus stress time.

Table 6: Drain current degradation data.

Stress Time (s)	I_D (A)	ΔI_D (A)	ΔI_D (%)
0	7.222E-04	Reference	
10	6.316E-04	9.061E-05	12.55%
30	6.308E-04	9.138E-05	12.65%
100	6.283E-04	9.388E-05	13.00%
300	6.136E-04	1.086E-04	15.04%
1000	6.015E-04	1.207E-04	16.72%

Comparison of HCI between SiO_2 and Si_3N_4 Dielectric Material:

For the comparison on hot carrier stress test between oxide materials, the materials that used are silicon dioxide, SiO_2 and silicon nitride, Si_3N_4. The comparison is purposely to see the degradation trend between these two materials. As presented before, the threshold voltage for Si_3N_4 is lower compare to SiO_2 due to high dielectric constant on Si_3N_4 material. Therefore, the value of threshold voltage for Si_3N_4 is lower in this simulation.

Fig. 10 shows the comparison graph for both materials. Material Si_3N_4 shows the shift of threshold voltage at 10 s but for the rest of stressing time it looks like similar. By looking at the result data in Table 7, the threshold voltage shift for Si_3N_4 material is very small after 10 s stress. This shows that the device with Si_3N_4 has smaller voltage shift at 10 s and more stable at longer stress time compared to SiO_2 material.

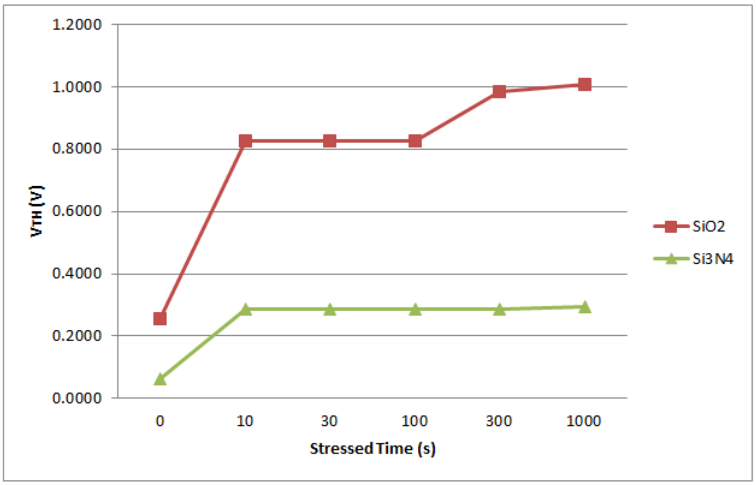

Fig. 10: V_{TH} versus stress time – Comparison between SiO_2 and $S_{i3}N_4$

Table 7: Threshold voltage shift data for SiO_2 versus Si_3N_4.

Stress Time (s)	V_{TH} (V) S_iO_2	V_{TH} (V) $S_{i3}N_4$	ΔV_{TH} (V)	ΔV_{TH} (%)
0	0.2553	0.0625	0.1928	75.52%
10	0.8250	0.2875	0.5375	65.15%
30	0.8254	0.2880	0.5374	65.10%
100	0.8273	0.2883	0.5390	65.15%
300	0.9825	0.2884	0.6941	70.64%
1000	1.0072	0.2938	0.7134	70.83%

Fig. 11 and data in Table 8 show that the drain current degradation is very small for Si_3N_4 material. This is due to the very small shift in threshold voltage for Si_3N_4 material. The shift of threshold voltage is less than 1 mV for between stressing times, therefore the drain current degradation is also very small which is less than 10 µA.

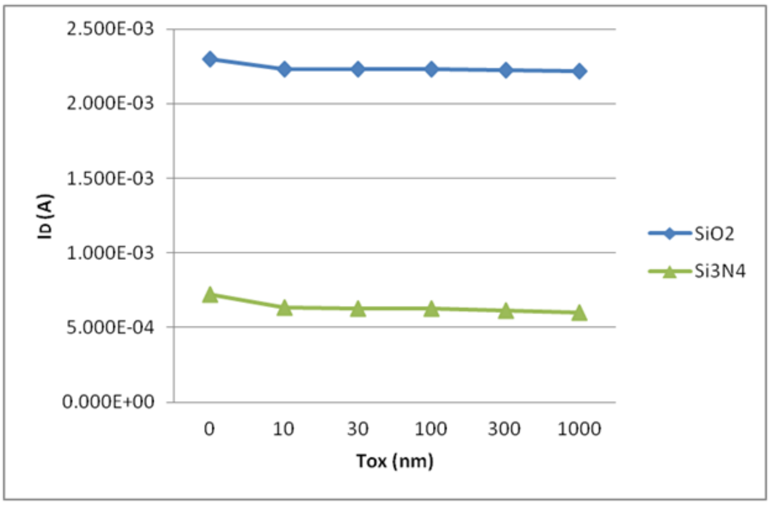

Fig. 11: I_D versus stress time – Comparison between SiO_2 and Si_3N_4

Table 8: Drain current degradation data for SiO_2 versus Si_3N_4.

Stress Time (s)	I_D (A) S_iO_2	I_D (A) $S_{i3}N_4$	ΔI_D (I)	ΔI_D (%)
0	7.222E-04	2.301E-03	1.579E-03	219%
10	6.316E-04	2.230E-03	1.598E-03	221%
30	6.308E-04	2.230E-03	1.599E-03	221%
100	6.283E-04	2.229E-03	1.601E-03	223%
300	6.136E-04	2.227E-03	1.613E-03	223%
1000	6.015E-04	2.218E-03	1.617E-03	224%

Summary:

A study of the electrical characteristics and hot carrier degradation of LDD n-MOSFET has been presented in this paper. The device electrical characteristics across the process parameter such as oxide thickness and oxide material were analyzed by determining the threshold voltage and the effect on the drain current. Si_3N_4 oxide material produced lower threshold voltage compared to SiO_2 oxide material. The higher threshold voltage produced lower drain current value vice versa. This is because of the drain current is proportional with $V_G - V_{TH}$ where the higher V_{TH} results lower value of $V_G - V_{TH}$. The hot carrier stress test was carried out on default structure. In addition, the devices with different oxide materials were also simulated with hot carrier stress test. The hot carrier stress test shows that the device with Si_3N_4 has smaller voltage shift at 10 s and more stable at longer stress time compared to SiO_2 material.

ACKNOWLEDGEMENT

This research is financially supported by the university under PJP grant scheme (No: PJP/2013/FKEKK(31B)/S01221).

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