Faculty of Manufacturing Engineering

STATISTICAL APPROACH IN SOLVING FOR INITIAL AND EVENTUAL WIRE BONDING PROBLEM

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Master of Science in Manufacturing Engineering

2013

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APPROVAL

This thesis is submitted to the Faculty of Manufacturing Engineering of Universiti Teknikal Malaysia Melaka as a partial fulfilment of the requirement for the degree of Master of Science in Manufacturing Engineering. The members of the supervisory committee are as follow:

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DECLARATION

I declare that this thesis entitled "Statistical Approach in Solving Initial and Eventual Bonding Interconnection" is the result of my own research except as cited in the references. The thesis has not been accepted for any degree and is not concurrently submitted in candidature of any other degree.

Signature : ....

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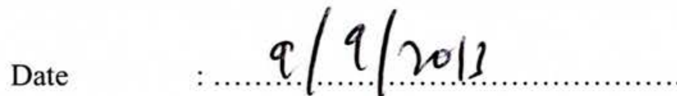

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ABSTRACT

The project scope is related to solve the real life Semiconductor industrial problem.Interconnection processis identifiedas the most critical process among others compared to overall flow in Semiconductor Packaging. In semiconductor manufacturing industries, ball bonding and wedge bonding techniques are commonly adopted in the thermo compression (T/C) and thermo sonic (T/S) processes. Approximately 95% of all semiconductor packages are produced by applying the ball bonding method, while wedge bonding is applied to produce about 5% of all assembled packages. The research study has proven the ability to have robust process with optimum probe touchdown for the initial and good wire properties selection for the eventual bonding. Two years research effort covering a complete wire bondcycle involving both Initial and Eventual bonding top defective rate. As shown in the research all the aspects have been completed to derive comprehensive conclusion in-terms of material, method with support of statistical approach, the results of this research has gain good yield performance by reducing 50% of defective rate (Please refer to published papers) satisfying respective industry.

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ABSTRAK

Skop projek ini mempunyai kaitan untuk menyelesaikan kehidupan sebenar di dalam masalah industry semikonduktor. Proses hubungkait merupakan proses yang paling kritikal dalam kalangan semua berbanding aliran keseluruhan di semikonduktor pakej. Di dalam pembuatan industry semikonduktor "ball bond" dan "wedge bond" teknik adalah proses termo mampatan dan proses termo sonic. Anggaran sebanyak 95% daripada semikonduktor pakej dihasilkan dengan menggunakan kaedah "ball bonding" sementara "wedge bonding" dihasilkan untuk menghasilkan 5% pakej. Hasil kajian "wire bonding" yang sudah disiapkan terdiri daripada kedua-dua "initial dan eventual" hubungan yang mempunyai kadar kerosakan yang tinggi. Dalam kajian ini, kesemua aspek telah lengkap untuk mendapatkan syarat-syarat kesimpulandi dalam sesuatu bahan, kaedah dan sebagainya dengan sokongan pendekatan statistik. Segala keputusan dalam hasil kajian ini akan menghasilkan sesuatu produk yang bagus dengan mengurangkan 50% kadar kerosakan dengan merujuk kepada kertas kajian yang telah diterbitkan.

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ACKNOWLEDGEMENT

First of all, I would like thank UTeM for wonderful opportunity given to pursue my MSc. Education It has given me an opportunity to solve a breakthrough industrial problem applying wonderful academic research values. While in-progress preparing this thesis, I had requested for a support from researchers, academicians and practitioners. In particular, I wish to express my sincere appreciation to my principal supervisor Associate Professor Ir. Dr. Sivarao Subramonian for encouragement, guidance critics and friendly approaches throughout the research. I am also very thankful to my co-supervisor Dr. Ahmad Kamely Mohamad for his guidance, advices and motivation. A special thanks to Miss Magret for improvement on the thesis readability. Without their continuous support and interest, this Thesis would not have been same as presented here. My fellow postgraduate students should also be recognised for their support. My sincere appreciation also extends to all my colleagues and others who have provided assistance at various occasions. Their views and tips are useful indeed. Unfortunately, it is not possible to list all of them in this limited space. I am grateful to all my family members.

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LIST OF ABBREVIATIONS

AEC	-	Automotive Engineering Council
ALD	-	Atomic Layer Deposition
ATE	-	Automated Test Equipment
BDR	-	Back End Design Rule
BPO	-	Bond Pad Opening
CMP	-	Chemical mechanical planarization
CPU	-	Central Processing Unit
CVD	-	Chemical Vapor Deposition
DA	-	Die bonding
DOE	-	Design of Experiment
ECD	-	Electrochemical Deposition
EOL	-	End of Line
FAB	-	Free Air Ball
FOL	-	Front of Line
FT	-	Final Test
HTS	-	High Temperature Storage
IC	-	Integrated Circuit

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IMC	-	Intermetallic Coverage
LF	-	Leadframe
MBE	-	Molecular beam epitaxy
NHD	-	Nail Head Diameter
NSOP	-	Non Stick on Pad
OD	-	Overdrive
PVD	-	Physical Vapor Deposition
QFN	-	Quad Flat Narrow Package
T&R	-	Tape and Reel
TF	-	Trim and Form
Temp	-	Temperature
TD	-	Touchdown
TC	-	Thermo compress
TS	-	Thermosonic
u-PPF	-	Micro Pre Plated Frame
UV	-	Ultraviolet
UVP	-	Ultraviolet processing
US	-	Ultrasonic Energy
WB	-	Wire Bonding
ZD	-	Zero Defects

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LIST OF SYMBOLS

Al	-	Aluminium
Au	-	Gold
Cu	-	Copper
C	-	Celsius
Gf	-	Gram Force
Hrs	-	Hours
mm/s	-	Milimeter per second
Mn	-	Mili-newtons
NiMop	-	Nickel Molybdenum Phosphide
Si	-	Silicon
Um	-	Micrometer
U	-	Micron
%	-	Percentage

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LIST OF PUBLICATIONS

1. Suresh Kumar, Sivarao, Tan Kim Guan and Fuaida Harun, *Influence of wafer probing against Initial bonding,* 34th International Electronics Manufacturing Technology conference (IEMT'10), 2010.

2. Suresh Kumar, Sivarao, MT Cheong, Mohd. Azmeer and Fuaida Harun, *Solving Eventual Bonding Quality to Enhance Adhension for QFN Packages,* 34th International Electronics Manufacturing Technology conference (IEMT'10), 2010.

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CHAPTER 1

INTRODUCTION

1.1 Background

Semiconductor is a material that is neither a good conductor of electricity (like copper) nor a good insulator (like rubber). The most common semiconductor materials are silicon and germanium. These materials are then doped to create an excess or lack of electrons. Computer chips, both for CPU and memory, are composed of semiconductor materials. Semiconductors make it possible to miniaturize electronic components, such as transistors. Not only does miniaturization mean that the components take up less space, it also means that they are faster and require less energy as shown in Figure 1.1. The semiconductor packaging is an integrated circuit generally comprises several steps.

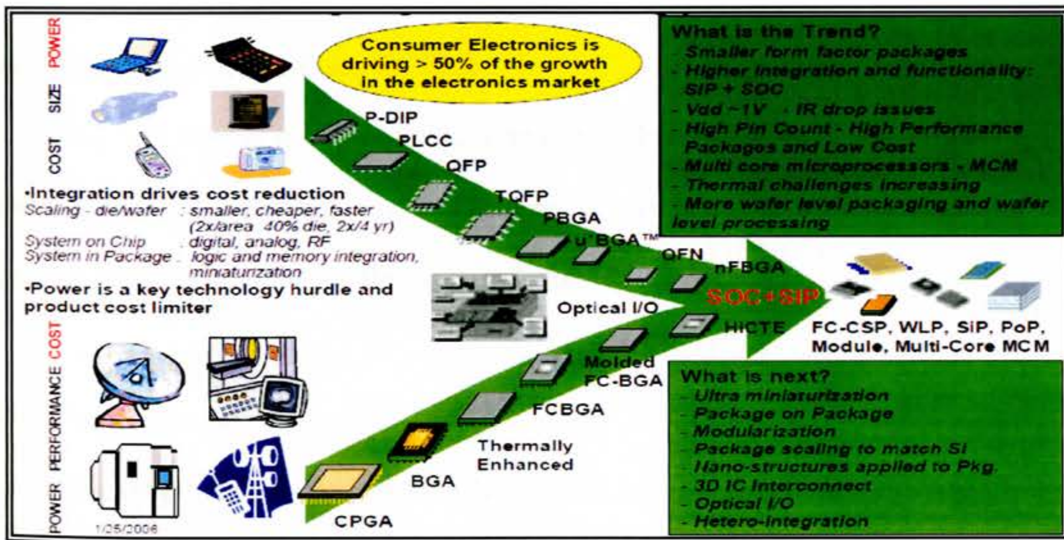

Figure 1.1: Semiconductor Future Miniaturization Packaging (Harman.G, 1997)

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The semiconductor process flow is divided into three segments and the complete process flow has been captured in Figure 12:-

- Front of Line - Assembly
- End of Line - Assembly
- Testing - Final Test.

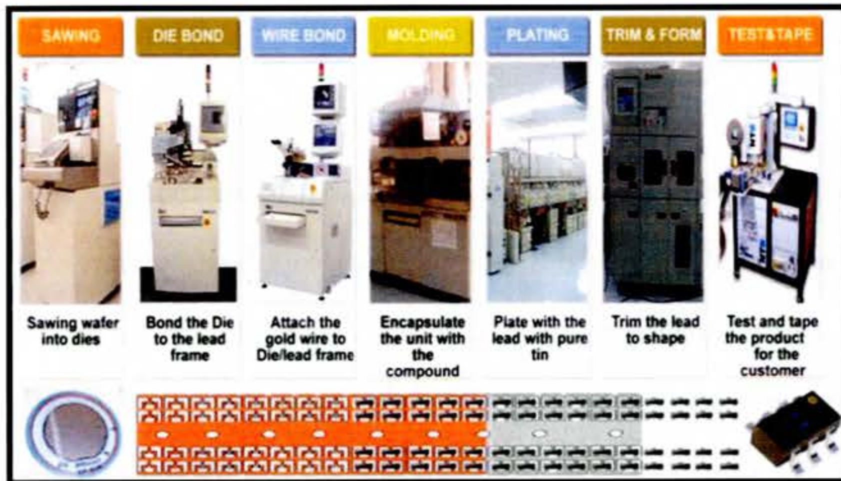

Figure 1.2: Assembly Flow Processes for Electronic Packages

1.2 Assembly Process Front Of Line

The most critical process in semiconductor is Front of Line or also known as FOL, where the focus for the experiment would be at wire bonding process. It also has three major processes which are briefly explained next.

1.2.1 Die Preparation

Die preparation is the process whereby the wafer is singulated into individual dice in preparation for following assembly processes. Die preparation consists of two major steps, namely, wafer mounting and wafer saw.

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1.2.2 Die Attach

Die Attach (also known as Die Bond) is the process of attaching the silicon chip to the die pad or die cavity of the support structure for example the lead frame of the semiconductor package. There are two common die attach processes, that are adhesive die attach and eutectic die attach. Both of these processes use special die attach equipment and die attach tools to mount the die.

1.2.3 Wire Bonding

Wire bonding is the process of providing electrical connection between the silicon chip and the external leads of the semiconductor device using very fine bonding wires. The wire used in wire bonding is usually made either of gold (Au) or aluminium (Al), although copper (Cu) wire bonding is starting to gain a foothold in the semiconductor manufacturing industry. There are two common wire bonding processes: Au ball bonding and Al wedge bonding (Zhong, et al., 2000).

1.3 Assembly Process End Of Line

End of Line or also known as EOL has three major processes which is briefly explained in following sections:-

1.3.1 Moulding

Moulding is the process of encapsulating the device in plastic material. Transfer moulding is one of the most widely used moulding processes in the semiconductor industry because of its capability to mould small parts with complex features. In this process, the moulding compound is first preheated prior to its loading into the moulding chamber.

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After pre-heating, the moulding compound is forced by a hydraulic plunger into the pot where it reaches melting temperature and becomes fluid. The plunger then continues to force the fluid moulding compound into the runners of the mould chase. These runners serve as canals where the fluid moulding compound travels until it reaches the cavities, which contain the lead frame for encapsulation.

1.3.2 Lead Finish

Lead finish is the process of applying a coat of metal over the leads of an Integrated circuit in order to protect and improve following aspects:-

- Protect the leads against corrosion
- Protect the leads against abrasion
- Improve the solder ability of the leads
- Improve the appearance of the leads.

There are two widely used lead finish techniques in the semiconductor industry namely plating and coating. There are two types of plating that are pure metal plating such as tin plating and alloy plating such as tin/lead plating (Srivastava, et al., 1979).

1.3.2.1 Trim And Form

Trim and Form are the processes which cut dambars that short the leads together towards forming the leads into the correct shape and position. This is very crucial as the process determines the exact required dimension of the leads.

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carrier tape is wound around a reel for convenient handling and transport. The reel is enclosed in a reel box before it is finally shipped to the customer.

1.5 Problem Statement

Referring to the assembly process or segment, this research has been narrowed to interconnection process as most critical process in the entire semiconductor manufacturing processes. Wire Bonding is an electrical interconnection technique using thin wire with combination of heat, pressure and/or ultrasonic energy and the sequence of bonding is shown in Figure 1.3.

Wire bonding is a solid phase welding process, where the two metallic materials (wire and pad surface) are brought into intimate contact. Once the surfaces are in intimate contact, electron sharing or inter-diffusion of atoms takes place, resulting in the formation of wire bond (Oldervoll, 2004). In wire bonding process, bonding force can lead to material deformation, breaking up contamination layer and smoothing out surface asperity, which can be enhanced by the application of ultrasonic energy. Heat can accelerate inter-atomic diffusion, thus the bond formation (Chen, et al., 1999).

Based on current industrial performance, high yield losses was due to wire bonding process and following defect are the common problems encountered at the wire bonding process. At the initial stage, below listed are the major issues normally encounter.

- Non-Sticking
- Lifted Bond
- Malformed ball.

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At the eventual stage, the issues encountered for either laminate or lead frame are as follow:

- Lifted Wedge
- Crack Wedge.

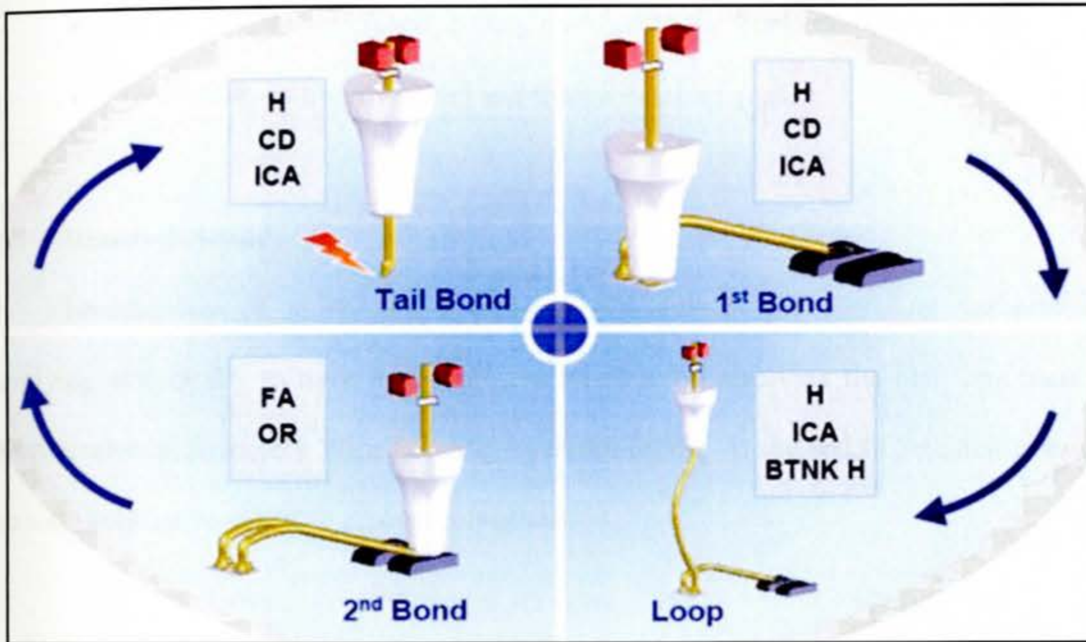

Figure 1.3: Typical Wire Bonding Cycle (Oldervoll, 2004)

Recent developments have reduced the chip size by introducing several new technologies that needs to be sustained and chapter two will be disclosing the literature review (Fuaida, 2001).

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1.6 Research Objectives

The following are the key research objectives;

- To identify suitable matrix that can well adhere with other interaction factors
- To produce high yield performance by developing initial and eventual interaction factors
- To propose the optimised probing diameter to the front end (Wafer FAB)
- To develop on improved ball and wedge bonding quality.

1.7 Research Scope

Investigation of initial and eventual would address the incoming variation by applying statistically to have robust process window on resolving the real time issue at Semiconductor Assembly Wire Bonding Interconnection. At the end of research it would be total solution to establish process robustness.

1.8 Research Benefits

- The contributions and outcomes from the design of experiment (DOE) results provides valuable information for process parameters optimization and also to improve the number of variable combination of initial and eventual bonding elements
- It will provide recommendations for design rule guidelines prior to die design and material selection
- The application on the material used versus the current demand will be a useful technology for future development.

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