8-CHANNEL LOGIC ANALYZER CONTROLLER DESIGN USING FPGA: WORK IN PROGRESS

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8-Channel Logic Analyzer Controller Design Using FPGA : Work in Progress

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Abstract **This paper presents a Field Programmable Gate Array (FPGA) based logic analyzer controller. The controller circuit is capable of performing data acquisition and signal display on a 600x480 VGA monitor. The controller was designed using Very High Speed Integrated Circuit Hardware Description Language (VHDL) coding and schematic capture. For validation, behavioral simulations are carried out using Xilinx ISE simulator. The synthesis of the controller onto Xilinx Spartan XC3S200-4FT256 FPGA chip is also presented. The motivation of this project is to explore the capability of designing a complete digital system in a single FPGA chip.**

Index Terms--**Logic Analyzer, Field Programmable Gate Array (FPGA), Very High Speed Integrated Circuit Hardware Description Language (VHDL).**

I. Introduction

Logic analyzers are widely used for testing digital or logic circuits. The continuous improvement of this test equipment is supported by the emergence of microprocessors and other complex digital circuitries [1,2]. The most popular type is the standalone logic analyzer. The capability of the logic analyzer to capture and display high speed signals in real time makes it the logical choice in research institutions and manufacturers. Nevertheless, the high performances of a standalone logic analyzer come at a high cost. For example, the TDS2000B logic analyzer manufactured by Tektronix is priced at several thousands of dollars.

An alternative would be a PC based logic analyzer, which utilizes the processing power of a normal computer. The system typically consists of a data acquisition card for capturing analog input signal and converting them to digital, a central processing unit for data processing tasks and a monitor screen for signal display. The PC based logic analyzer comes a lower price when compared to standalone logic analyzers [3]. However, the main drawback of a PC based logic analyzer is its dependence on software, which usually limits its performance.

FPGAs have been utilized to implement digital systems since its introduction in 1985 by Xilinx Inc. The initial application of FPGA to serve as prototyping module of VLSI chips and glue logic to the microprocessor-based circuits has changed to commercial design. This chip is capable of performing fast data processing to imitate the standalone logic analyzer processing circuit [4]. It has also been proven to be capable of replacing the central processing unit (CPU) in a typical PC based digital oscilloscope [5]. The final aim of this project is to have a complete FPGA based logic analyzer.

The paper is organized as follows: Section II describes the FPGA based logic analyzer system. Simulation and synthesis results are reported in part III and IV respectively. Part V concludes this paper.

II. System Overview

The proposed FPGA based logic analyzer is illustrated in Figure 1. It consists of an analog digital converter, an FPGA and a monitor screen.

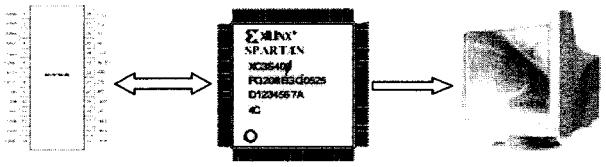

Figure 1. Structure of the system

The logic analyzer operates in two modes, Capture and Display. Figure 2 shows a general state diagram showing the two operations. The system starts to operate when it is turned on. Capture mode is immediately activated where data are captured, processed and stored. It will only go into Display mode once all memory locations are full. It will then enter the Display mode, where all stored signals are retrieved and drawn on a monitor screen. The operation then returns to Capture mode, and continues to operate in the stated manner until the system is turned off.

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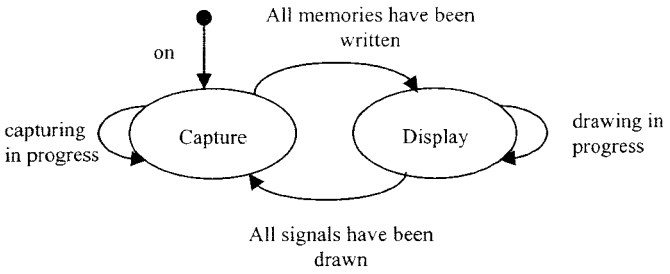

Figure 2. Logic analyzer operation

A. Analog to digital converter

Two ADS7842 ADCs from Texas Instruments are used to convert signals captured by external probe into 12-bit parallel data. This four channels ADC is capable to sample maximum of 133 KHz signal. The connection between ADS7842 and FPGA is depicted in Figure 3. All chips share common 5V supply. The clock of the ADCs is supplied by frequency divider designed in FPGA. Chip Select ($\overline{CS}$) determines which ADC will operate at one time. Each ADC starts signal conversion when Write Input ($\overline{WR}$) is activated. The 12-bit digitized data is passed to FPGA through pin *DB0-DB11* when Read Input ($\overline{RD}$) is asserted. ADC0 analog inputs are regarded as channel 0 to channel 0. Whilst, analog inputs for ADC1 is set as channel 4 to channel 7. These set up realizes the eight channels logic analyzer.

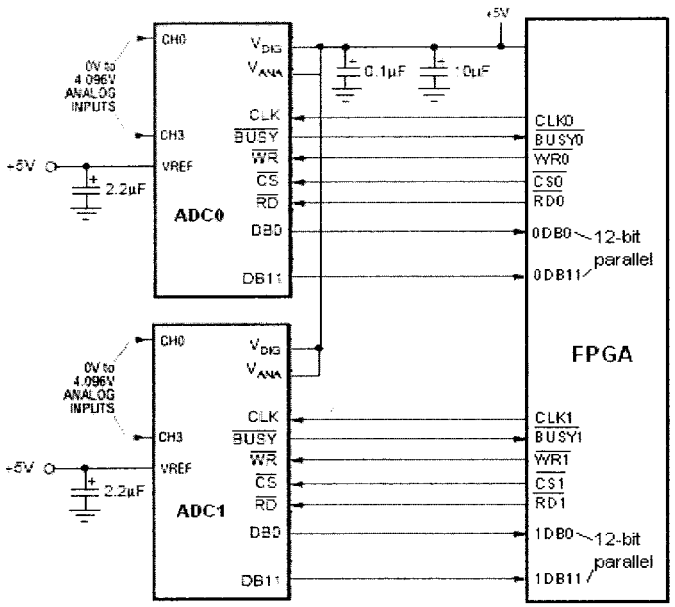

Figure 3. Connection between ADS7842 ADC and FPGA.

B. Logic analyzer controller

This is the main part of this project. The typical FPGA top-down design approach is utilized. The entire design is organized by dividing it into smaller units in the early design phase. Figure 4 shows the top view of the controller. The main components that constitute the controller are a sequencer, a frequency divider, a data comparator, a data storage unit, an address generator and a video signal generator.

The controller performs various functions such as frequency division, ADC channel multiplexing, serial to parallel conversion, level comparison and data storage. The global clock signal of 50 MHz is divided by 25 to get the 2 MHz clock signals to drive the two ADS7842 ADCs. The ADCs has a maximum operating frequency 3.2 MHz [6].

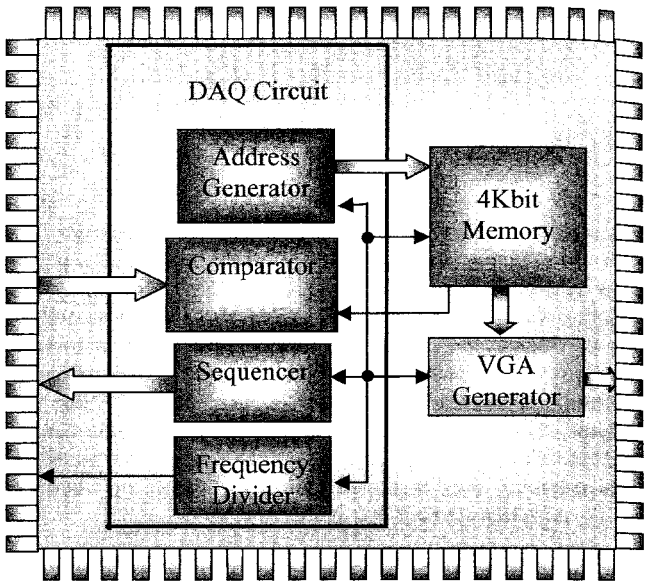

Figure 4. Logic analyzer controller

The capture of the eight input signals is performed by time-multiplexing these signals. A three-bit control signal is employed for the selection of the active channel. The value of the control bits corresponds to the channel to be activated, for example 000 means channel 0 and 100 means channel 4. The sequencer module generates the appropriate Chip Select and channel selection signals based on the three-bit control signal, which is incremented in sequence.

The 12-bit data representing the voltage level of input signals are sent to a comparator module in order to determine the logic level, 0 or 1. A simple threshold scheme is employed, where signal levels from 000000000000000 to 011111111111 are regarded as logic 0, while signal levels from 1000000000000000 to 111111111111 is regarded as logic 1. This is valid in most cases [6], but the plan is to incorporate a simple mechanism, which allows the user to self-configure the threshold in future designs.

The comparison results from the comparator are stored in a 4096-bit memory unit in groups of eight. The organization is made in such way to make it easy to retrieve and display the signal on a monitor screen. Figure 5 shows how compared signals are stored in the memory. During the first capture, data from channel 0 to 7 is written in locations 0 to 7. In the next sweep, the locations concerned are 8 to 15. This operation is repeated until all locations of the memory have been occupied.

When the memory is full, the ADC is disabled to stop signal capture. The system then goes into Display mode. The VGA controller is activated and the stored signal is read out and processed in order to display it on a monitor screen. Stored signals are drawn in sequence from channel 0 to channel 7, similar to the storage operation. The signals are drawn continuously until all memory locations have been

read. When that happens, the Display mode is stopped and the system goes into Capture mode.

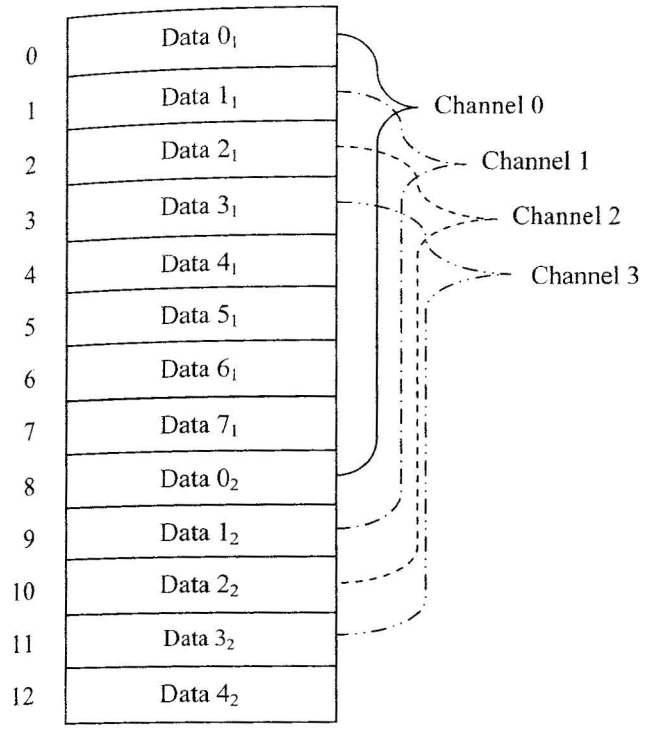

Figure 5. Memory organization

C. Monitor screen

The third element of the system is a 640 x 480 video graphic array (VGA) monitor screen. The VGA monitor can be thought of as a grid of pixels (picture elements which can be individually set to a specific color). A 640 x 480 monitor basically contains 640 columns and 480 rows of pixels. A typical monitor uses a serial scheme to set the color of each pixel. This means that the VGA controller sends the color information for each pixel one at a time, rather than all of the pixels at once in a parallel scheme. This color information for each pixel is provided by a RGB (Red, Green, Blue) triplet. Three analog signals are used represent relative amounts of red, green and blue that composes the color [5]. The template employed in displaying the signals of the eight input channels is shown in Figure 6.

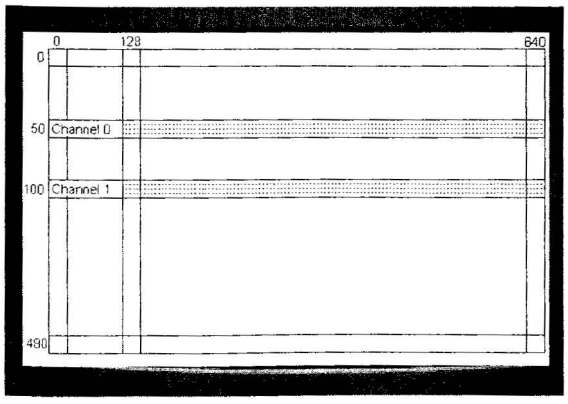

Figure 6. VGA display

Each channel occupies a uniform-sized block on the screen, defined by two sets of horizontal and vertical coordinates (x, y). For example, channel 0 occupies the block defined by coordinates (0, 0) and (640, 50). Channel 1 is positioned in block (0, 50) to (640, 100). The data stored in memory are used to draw digital signals on the screen from x = 128 to x = 640 along the horizontal lines y = 25*(k+1), k being the channel number. Pixels are drawn from left to right, suitable to the order signal data are stored in memory. Since signal data from all channels are stored in memory in an interleaved manner, this balances the display of the different channels, which gives the impression that signals from all channels are being drawn simultaneously. The display process is continued until all 4096 memory locations have been read. This corresponds to 512 horizontal positions times 8 channels.

III. Simulation Result

Figure 8 shows the simulation results of the data acquisition operation. Signal *clk2* is the 2 MHz clock supply to ADS7842, which was derived from the global 50 MHz (*clk50*) clock, after it has gone through a 1:25 frequency divider. Signal *adcmux* is activated to perform analog to digital conversion. When *adcmux* is 000 channel 0 is selected, 001 selects channel 1 and so on. A conversion is initiated on the falling edge of *adc_wr*. Data is read after falling edge of *adc_rd*. The operation is in Capture mode since *ram_enable* is HIGH and *vga_enable* is LOW. These signals match the timing diagram of ADS7842 read and write operations.

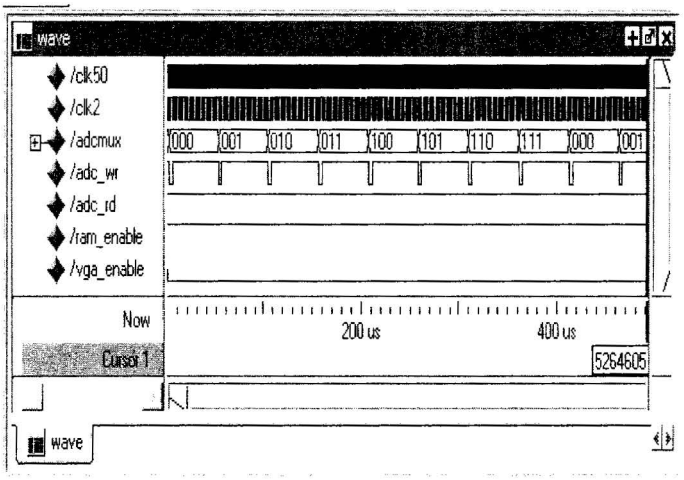

Figure 8. Data acquisition waveform.

IV. Synthesis Result

The design in register-transfer-level VHDL was sent through synthesizer software in order to produce a gate-level design, consisting of logic gates, flip-flops and their interconnections. Figure 9 depicts the synthesized circuit of the controller module.

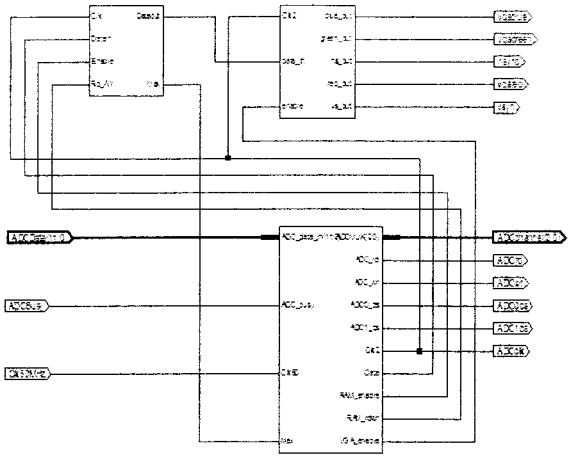

Figure 9. RTL schematic for logic analyzer controller.

V. CONCLUSION

In this paper, we described the current progress of design and implementation of an FPGA based 8-channel logic analyzer controller. It is shown that the entire logic analyzer can be accommodated in a single FPGA. Typical Xilinx FPGA design flow has been followed in completing this project. Further progress is to implement the controller circuit into FPGA chip. The performances and other aspects, such as costs and simplicity, of this completed FPGA based logic analyzer will also be compared to existing standalone and PC based logic analyzers.

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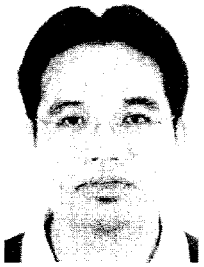
VII. BIOGRAPHIES



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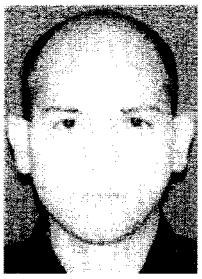
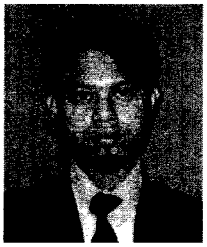


Amir Shah Abdul Aziz received his Bachelor's Degree in Electrical Engineering from the University of Rennes, France in 1999. He was accepted into ENSEEIHT, one of the major grandes ecoles in France and received his Master's Degree in Electronics in 2002. Before returning to Malaysia, he completed a research project for France Telecom R&D.
He served as lecturer for the Malaysian Multimedia University (MMU) from 2003 to 2005, before joining the Malaysian Technical University of Melaka (UTeM) in 2005. Currently, he is a researcher for a major Malaysian research company, TM R&D Sdn. Bhd.



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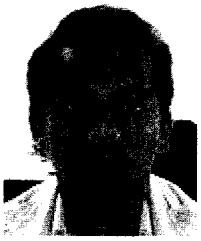

Sani Irwan Md Salim received his Bachelor Degree in Electronics Engineering from Universiti Teknologi Malaysia (UTM) in 2002 before commencing on Master Degree in Computer & Communication at Queensland University of Technology (QUT), Brisbane, Australia. Graduated in 2004, he then resume his duties as a lecturer in Universiti Teknikal Malaysia Melaka (UTeM), specializing on microprocessors and microcontrollers. His research interest is mainly on programmable devices and system with emphasis on mobile robot applications.