Characterisation of Sheet Resistivity and Contact Resistivity for Source/Drain of *n*-MOSFET Device

Rhonira Latif
Faculty of Electronics and Computer Engineering (FKEKK)
Universiti Teknikal Malaysia Melaka (UTeM), Malaysia
rhonira@utem.edu.my

***Abstract*— In this study, the sheet resistivity (ρ_s) of the thin film phosphorus ion source/drain implantation regions, and the specific interfacial contact resistivity (ρ_c) between the thin film aluminium 1% silicon electrode layer and the thin film phosphorus ion source/drain implantation regions of the *n*-channel metal-oxide-semiconductor field effect transistor (*n*-MOSFET) devices have been characterised using the Greek cross and Kelvin resistor test structures. From *TSUPREM-4*, the dose and energy of the phosphorus ion beam have been simulated to influence the sheet resistivity of the source/drain implantation regions. The secondary ion mass spectrometry (SIMS) measurement has verified the simulated surface concentration of the phosphorus ions. The measurements from the test structures have shown that the sheet resistivity and the specific interfacial contact resistivity of the source/drain terminals varied across the wafer. The influence of the heart size from the Greek cross structure and the contact area size from the Kelvin resistor structure have been investigated. In our application, the phosphorus ion dose of $1e^{16}\ ions/cm^2$ and energy of $40\ keV$ have been measured to provide the desired small sheet resistivity of $\rho_s = 25.93\ \Omega/\square$. From the measured interfacial contact resistivity of $\rho_c \sim 10^{-4}\ \Omega cm^2$, the interfacial contact area for the source/drain regions have been designed to be approximately $80\ \mu m \times 40\ \mu m$ in order to achieve the reasonable interfacial contact resistance of $R_c = 3\ \Omega$. The fabrication design for the source/drain of the *n*-MOSFET devices is optimised in order to obtain good drain current conduction with small resistances.**

***Keywords* – Contact resistivity, Greek cross, Kelvin resistor, and sheet resistivity.**

I. INTRODUCTION

The sheet resistivity and the specific interfacial contact resistivity of the source/drain regions within the metal-oxide-semiconductor field effect transistor (MOSFET) devices are important parameters to be characterised, and they have been corroborated by a large volume of published research over the years [1]-[5]. The specific interfacial contact resistivity, ρ_C specifies the contact resistance R_c between the source/drain regions and the contact materials, while the sheet resistivity ρ_s quantifies the resistance of the thin film layer ion implanted source/drain regions. These two parasitic intrinsic resistance components have significant imperative effects over the electrical performance of the MOSFET, particularly when the device is scaled down to micrometer regime. These undesirable resistances reduce the amount of current drive and degrade transconductance of the device. In order to minimise the parasitic intrinsic resistance effect, the interfacial contact areas can be made bigger, which will then reduce the interfacial contact resistance [6]. In [3], Butler *et al.* discussed the importance of creating shallow source/drain regions in MOSFETs to minimise the short channel effect at the cost of raising the undesired sheet resistivity. They suggested the silicidation of the source/drain for the reduction of the sheet resistivity from $200\ \Omega/sq$ to $8\ \Omega/sq$.

The cross sectional view of the enhancement mode *n*-channel MOSFET (*n*-MOSFET) is shown Figure 1. In our work, the boron-doped $< 100 >$ silicon wafer with the average bulk resistivity of $17\ \Omega cm$ (nominal resistivity of $\rho = 14\ \Omega cm - 20\ \Omega cm$) has been used as the substrate body [7]. The average concentration of boron within the silicon wafer is estimated to be $N_A \sim 8e^{14}\ atoms/cm^3$. The heavily doped phosphorus ion source/drain regions have been created into the lightly boron-doped silicon substrate via ion implantation technique. After the implantation, the wafer has been annealed at 1100 ℃ for $30\ minutes$ for the implanted phosphorus ions within the substrate to be activated electrically [8]. A thin layer of gate oxide with $\sim 70\ nm$ thickness has been grown thermally using the dry oxidation process at 1100 ℃ for $30\ minutes$.

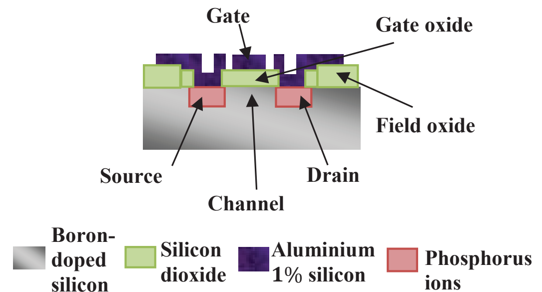


Figure 1: The cross sectional view of the enhancement mode *n*-MOSFET.

Normally, high implant doses are required for the source/drain in order for these regions to possess small resistances. The common dose values for source/drain are within $\sim 10^{15} - \sim 10^{16}\ ions/cm^2$ range, which is $\sim 4 - 5$ orders of magnitude higher than the doses used for the depletion mode channel [3][9][10]. The sheet resistivity ρ_s of

the implanted region is determined by the phosphorus ions' surface concentration N_D and the junction depth X_j [9]. ρ_s of $13\,\Omega/\square - 53\,\Omega/\square$ range has been measured for the phosphorus and arsenic ion implanted source/drain regions [3]. A small sheet resistivity for source/drain implantation regions is necessary in order to achieve high drain current conduction within the n-MOSFET devices. The source/drain regions are optimised by controlling the process parameters, such as the ion implantation energy, ion implantation dose and temperature treatment.

Aluminium 1% silicon has been employed as the metal contacts for the source/drain terminals. The aluminium 1 % silicon was used instead of aluminium in order to prevent the silicon-to-aluminium solid state diffusion process from occurring at the source/drain regions. The silicon from the substrate tend to migrate into the on-deposited aluminium leaving voids; and subsequently, the aluminium will migrate to fill in the voids, causing metal spikes into the substrate and junction shorts [11]. An addition of 1 % silicon helps to minimise the migration process. The aluminium 1 % silicon has been sputter-deposited onto the substrate before being annealed at 450 ℃ for 30 $minutes$ in order to lower the contact resistance between the aluminium 1% silicon metal and the phosphorus ion implanted source/drain regions. All metal-semiconductor contacts exhibit the interfacial contact resistance R_c [5][11][12]. The typical values of the specific interfacial contact resistivity ρ_c for source/drain of the MOSFET devices have been measured and simulated to be in $\rho_c \sim 10^{-6} - 10^{-8}\,\Omega cm^2$ range [5][6][13][14]. As the MOSFET scales down to a smaller regime, the interfacial contact resistance for source/drain of contact area $1\,\mu m \times 1\,\mu m$ has been measured to be $R_c = 30\,\Omega$ [12].

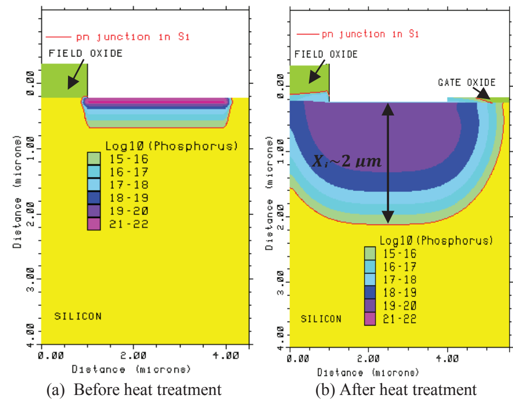
The necessity to analyse and characterise the source/drain of the fabricated n-MOSFET devices has called for suitable microelectronic test structures that are fully compatible with the device processing. Other than accurately extracting the transistor's parameter, the test structures can also be used to identify any wafer processing problems and investigate the consistency of the device performance across the wafer. In this paper, 2 test structures, namely the Greek cross structure and the Kelvin resistor structure have been fabricated across the 3–inch boron-doped $< 100 >$ silicon wafer. The Greek cross and Kelvin resistor test structures only occupy small areas on the wafer and can be fabricated simultaneously with the n-MOSFET devices using the same fabrication steps. This process provides an *in situ* sheet resistivity and interfacial contact resistivity measurements for the thin film phosphorus ion implanted source/drain regions of the n-MOSFET.

The experimental detail for the sheet resistivity characterisation has been first described. A simulation has been carried out using *TSUPREM-4* to determine the appropriate dose and energy of the phosphorus ion beam for the sheet resistivity design. After that, the silicon test wafers have been implanted with phosphorus ions according to the simulated fabrication parameters, and then they were measured using the secondary ion mass spectrometry (SIMS) in order to characterise the surface concentration and the junction depth of the source/drain regions that quantify the sheet resistivity. Alternatively, Greek cross structures have been used to measure directly the sheet resistivity of the phosphorus ion implanted source/drain regions. Finally, the Kelvin resistor structures have been employed to measure and design the resistance of the metal contact to the phosphorus ion implanted source/drain regions. Reasonable sheet and interfacial contact resistivities for the source/drain regions are pursued.

II. EXPERIMENT DESCRIPTION

A. Simulation and measurement of sheet resistivity ρ_s using TSUPREM-4 and secondary ion mass spectrometry (SIMS)

In this section, the phosphorus ion implantation parameters (i.e. ion beam dose and energy) for creating the source/drain regions of the n-MOSFET have been simulated using *TSUPREM-4*. The influence of temperature on phosphorus ion dopants distribution within the source/drain was included in the simulation. Figure 2 shows the two-dimensional simulation profiles of the implanted phosphorus ions in source/drain regions before and after being subjected to the gate oxidation and ion implantation annealing processes. High furnace temperatures in these two processes have been simulated to cause the implanted phosphorus ions to diffuse laterally across the wafer and vertically into the wafer, giving the junction depth of $X_j \sim 2\,\mu m$ for the phosphorus dose of $1e^{16}\ ions/cm^2$ and energy of 40 keV.



(a) Before heat treatment (b) After heat treatment

Figure 2: Simulation of the source/drain doping profile within the substrate wafer (a) before and (b) after the ion implantation annealing and gate oxidation processes. The high temperature processes caused vertical and lateral diffusion of the implanted phosphorus dopants.

For source/drain ion implantation, phosphorus doses of $1e^{14}\ ions/cm^2$ to $1e^{16}\ ions/cm^2$ and energies ranging from 20 keV to 40 keV have been considered for the simulation of phosphorus surface concentration N_D and junction depth X_j. The sheet resistivity, ρ_s of the thin film ion implanted region is proportional to N_D and inversely proportional to X_j. The simulation result in Table 1 shows that higher ion beam dose and energy increase both the phosphorus surface concentration and junction depth. The increase in phosphorus surface concentration with respect to the increase in ion beam energy has been found to be due to the high temperature processes

involved during the fabrication of n-MOSFET devices. The effect of increasing the junction depth is more dominant than the effect of increasing in phosphorus surface concentration and thus, it decreases the sheet resistivity of the phosphorus ion implanted source/drain regions. In our application, short channel effect due to the increase in junction depth and lateral diffusion is not a major problem for the designed channel length of $10\ \mu m - 30\ \mu m$ range [7].

From Table 1, the phosphorus dose of $1e^{16}\ ions/cm^2$ with energy of $40\ keV$ was used in the source/drain implantation process in order to obtain a reasonably small sheet resistivity of $20.4\ \Omega/\square$. The surface concentration N_D and junction depth X_j of the phosphorus ion implanted source/drain regions with dose/energy of $1e^{16}/40$ were measured using SIMS to quantify ρ_s.

Table 1: Design of N_D and X_j with respect to dose and energy of phosphorus ion beam that quantifies ρ_s for the source/drain regions.

Dose $(ions/cm^2)$	Energy (keV)	N_D (cm^{-3})	X_j (μm)	ρ_s $(\Omega/\square)$
$1e^{14}$	20	$3.0e^{17}$	1.14	870.36
$1e^{14}$	30	$4.0e^{17}$	1.16	754.85
$1e^{14}$	40	$5.0e^{17}$	1.19	683.46
$1e^{15}$	20	$3.5e^{18}$	1.36	201.01
$1e^{15}$	30	$4.5e^{18}$	1.39	178.28
$1e^{15}$	40	$5.5e^{18}$	1.40	174.51
$1e^{16}$	20	$4.0e^{19}$	1.92	22.64
$1e^{16}$	30	$5.5e^{19}$	1.97	21.00
$1e^{16}$	40	$6.5e^{19}$	1.99	20.40

The 3-inch $< 100 >$ boron-doped silicon wafer has been employed as the test wafer. The wafer has been measured in the automatic 4-point probe station and the average bulk resistivity of the substrate is $\rho \sim 17\ \Omega cm$. Thus, the concentration of boron dopant within the wafer has been taken to be $N_A \sim 8e^{14}\ atoms/cm^3$. Then, the phosphorus ions with dose of $1e^{16}\ ions/cm^2$ and $40\ keV$ energy have been implanted into the wafer. As for the references, additional two test wafers have been implanted with dose/energy of $8e^{11}/40$ and $2e^{12}/40$, respectively. The influence of temperature at $1100\ ℃$ from the gate oxidation and annealing processes is included in the experiment. Then, the doping profiles of the phosphorus ion implanted silicon test wafers have been inspected using SIMS. The technique employed the primary focused beam of high energy caesium ions Cs^+onto the phosphorus implanted silicon test wafers, producing secondary particles of phosphorus ions P^- that are detected by the mass spectrometer [15]. A well-defined crater is produced on the silicon substrate when the primary beam is sputtered over a rectangular area on the test wafer. The secondary ions are detected at a smaller area within the crater. The concentration of the implanted phosphorus ions with respect to depth within the boron-doped silicon substrate is then obtained.

B. Measurement of sheet resistivity ρ_s using Greek cross test structures

In this section, the Greek cross test structures have been fabricated to measure the sheet resistivity of the phosphorus ion implanted source/drain regions with dose/energy of $1e^{16}/40$. The Greek cross test structure is a 4-point probing technique that can extract the sheet resistivity of the thin film ion-implanted semiconductor layer or the thin film sputter-deposited metallic conductor layer [11]. The fabricated Greek cross structures have been distributed uniformly on the wafer in order to map the sheet resistivity of the phosphorus ion implantation across the wafer. The fabrication steps and geometrical dimensions of the Greek cross test structure are illustrated in Figure 3 and Figure 4. In Figure 3(a)(i), the silicon dioxide layer of $0.5\ \mu m$ thickness was grown thermally on a 3-inch boron-doped $< 100 >$ silicon wafer with an average bulk resistivity of $17\ \Omega cm$. Then, in Figure 3(b)(ii), the wafer has been patterned photolithographically with the cross structure, and reactive ion etching (RIE) technique has been performed on the silicon dioxide layer using CF_4/H_2 plasma, revealing the regions for implantation.

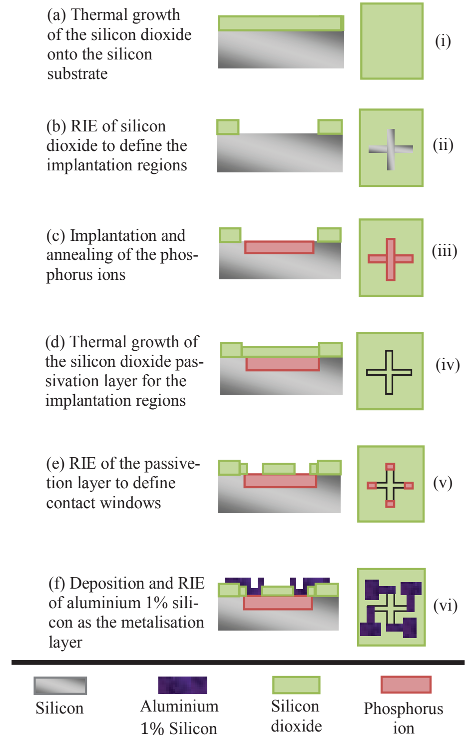
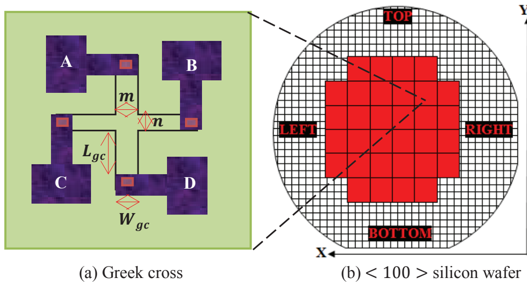


Figure 3: The fabrication steps for making the Greek cross test structures. [(a)-(f)] The cross sectional view of the process and [(i)-(vi)] top view of the process.

The silicon wafer substrate has been implanted with phosphorus ions of dose $= 1e^{16}\ ions/cm^2$ and energy $= 40\ keV$ [Figure 3(c)(iii)]. The annealing/activation step for the implanted phosphorus ions has been carried out at $1100\ ℃$ for $30\ minutes$. A thin silicon dioxide passivation layer of $\sim 70\ nm$ thickness has been grown thermally on top of the implantation regions using the dry oxidation process at

1100 °C for 30 $minutes$ [Figure 3(d)(iv)].

Next, the implanted phosphorus ion regions need to be in contact with the metal electrode pads through the pre-defined contact windows. The metal to silicon contact windows have been patterned photolithographically on the wafer, and RIE using CF_4/H_2 plasma has been performed on the passivation layer to create the contact windows [Figure 3(e)(v)]. The etch time of 5 $minutes$ is required to pattern 70 nm of the passivation layer. Then, 0.5 μm thickness of aluminium 1% silicon has been sputter-deposited onto the wafer as the metalisation layer and patterned photolithographically to define the electrodes [Figure 3(f)(vi)]. Aluminium 1% silicon has been etched using RIE employing $SiCl_4/Ar$ plasma for 20 $minutes$ in the STS metal etcher. The wafer has been annealed at 450 °C for 30 $minutes$ and finally, the fabricated Greek cross test structures have been probed electrically to measure the sheet resistivity of the phosphorus ion implanted regions.



(a) Greek cross (b) < 100 > silicon wafer

Figure 4: (a) The geometrical dimensions of the Greek cross test structure (b) The Greek cross test structures are distributed on the 32 chips across the 3–inch boron-doped < 100 > silicon wafer according to the X-Y coordinates.

The fabricated Greek cross test structures have been measured using the Hewlett Packard 4156B Semiconductor Parameter Analyzer. In this 4-point probe technique, two probes are used to carry the current, and the remaining two probes are used for voltage sensing [11]. For the Greek cross test structure shown in Figure 4(a), 50 μA of drive current I_{AB} is passed between metal pad A and B and the corresponding potential difference between metal pad D and C is measured as V_{DC} [16][17]. The drive current must be kept below 0.1 mA to prevent surface leakage current [11][17]. Higher measurement accuracy is achieved by reversing the current to I_{BA} and measure V_{CD}. The measured resistance R_{0° is given by Equation (1). Similarly, the action is repeated for the drive current applied between metal pad B and C, giving the measured resistance R_{90° as in Equation (2) [11][16].

$$R_{0^\circ} = \frac{V_{DC} - V_{CD}}{I_{AB} - I_{BA}} \quad (1)$$

$$R_{90^\circ} = \frac{V_{AD} - V_{DA}}{I_{BC} - I_{CB}} \quad (2)$$

The average of the measured resistances is calculated as R_{ave} and finally, the sheet resistivity ρ_s is extracted as in Equation (3)

$$\rho_s = \frac{\pi R_{ave}}{ln(2)} \quad (3)$$

In Figure 4(a), the Greek cross test structures with arms length of $L_{gc} = 100\ \mu m$ and arms width of $W_{gc} = 5\ \mu m$, $8\ \mu m$, $10\ \mu m$ and $16\ \mu m$ have been fabricated. In Figure 4(b), the fabricated structures are shown to be distributed at 32 different chips across the whole wafer. The electrical measurement requires $L_{gc} > 2W_{gc}$ but the arms length should also be made as short as possible in order 1) to minimise the heat generation in the arms; and 2) to prevent the surface leakage current [11][17]. In Figure 4(a), the extracted sheet resistivity of the implanted phosphorus ions is at the heart of the cross structure with the size of $m \times n$ [11][17].

C. Measurement of contact resistivity ρ_c using Kelvin resistor test structures

In this section, Kelvin resistor test structures have been fabricated in order to investigate the interfacial contact resistance between the aluminium 1 % silicon layer and the phosphorus ion implanted source/drain regions of dose $= 1e^{16}\ ions/cm^2$ and energy $= 40\ keV$. For our n-MOSFET devices, $R_c < 30\ \Omega$ is targeted and the design of the contact area will be optimised in order to achieve this. The main concern was to make sure that there is sufficient current flow with low voltage drop across the interfacial contact.

Kelvin resistor test structure is a 4-point probing technique that measures the interfacial contact resistance between two conductive layers. In order to characterise the interfacial contact resistance of the source/drain terminals in our n-MOSFET devices, aluminium 1% silicon layer and phosphorus ion implanted regions have been employed in the Kelvin resistor test structure. The geometrical dimensions of the Kelvin resistor structure are illustrated in Figure 5 and its fabrication steps are similar with the Greek cross test structure's, described previously in Figure 3.

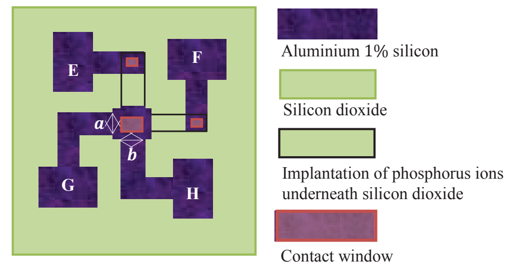


Figure 5: The geometrical dimensions of the Kelvin resistor test structure. a × b defines the interfacial contact area.

Four sizes of the interfacial contact area, $a \times b$ have been considered for the Kelvin resistor structure, which are $5\ \mu m \times 5\ \mu m$, $8\ \mu m \times 8\ \mu m$, $10\ \mu m \times 10\ \mu m$ and $16\ \mu m \times 16\ \mu m$. The electrical characteristics of the interfacial contacts have been probed electrically. The voltage across pad F and G is measured when the drive current is forced between pad E and H, giving the interfacial contact resistances of $R_1 = \frac{V_{FG}}{I_{EH}}$ and $R_2 = \frac{V_{GF}}{I_{HE}}$. The measurement is repeated by exchanging

the voltage and current pads giving $R_3 = \frac{V_{EH}}{I_{FG}}$ and $R_4 = \frac{V_{HE}}{I_{GF}}$. The average of these measured four resistances will give the total interfacial contact resistance of R_c between the implanted phosphorus ion regions and the aluminium 1% silicon metal. The specific interfacial contact resistivity can then be derived as $\rho_c = R_c A_k$ where A_k is the area of the interfacial contact, $a \times b$ [11][16].

III. Result and Discussion

A. The analysis of source/drain doping profile from SIMS

The measured doping profiles for the source/drain using SIMS are plotted in Figure 6 and compared to the simulation results from *TSUPREM-4*. The measured phosphorus surface concentrations N_D agree well with the simulations. $N_D \sim 3e^{15}\ atoms/cm^3$, $N_D \sim 7e^{15}\ atoms/cm^3$, and $N_D \sim 6e^{19} atoms/cm^3$ can be achieved by employing dose/energy of $8e^{11}/40$, $2e^{12}/40$ and $1e^{16}/40$, respectively.

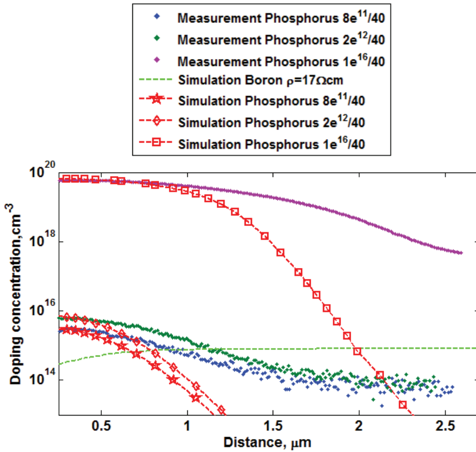


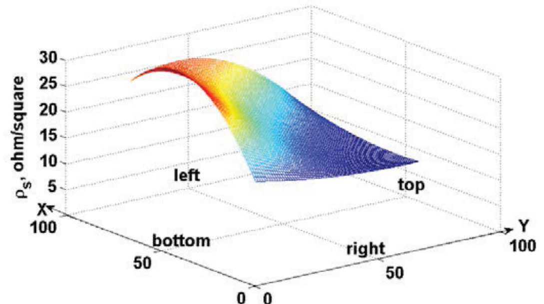
Figure 6: Comparison between the measurement and simulation of the doping profiles for dose/energy of $8e^{11}/40$, $2e^{12}/40$ and $1e^{16}/40$.

The junction depth is defined as the depth at which the phosphorus concentration equals to the boron concentration. In Figure 6, the junction depths X_j are measured to be bigger than the simulated values. There are two reasons that might explain this discrepancy. First, the phosphorus ion channelling effect might have occurred along the crystal planes in silicon. Thus, the phosphorus ion penetration is enhanced, making the junction depth to be deeper than expected. From the simulation, the phosphorus channelling effect in $< 100 >$ silicon wafer as a function of ion beam tilt and twist angle has not been included. Thus, the body tails of the distribution curves from simulations are shallower than the profiles obtained from SIMS measurements. Second, the secondary ions detection area has been made to be comparatively the same as the area of the crater. An accurate depth profiling method requires the area of the crater to be larger than the detection area in order to prevent the contribution of the phosphorus ions from the crater wall. The detected phosphorus ions from the crater wall can cause the measured junction depths to be deeper than their actual depth [15].

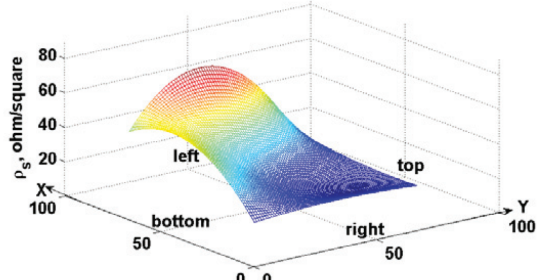
For the phosphorus ion implanted source/drain regions, the measured surface concentration of $N_D \sim 6e^{19} atoms/cm^3$ can be used in conjunction with the measured junction depth to estimate the sheet resistivity of the implanted phosphorus regions. Since the junction depth X_j could not be detected accurately from SIMS measurement, the sheet resistivity of the phosphorus ion implanted source/drain regions have been measured directly using the Greek cross test structures.

B. The characterisation of sheet resistivity ρ_s for source/drain terminals from Greek cross structures

In Figure 7, the sheet resistivities ρ_s of the implanted phosphorus ions have been measured and mapped with respect to the X-Y coordinates of the 3-inch boron-doped $< 100 >$ silicon wafer. The Greek cross test structures with the heart size of $16\ \mu m \times 16\ \mu m$ and $5\ \mu m \times 5\ \mu m$ have been considered. In both cases, the measured sheet resistivities of the implanted phosphorus ions have been observed to be non-uniform across the wafer. At the positions close to the bottom and left side of the wafer, the sheet resistivities are approximately $2-3$ times higher in magnitude compared to the ones measured close to the top and right positions of the wafer.



(a) Heart size of $16\ \mu m \times 16\ \mu m$



(b) Heart size of $5\ \mu m \times 5\ \mu m$

Figure 7: The non-uniform sheet resistivity profile of the implanted phosphorus ions measured with respect to the X-Y coordinates of the 3-inch boron-doped $< 100 >$ silicon wafer. The Greek cross test structures with heart size of (a) $16\ \mu m \times 16\ \mu m$ and (b) $5\ \mu m \times 5\ \mu m$ have been used.

The variation in sheet resistivity measurement across the wafer might be due to the 1) non-uniform boron doping within the wafer substrate, 2) non-uniform phosphorus ions implantation on the wafer, or 3) error in measurement [11]. In

our study, the phosphorus implantation process has been carried out with high uniformity across the whole wafer. Consistent probe spacings have been used during measurement and the averaging of several independent readings has reduced the measurement error to $\pm 0.4\ \Omega/\square$. Thus, the main reason for the variation in sheet resistivity measurement is due to the variation of boron concentration within the substrate.

In Figure 7(a), the measured sheet resistivities from the Greek cross structures of heart size $16\ \mu m \times 16\ \mu m$ have been observed to be smaller compared to the measured sheet resistivities from the Greek cross structures of heart size $5\ \mu m \times 5\ \mu m$ in Figure 7(b). In Figure 8, the measured sheet resistivities from the Greek cross structures of heart size $5\ \mu m \times 5\ \mu m$, $8\ \mu m \times 8\ \mu m$, $10\ \mu m \times 10\ \mu m$ and $16\ \mu m \times 16\ \mu m$ at five different positions across the wafer have been plotted. The average sheet resistivity of the implanted phosphorus ions across the wafer for $16\ \mu m \times 16\ \mu m$ is $\rho_s = 25.93\ \Omega/\square$. The decrease of heart size to $10\ \mu m \times 10\ \mu m$, $8\ \mu m \times 8\ \mu m$ and $5\ \mu m \times 5\ \mu m$ has increased the average sheet resistivity to $32.27\Omega/\square$, $44.14\ \Omega/\square$ and $52.21\ \Omega/\square$, respectively.

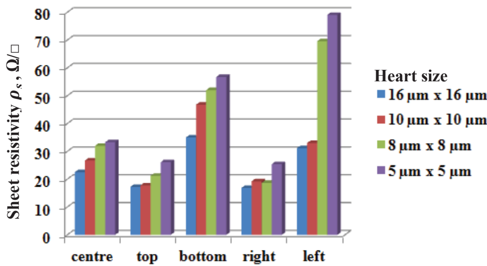


Figure 8: The sheet resistivity measurement at the positions close to the centre, top, bottom, right and left section of the wafer with respect to different heart size of the Greek cross structures. The decrease in heart size increases the sheet resistivity.

The applied drive current raises the temperature of the implanted phosphorus ion region at the arms and heart of the Greek cross test structure [11][17]. The heating increases the sheet resistivity of the implanted phosphorus ion region and this introduces error in the measurement. The heating can be minimised by decreasing the arm length L_{gc} or increasing the heart size $m \times n$ of the Greek cross test structure [17]. Thus, a more accurate sheet resistivity measurement with smaller heating effect has been obtained from the Greek cross test structure of heart size $16\ \mu m \times 16\ \mu m$. In conclusion, the average sheet resistivity of the phosphorus ion implanted source/drain regions using ion beam dose of $1e^{16}\ ions/cm^2$ and energy of $40\ keV$ has been measured to be $\rho_s = 25.93\ \Omega/\square$. The measured value is slightly higher than the simulated value of $\rho_s = 20.4\ \Omega/\square$, probably due to the heating effect within the structure. The measured sheet resistivity for source/drain regions is considerably small and thus, good drain current conduction can be achieved from the *n*-MOSFET devices.

C. The characterisation of contact resistivity ρ_c for source/drain terminals from Kelvin resistor structures.

The measured current-voltage curves of the interfacial contact between aluminium 1 % silicon layer and the phosphorus ion implanted regions at four different contact areas are shown in Figure 9. Linear current-voltage curves have been achieved for $8\ \mu m \times 8\ \mu m$, $10\ \mu m \times 10\ \mu m$ and $16\ \mu m \times 16\ \mu m$ of contact areas while non-linear current-voltage characteristic has been measured for the contact area of size $5\ \mu m \times 5\ \mu m$. This signifies that better ohmic contacts have been obtained for the larger contact areas. In addition, the increase in gradient as the contact area decreases indicates that higher interfacial contact resistance R_c has been developed as the interfacial contact area becomes smaller.

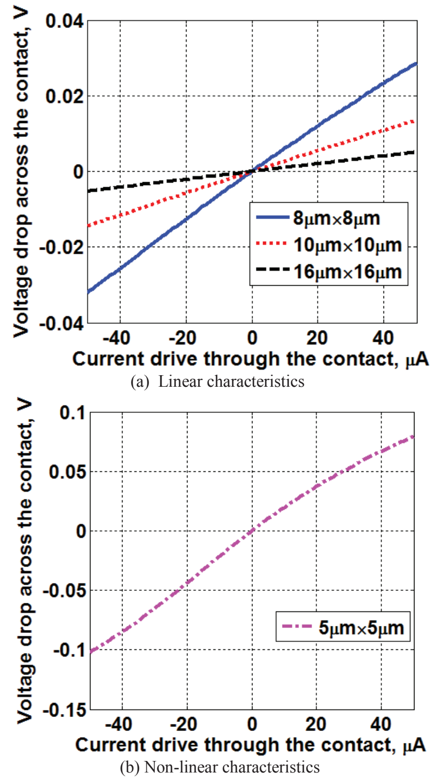


Figure 9: The measured current-voltage characteristics of the interfacial contact between aluminium 1% silicon and phosphorus ion implantation region of dose $1e^{16}\ ions/cm^2$ and energy 40 keV. The decrease in interfacial contact area has increased the gradient i.e. the interfacial contact resistance R_c.

The interfacial contact resistances R_c have been measured from the gradient of the linear current-voltage characteristics with the contact areas of $8\ \mu m \times 8\ \mu m$, $10\ \mu m \times 10\ \mu m$ and $16\ \mu m \times 16\ \mu m$. Then, the specific interfacial contact resistivities ρ_c have been derived. In Figure 10, the measured ρ_c at five different positions on the wafer have been plotted and the values have been observed to vary across the wafer.

The variation in sheet resistivity due to the non-uniform distribution profile of the boron-doped substrate has been postulated to cause the variation in the interfacial contact resistivities across the wafer [18]. The variation of ρ_c with respect to the size of the interfacial contact area in Figure 10 indicates that the contacts between aluminium 1 % silicon layer and the implanted phosphorus ion regions are non-uniform and imperfect [19]. Practically, the real contact of metal-semiconductor is not that smooth and intimate [11].

From Figure 10, the measured specific interfacial contact resistivities for the source/drain of n-MOSFET are within $\rho_c{\sim}10^{-5}-10^{-4}\,\Omega cm^2$ range which is relatively higher compared to the ones published in the literatures. Contact misalignment and insufficient phosphorus surface concentration in the source/drain can lead to higher measurement of ρ_c [13][14]. An epitaxial silicon layer might have as well regrown from the aluminium 1 % silicon metal. The presence of this epitaxial silicon layer between the original silicon surface and the aluminium 1 % silicon metal layer can increase the contact resistance [11]. Other parasitic interfacial layer that can exist is the native oxide, probably due to poor substrate cleaning or poor vacuum used during the metal deposition process [11].

The interfacial contact area for our source/drain regions will be increased in order to minimise the interfacial contact resistance [13]. The maximum interfacial contact resistivity of $\rho_c{\sim}10^{-4}\,\Omega cm^2$ has been measured between the aluminium 1 % silicon layer and the phosphorus ion implanted source/drain regions of dose $= 1e^{16}\,ions/cm^2$ and energy $= 40\,keV$. From $\rho_c{\sim}10^{-4}\,\Omega cm^2$, a reasonable interfacial contact resistance of $R_c = 3\,\Omega$ can be achieved by designing the interfacial contact area for source/drain regions to be $80\,\mu m \times 40\,\mu m$.

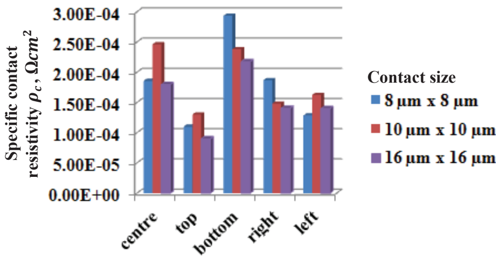


Figure 10: The specific interfacial contact resistivity measurement at the positions close to the centre, top, bottom, right and left section of the wafer with respect to the different interfacial contact area of the Kelvin resistor test structures. The variation of ρ_c for different interfacial contact area signifies that the contacts are non-uniform.

IV. Conclusion

The fabrication process and fabrication design of the source/drain regions have been studied in order to enhance the electrical performance of the n-MOSFET device. The thin film source/drain regions in n-MOSFET are formed by phosphorus ion implantation technique and metal-semiconductor interfacial contact development. The designs for the source/drain are focused on the 1) sheet resistivity of the thin film phosphorus ion implantation regions; and 2) the interfacial contact resistivity between the phosphorus ion implantation regions and the thin film aluminium 1% silicon electrode layer through the pre-defined contact windows. The thin film phosphorus ion surface concentrations of the source/drain regions have been measured using the SIMS technique, and it was found to be consistent with the simulation. From simulation, the dose and energy for the implantation of the phosphorus ion have been designed to be $1e^{16}\,ions/cm^2$ and $40\,keV$, respectively in order to obtain small sheet resistivity of $\rho_s = 20.4\,\Omega/\square$. From measurement, the average sheet resistivity of the phosphorus ion implanted source/drain regions has been extracted using the Greek cross test structure to be $\rho_s = 25.93\,\Omega/\square$, higher than the designed value probably due to the heating effect within the structure. The design and characterisation of the interfacial contact for the source/drain regions has been carried out using the Kelvin resistor test structure. As the interfacial contact area increases, better ohmic contact with linear current-voltage characteristics has been obtained. Furthermore, the interfacial contact resistance R_c has been measured to decrease with the increase of the interfacial contact area. The maximum specific interfacial contact resistivity of $\rho_c{\sim}10^{-4}\,\Omega cm^2$ has been extracted between the aluminium 1 % silicon layer and the phosphorus ion implanted source/drain regions of dose $1e^{16}\,ions/cm^2$ and energy $40\,keV$. From $\rho_c{\sim}10^{-4}\,\Omega cm^2$, the interfacial contact area for the source/drain regions have been designed to be approximately $80\,\mu m \times 40\,\mu m$ in order to achieve the reasonable interfacial contact resistance of $R_c = 3\,\Omega$. Good drain current conduction can be achieved from the n-MOSFET with the design of small interfacial contact resistivity and sheet resistivity for the source/drain regions. The variation of the interfacial contact resistivity and sheet resistivity across the wafer due to the non-uniform boron doping of the substrate wafer needs to be minimised in order to obtain a more reliable and consistence device performance.

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