VOL. 11, NO. 11, JUNE 2016 ISSN 1819-6608
ARPN Journal of Engineering and Applied Sciences
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# APPLICATION OF TAGUCHI METHOD WITH THE INTERACTION TEST FOR LOWER DIBL IN $WSi_x/TiO_2$ CHANNEL VERTICAL DOUBLE GATE NMOS

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## ABSTRACT

The poly-Si/$SiO_2$ based MOSFETs have been encountering a problem with the limitation of channel length for the device miniaturization. The drain induced barrier lowering (DIBL) effect is the main threat for the device to acquire excellent device's characteristics. Thus, the metal-gate/high-*k* technology is a smart choice for the future replacement of poly-Si/$SiO_2$ channel. This paper introduces the implementation of $WSi_x/TiO_2$ channel to replace the poly-Si/$SiO_2$ channel in vertical double-gate NMOS structure, followed by the application of Taguchi method to reduce the drain induced barrier lowering (DIBL) effects. The device was virtually fabricated and characterized by using both ATHENA and ATLAS modules of SILVACO TCAD tools. The $L_{12}$ orthogonal array, main effects, signal-to noise ratio (SNR) and analysis of variance (ANOVA) were utilized to analyze the effect of process parameter variations on the DIBL. Later, the interactions between the process parameters were investigated by using $L_8$ orthogonal array of Taguchi method. Based on the final results, halo implant tilt angle and source/drain (S/D) implant energy were identified as the most dominant process parameters where each of them contributes 24% and 16% of factor effects on SNR respectively. The lowest possible value of DIBL after the optimization with the interaction test is 1.552 mV/V.

**Keywords:** ANOVA, DIBL, SNR, Taguchi method.

## INTRODUCTION

The drain induced barrier lowering (DIBL) effect arises in the planar MOSFET device when the channel length (Lc) is reduced for scaling purpose which lead to the degradation of the device characteristics. As the channel length (Lc) decreases, the depletion region of the source and drain become closer to each other which leads to the increase of the charge sharing effect [1]. Under this circumstance, the controllability of the channel region by the gate is reduced as the electric field in the source region is increased [2].

The introduction of the vertical type of MOSFET layout was proven to tackle these issues as the channel length (Lc) has no dependence on critical lithography [3-6]. Another factor that causes the device to suffer the severe DIBL effect is the reduction of $SiO_2$ gate dielectric thickness (Tox). The scaling of the thickness of $SiO_2$ gate dielectric is very crucial to increase the capacitance of the gate dielectric for SCE's mitigation [7, 8]. However, the reduction of Tox leads to the increase of gate leakage. Thus, the solution to address this issue is to replace the $SiO_2$ gate dielectric with a higher dielectric constant (high-*k*) material [9].

The incompatibility of high-*k* material with the poly-Si gate has caused severe carrier mobility degradation which eventually leads to lower drive current ($I_{ON}$). To eliminate this problem, the poly-Si gate is replaced by the metal-gate which is proven to solve the compatibility issues. The most recent researches on the metal-gate/high-*k* MOSFET device by Afifah et al. and Atan et al. indicated that the compatibility of titanium dioxide ($TiO_2$) and hafnium dioxide ($HfO_2$) dielectric towards the tungsten silicide ($WSi_x$) gate exhibited significant improvements on the overall MOSFET's characteristics [10, 11]. It was observed that the leakage current ($I_{OFF}$) has tremendously decreased even at a very small gate length (Lg) due to the utilization of $TiO_2$ and $HfO_2$ dielectric along with $WSi_x$ gate.

The process parameter variations are one of the major factors that affecting the performance of MOSFET device. These variations have directly influenced the DIBL value in the MOSFET device. An attempt to reduce the DIBL value was done by Salehudin et al. using Taguchi method [12]. This work proved that Taguchi method was capable of reducing approximately 26.5% of the DIBL value. Furthermore, Taguchi method was also utilized to reduce the sheet resistance (Rs) and to obtain the nominal threshold voltage ($V_{TH}$) as demonstrated by Mansor et al. and Mohammad et al. respectively [13, 14].

This paper emphasizes on the optimization of multiple process parameters for the lowest possible value of DIBL in WSix/$TiO_2$ channel vertical double-gate NMOS device. The optimization approaches presented in this paper were split into two stages. The first stage describes on the optimization of eleven process parameters upon the DIBL value using the $L_{12}$ orthogonal array of Taguchi method. The optimization process was further improved with the interaction test analysis using the $L_8$ orthogonal of Taguchi method to detect the presence of the interaction effect among the process parameters. The optimal level of process parameters was then predicted from the lowest recorded DIBL value.

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## DEVICE STRUCTURE

The cross-sectional view simulated by using an ATHENA module of the Silvaco TCAD tools is depicted in Figure-1. The sample used for the device structure was <100> orientation of p-type (boron doped) silicon substrate with concentration of 1 x $10^{14}$ atom/cm$^3$. The vertical silicon pillar was constructed to isolate the two vertical metal gates ($WSi_x$). The nitride layer ($Si_3Ni_4$) was deposited on the sidewalls of both the gates and the pillar as they are the active area of the device [15]. The device was simulated with a $TiO_2$ dielectric thickness of 3 nm.

The source/drain regions were heavily doped ($10^{18}$ atom cm$^{-3}$) whereas the channel has a uniform p-doping of 1.81x$10^{12}$ atom cm$^{-3}$. The halo implantation was implemented by implanting 2.82 x $10^{13}$ atom cm$^{-3}$ in the substrate to prevent expansion of the drain depletion region into the lightly doped channel when the device is biased for operation [16].

Finally, phosphor compensation implantation with the dose of 2.51x$10^{12}$ atom cm$^{-3}$ was performed to reduce the parasitic capacitance. The aluminum layer was deposited on the top structure's surface and any unwanted aluminum was etched to create the contacts [17, 18]. The final vertical double gate NMOS device structure with $WSi_x/TiO_2$ stack technology was completed by mirroring the right-hand side structure.

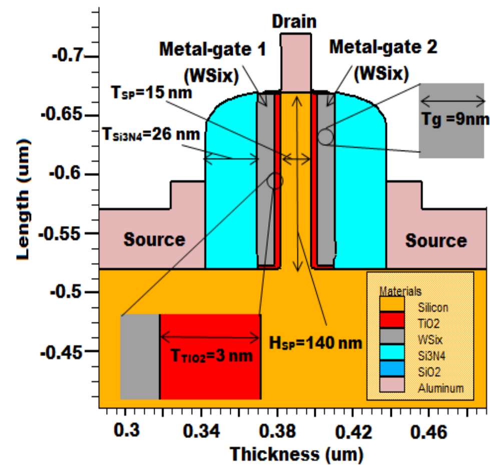


**Figure-1.** Cross-sectional view of $WSi_x/TiO_2$ vertical double-gate NMOS device.

## DEVICE CHARACTERIZATION

The DIBL value of the $WSi_x/TiO_2$ channel vertical double-gate NMOS device were retrieved by utilizing ATLAS module of Silvaco TCAD tools. The device simulation condition for DIBL value was set up as shown in Table-1.

**Table-1.** Device simulation conditions.

| Device characteristics | Drain voltage, $V_D$ (V) | Gate voltage, $V_G$ (V) | | |
|---|---|---|---|---|
| | | $V_{Initial}$ | $V_{Step}$ | $V_{Final}$ |
| Drain Induced Barrier Lowering (DIBL) | 0.1 | 0 | 0.1 | 1.5 |
| | 3.0 | 0 | 0.1 | 1.5 |

Figure-2 depicts the graph of subthreshold drain current ($I_D$) versus ramp gate voltage ($V_G$) at drain voltage $V_D$ = 0.1 V and $V_D$ = 3.0 V for $WSi_x/TiO_2$ channel vertical double-gate NMOS device. This procedure was performed in order to obtain two different values of threshold voltage which were $V_{TH1}$ and $V_{TH2}$. Afterwards, the value of DIBL was calculated by using the Equation (1) [12]:

$$DIBL = \frac{V_{TH1} - V_{TH2}}{V_{D2} - V_{D1}} \quad (1)$$

The initial DIBL value was observed to be 2.168 mV/V. In the next section, the $L_{12}$ orthogonal array of Taguchi method was conducted to figure out the best process recipe that could yield the lowest DIBL value. Moreover, the process parameters that significantly influence the DIBL value can also be identified.

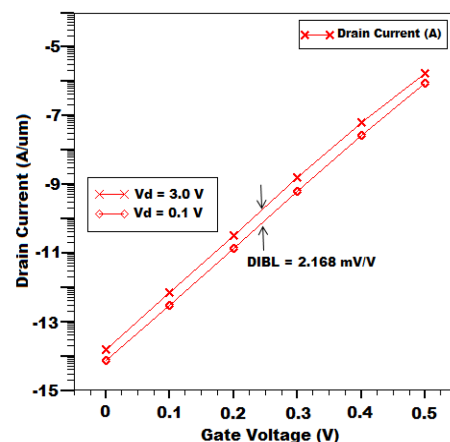


**Figure-2.** Graph sub-$I_D$ vs. ramp $V_G$ for vertical double gate NMOS device.

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## TAGUCHI METHOD WITHOUT INTERACTION TEST

### Selection of the process parameters and the orthogonal array

The control factors (process parameters) that were involved in the Taguchi analysis were known as: substrate implant dose, $V_{TH}$ implant dose, $V_{TH}$ implant energy, $V_{TH}$ implant tilt, halo implant dose, halo implant energy, halo implant tilt, S/D implant dose, S/D implant energy, S/D implant tilt and compensation implant dose and they were represented by the alphabetical symbols: A, B, C, D, E, F, G, H, J, K and L respectively. The compensation implant energy and compensation implant tilt angle were selected to be the noise factors as they do not contribute much effect on the DIBL value. The detailed level of the process parameters and the noise factor are listed in Table-2 and Table-3 respectively.

**Table-2.** Process parameters of $WSi_x/TiO_2$ vertical double gate NMOS device

| Symbol | Process parameter | Units | Level 1 | Level 2 |
|---|---|---|---|---|
| A | Substrate Implant Dose | atom/cm$^3$ | 1x10$^{14}$ | 1.03x10$^{14}$ |
| B | $V_{TH}$ Implant Dose | atom/cm$^3$ | 1.81x10$^{12}$ | 1.84x10$^{12}$ |
| C | $V_{TH}$ Implant Energy | kev | 20 | 22 |
| D | $V_{TH}$ Implant Tilt | degree | 7 | 10 |
| E | Halo Implant Dose | atom/cm$^3$ | 2.82x10$^{13}$ | 2.85x10$^{13}$ |
| F | Halo Implant Energy | kev | 170 | 172 |
| G | Halo Implant Tilt | degree | 25 | 28 |
| H | S/D Implant Dose | atom/cm$^3$ | 1.22x10$^{18}$ | 1.25x10$^{18}$ |
| J | S/D Implant Energy | kev | 18 | 20 |
| K | S/D Implant Tilt | degree | 80 | 83 |
| L | Compensation Implant Dose | atom/cm$^3$ | 2.51x10$^{12}$ | 2.54x10$^{12}$ |

**Table-3.** Noise factors and their levels.

| Symbol | Noise factor | Units | Level 1 | Level 2 |
|---|---|---|---|---|
| **U** | Compensation Implant Energy | kev | 60 | 62 |
| **V** | Compensation Implant Tilt | degree | 7 | 10 |

The total degree of freedom (DF) of the process parameters is an important aspect that is required in the selection of the orthogonal array (OA) for the design of experiment (DoE) [20, 21]. Basically, the DF is the number of comparisons among process parameters that is involved in the process of determining the best parametric level [22]. In this study, the total DF for the process parameters were equal to eleven, since each process parameter was only varied into two levels. Thus, the $L_{12}$ ($2^{11}$) orthogonal array with eleven columns and twelve rows was selected for the DoE. The DoE layout for the eleven process parameters using the $L_{12}(2^{11})$ orthogonal array is shown in Table-4.

### Signal-to-noise ratio (SNR) analysis

The signal-to-noise ratio (SNR) was computed in order to determine the sensitivity of multiple process parameters upon DIBL value in a controlled procedure. From the perspective of the Taguchi approach, the term ‘signal’ implies the desirable effect for the DIBL value. On the other hand, the term ‘noise’ indicates the undesirable effect for the DIBL value. The main aim of the SNR analysis is to figure out which process parameters produce the highest SNR. The highest SNR is desired for a certain process parameter that would indicate how much the signal is larger than the noise, thereby reduces the process variations. In order to find the process recipe that would yield the lowest DIBL value, the lower-the-better quality characteristic of SNR analysis was utilized. The SNR (lower-the-better), η can be expressed as [23]:

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$$\eta = -10Log_{10}\left[\frac{1}{n}\sum_{i=1}^{n} y_i^2\right] \quad (2)$$

where $n$ is number of tests and $yi$ is the experimental values of the DIBL.

The SNR of each set of experiment was computed by using (2) and recorded in Table-4. Since the DoE was orthogonally constructed, the effect of each process parameter can be separated out. The SNR (Lower-the-better) for each level of process parameters with an overall mean of SNR were summarized in Table-6.

**Table-4.** $L_{12}$ Orthogonal array of taguchi method.

| Exp. No. | Process parameter (Control Factors) level | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | A | B | C | D | E | F | G | H | J | K | L |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 2 | 1 | 1 | 1 | 1 | 1 | 2 | 2 | 2 | 2 | 2 | 2 |
| 3 | 1 | 1 | 2 | 2 | 2 | 1 | 1 | 1 | 2 | 2 | 2 |
| 4 | 1 | 2 | 1 | 2 | 2 | 1 | 2 | 2 | 1 | 1 | 2 |
| 5 | 1 | 2 | 2 | 1 | 2 | 2 | 1 | 2 | 1 | 2 | 1 |
| 6 | 1 | 2 | 2 | 2 | 1 | 2 | 2 | 1 | 2 | 1 | 1 |
| 7 | 2 | 1 | 2 | 2 | 1 | 1 | 2 | 2 | 1 | 2 | 1 |
| 8 | 2 | 1 | 2 | 1 | 2 | 2 | 2 | 1 | 1 | 1 | 2 |
| 9 | 2 | 1 | 1 | 2 | 2 | 2 | 1 | 2 | 2 | 1 | 1 |
| 10 | 2 | 2 | 2 | 1 | 1 | 1 | 1 | 2 | 2 | 1 | 2 |
| 11 | 2 | 2 | 1 | 2 | 1 | 2 | 1 | 1 | 1 | 2 | 2 |
| 12 | 2 | 2 | 1 | 1 | 2 | 1 | 2 | 1 | 2 | 2 | 1 |

**Table-5.** Experimental results for DIBL and SNR.

| Exp. No. | **DIBL** (mV/V) | | | | | |
|---|---|---|---|---|---|---|
| | **$DIBL_1$** ($U_1V_1$) | **$DIBL_2$** ($U_1V_2$) | **$DIBL_3$** ($U_2V_1$) | **$DIBL_4$** ($U_2V_2$) | **Mean sum of SQ** | **SNR** (Lower-the-better) (dB) |
| 1 | 2.168 | 2.336 | 2.182 | 2.237 | 5.0 | -6.97 |
| 2 | 1.823 | 1.843 | 3.512 | 1.768 | 5.5 | -7.44 |
| 3 | 2.279 | 2.458 | 2.289 | 2.350 | 5.5 | -7.40 |
| 4 | 2.246 | 2.446 | 2.269 | 2.331 | 5.4 | -7.33 |
| 5 | 1.738 | 1.880 | 1.751 | 1.798 | 3.2 | -5.07 |
| 6 | 3.349 | 1.692 | 4.966 | 3.256 | 1.2 | -10.91 |
| 7 | 1.835 | 1.984 | 1.859 | 1.902 | 3.6 | -5.56 |
| 8 | 1.914 | 2.073 | 1.935 | 1.984 | 3.9 | -5.92 |
| 9 | 1.674 | 1.825 | 1.678 | 1.732 | 3.0 | -4.75 |
| 10 | 1.894 | 2.048 | 1.901 | 1.955 | 3.8 | -5.80 |
| 11 | 1.610 | 1.739 | 1.623 | 1.664 | 2.8 | -4.40 |
| 12 | 2.163 | 2.350 | 2.181 | 2.242 | 5.0 | -6.99 |

The data from Table-6 was converted to SNR response graph as depicted in Figure-3 for better interpretation. The higher SNR of the level of certain process parameter contributes the lower value of DIBL for the device. Nevertheless, the significant measurement for every process parameter in acquiring the lowest possible DIBL value is still required to be implemented. This was done by using the analysis of variance (ANOVA) as described in the next section.

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**Table-6.** SNR of process parameters in $WSi_x/TiO_2$ channel vertical double gate NMOS device.

| Sym. | Process parameter | SNR (Higher-the-better) in dB | | Overall mean SNR (dB) |
|---|---|---|---|---|
| | | Level 1 | Level 2 | |
| A | Substrate Implant Dose | -7.52 | -5.57 | -6.55 |
| B | $V_{TH}$ Implant Dose | -6.34 | -6.75 | |
| C | $V_{TH}$ Implant Energy | -6.31 | -6.78 | |
| D | $V_{TH}$ Implant Tilt | -6.37 | -6.72 | |
| E | Halo Implant Dose | -6.85 | -6.24 | |
| F | Halo Implant Energy | -6.67 | -6.42 | |
| G | Halo Implant Tilt | -5.73 | -7.36 | |
| H | S/D Implant Dose | -7.10 | -5.99 | |
| J | S/D Implant Energy | -5.87 | -7.22 | |
| K | S/D Implant Tilt | -6.95 | -6.14 | |
| L | Compensation Implant Dose | -6.71 | -6.38 | |

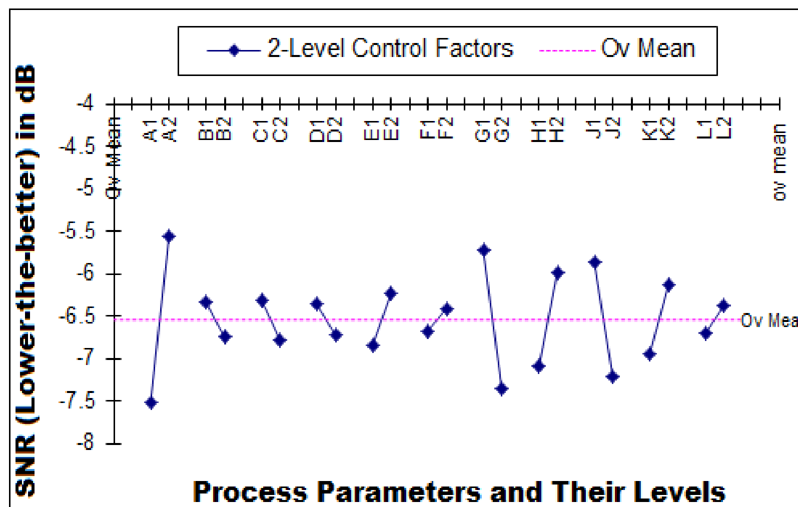


**Figure-3.** Factor effects graph for SNR (Lower-the-better).

**Analysis of variance (ANOVA)**

The main objective of the ANOVA was to reveal the level of significance for each process parameter that would possibly affect the DIBL value. The ANOVA consists of the sum of squares (SSQ), degree of freedom (DF), variance or mean square (MS), F-value and percentage of the effect of each factor or process parameter [24]. Table-7 depicts the results of pooled ANOVA for lower DIBL.

The F-ratio is computed for 95% level of confidence. According to the ANOVA results, factor A (halo implant energy), factor G (halo implant tilt) and factor J (S/D implant energy) were identified to be the most dominant process parameters that affect the DIBL value in which each of them have contributed 34%, 24% and 16% of factor effect on SNR respectively.

**Verification test**

Based on the results retrieved from SNR analysis and ANOVA, the optimal level of process parameters for lower DIBL value was identified to be factor: $A_2$, $B_1$, $C_1$, $D_1$, $E_2$, $F_2$, $G_1$, $H_2$, $J_1$, $K_2$ and $L_2$. The detailed level of the optimized process parameters for lower DIBL in the $WSi_x/TiO_2$ channel vertical double-gate NMOS device suggested by $L_{12}$ orthogonal array of Taguchi method is shown in Table-8.

The device with the optimized process parameters was then re-simulated by using Silvaco TCAD tools for verification. The verification results are listed in Table-9 and the lowest value of DIBL was observed to be 1.730 mV/V with SNR of -2.83 dB.

However, it can be observed that the DIBL value was not the lowest among all the DIBL values listed in Table-5. Thus, the interaction effects among the process parameters were suspected to be presented on the device.

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After some observation made on the results, factor A (substrate implant dose), factor E (halo implant dose) and factor G (halo implant tilt) were suspected to have interaction effects with each others.

In the next section, the three suspected process parameters were re-analyzed for the interaction test by using $L_8$ orthogonal array of Taguchi method. Meanwhile, the level of the remaining process parameters that were not involved in the interaction test were fixed as shown in Table-8.

**Table-7.** Results of ANOVA.

| Factor | DF | SSQ | MS | F-value | Factor effect on SNR (%) | Dominant/ Significant/ Neutral |
|---|---|---|---|---|---|---|
| A | 1 | 11 | 11 | 3407 | 34 | Dominant |
| B | 1 | 1 | 1 | 150 | 1 | Neutral |
| C | 1 | 1 | 1 | 193 | 2 | Neutral |
| D | 1 | 0 | 0 | 116 | 1 | Neutral |
| E | 1 | 1 | 1 | 327 | 3 | Neutral |
| F | 1 | 0 | 0 | 60 | 1 | Neutral |
| G | 1 | 8 | 8 | 2360 | 24 | Dominant |
| H | 1 | 4 | 4 | 1101 | 11 | Significant |
| J | 1 | 5 | 5 | 1611 | 16 | Dominant |
| K | 1 | 2 | 2 | 581 | 6 | Significant |
| L | 1 | 0 | 0 | 95 | 0.95 | Neutral |

**Table-8.** Best combinational level of process parameters.

| Sym. | Process parameter | Units | Best value |
|---|---|---|---|
| A | Substrate Implant Dose | atom/cm$^3$ | 1.03x10$^{14}$ |
| B | $V_{TH}$ Implant Dose | atom/cm$^3$ | 1.81x10$^{12}$ |
| C | $V_{TH}$ Implant Energy | kev | 20 |
| D | $V_{TH}$ Implant Tilt | degree | 7 |
| E | Halo Implant Dose | atom/cm$^3$ | 2.85x10$^{13}$ |
| F | Halo Implant Energy | kev | 172 |
| G | Halo Implant Tilt | degree | 25 |
| H | S/D Implant Dose | atom/cm$^3$ | 1.25x10$^{18}$ |
| J | S/D Implant Energy | kev | 18 |
| K | S/D Implant Tilt | degree | 83 |
| L | Compensation Implant Dose | atom/cm$^3$ | 2.54x10$^{12}$ |

**Table-9.** Verification results for DIBL using $L_{12}$ orthogonal array of Taguchi Method.

| **DIBL** (mV/V) | | | | **SNR** (Lower-the-better) **in dB** |
|---|---|---|---|---|
| **DIBL** ($U_1V_1$) | **DIBL** ($U_1V_2$) | **DIBL** ($U_2V_1$) | **DIBL** ($U_2V_2$) | |
| 1.730 | 1.874 | 1.743 | 1.790 | -2.83 |

## TAGUCHI METHOD WITH INTERACTION TEST

### Selection of the process parameters and the orthogonal array

Three process parameters which were Factor A (substrate implant dose), factor E (Halo implant dose) and factor G (halo implant tilt) were included in the DoE of Taguchi method with the interaction test. The $L_8$ orthogonal array of Taguchi method was employed for the interaction test where each of the factors was varied into two levels as depicted in Table-10. The substrate implant dose, Halo Implant Dose, and Halo Implant Tilt were reassigned as factor A, B and C respectively. The noise factors were fixed at the same level as in Table-2. Eight sets of experiment were run as outlined in Table-11.

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**Table-10.** Process parameters of $WSi_x/TiO_2$ vertical double gate NMOS device.

| Sym. | Process parameter | Units | Level 1 | Level 2 |
|---|---|---|---|---|
| A | Substrate Implant Dose | atom/cm$^3$ | 1x10$^{14}$ | 1.03x10$^{14}$ |
| B | Halo Implant Dose | atom/cm$^3$ | 2.82x10$^{13}$ | 2.85x10$^{13}$ |
| C | Halo Implant Tilt | degree | 25 | 28 |

**Table-11.** $L_8$ Orthogonal array of Taguchi Method with interaction.

| Exp. no. | Process parameter | | | | |
|---|---|---|---|---|---|
| | **A** | **B** | **N(AxB)** | **C** | **M(BxC)** |
| 1 | 1 | 1 | 1 | 1 | 1 |
| 2 | 1 | 1 | 1 | 2 | 2 |
| 3 | 1 | 2 | 2 | 1 | 2 |
| 4 | 1 | 2 | 2 | 2 | 1 |
| 5 | 2 | 1 | 2 | 1 | 1 |
| 6 | 2 | 1 | 2 | 2 | 2 |
| 7 | 2 | 2 | 1 | 1 | 2 |
| 8 | 2 | 2 | 1 | 2 | 1 |

**Signal-to-noise ratio (SNR) analysis**

Table-12 shows the experimental data for DIBL value and their corresponding SNR computed by using (2). The mean of SNR for each level of process parameters was computed and listed in Table-13. According to Table-13, the factor effects graph for SNR (Lower-the-better) is plotted as depicted in Figure-4. The dashed horizontal line in the graph represents the overall mean of SNR (Lower-the-better) which is -4.92 dB. From the graph, it can be observed that factor $A_2B_1C_1$ have been selected as the optimal value due to their higher SNR.

The interpretation of the data produced from the SNR analysis was done in order to determine the presence of the interaction effects. Basically, the approach was to separate the influence of an interacting process parameter from the influence of the others. Factor interaction: AxB and BxC are the interactions that have been tested in this experiment.

**Table-12.** Experimental results for DIBL and SNR.

| Exp. No. | **DIBL** (mV/V) | | | | | |
|---|---|---|---|---|---|---|
| | **$DIBL_1$** ($U_1V_1$) | **$DIBL_2$** ($U_1V_2$) | **$DIBL_3$** ($U_2V_1$) | **$DIBL_4$** ($U_2V_2$) | **Mean of Sum reciprocal squares** | **SNR** (Lower-the-better) |
| 1 | 1.552 | 1.675 | 1.566 | 1.605 | 2.56 | -4.08 |
| 2 | 1.683 | 1.819 | 1.705 | 1.744 | 3.02 | -4.80 |
| 3 | 1.730 | 1.873 | 1.743 | 1.789 | 3.18 | -5.03 |
| 4 | 1.877 | 2.036 | 1.900 | 1.947 | 3.77 | -5.76 |
| 5 | 1.552 | 1.675 | 1.566 | 1.605 | 2.56 | -4.08 |
| 6 | 1.683 | 1.819 | 1.705 | 1.744 | 3.02 | -4.80 |
| 7 | 1.730 | 1.874 | 1.743 | 1.790 | 3.19 | -5.03 |
| 8 | 1.877 | 2.036 | 1.900 | 1.947 | 3.77 | -5.76 |

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**Table-13.** SNR of process parameters in $WSi_x/TiO_2$ vertical double Gate NMOS device.

| Sym. | Process parameter | **SNR** (Lower-the-better) **in dB** | | **Overall mean SNR** (dB) |
|---|---|---|---|---|
| | | **Level 1** | **Level 2** | |
| A | Substrate Implant Dose | -4.92 | -4.92 | -4.92 |
| B | Halo Implant Dose | -4.44 | -5.40 | |
| N(AxB) | AxB | -4.92 | -4.92 | |
| C | Halo Implant Tilt | -4.56 | -5.28 | |
| M(BxC) | BxC | -4.92 | -4.92 | |

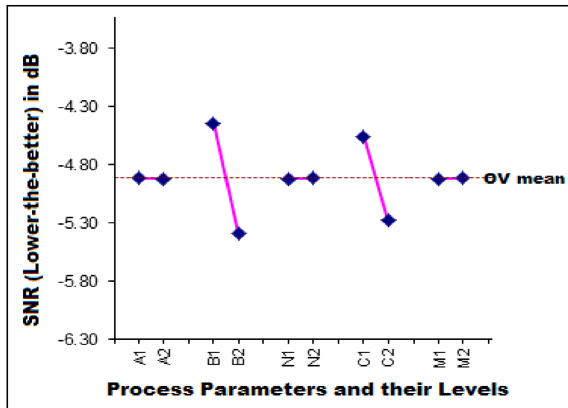


**Figure-4.** Factor effects graph for SNR (Lower-the-better).

For the interaction test analysis, both column 3 and column 5 in Table-11 are not utilized. However, the columns that represent the individual factors are used in the analysis. It can be observed that the column 1 of Table-11 indicates $A_1$ is contained in experiment row 1, 2, 3 and 4, while $B_1$ is in experiment row 1, 2, 5 and 6. However, the rows that contain both $A_1$ and $B_1$ are in experiment row 1 and 2. Therefore, the average SNR for $A_1B_1$ is computed from the results of experiment row 1 and 2.

The average effect of $\overline{A_1B_1}$ = (-4.92-4.44) / 2) = -4.44. The two corresponding experiment rows for $A_1B_2$ are row 3 and 4, hence the average effect of $\overline{A_1B_2}$ = (-4.92-5.40) / 2)) = -5.40. In the computations for $\overline{A_1B_1}$ and $\overline{A_1B_2}$ , factor level $A_1$ is fixed. The difference between the result for $\overline{A_1B_1}$ = -4.44 and $\overline{A_1B_2}$ = -5.40 is due only to factor B. By using similar method, $\overline{A_2B_1}$ , $\overline{A_2B_2}$ , $\overline{B_1C_1}$ , $\overline{B_1C_2}$ , $\overline{B_2C_1}$ and $\overline{B_2C_2}$ can be computed as well. The test of interaction for AxB and BxC are shown in Figure-5 and Figure-6 correspondingly. The intersection line in Figure-5 indicates that there is the interaction effect between A and B. Since, there is no intersection line Figure-6, it is concluded that there is no interaction effects between B and C. Therefore the optimal level for factor A, B and C are level $A_2$, $B_1$, $C_1$ as they produced the highest SNR.

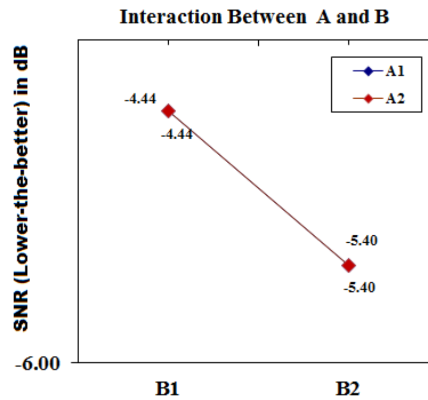


**Figure-5.** The interaction test for AxB.

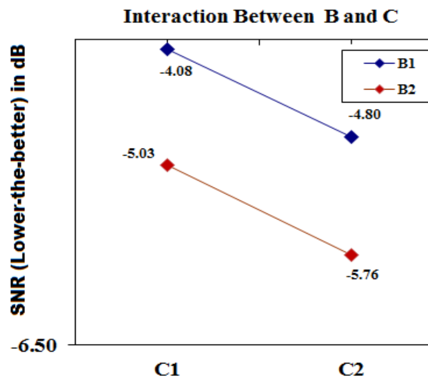


**Figure-6.** The interaction test for BxC.

**Analysis of variance (ANOVA)**

The ANOVA was implemented to identify the most significant process parameters that affected the DIBL value in the $WSi_x/TiO_2$ channel vertical double-gate NMOS device. The contribution of each process parameter was also revealed by computing the percentage of factor effect on SNR. Table-14 shows the results of pooled ANOVA.

The F-ratio were calculated based on 95% level of confidence. Factor B (halo implant dose) and factor C (halo implant energy) were the most dominant process parameters that contribute to lower DIBL value. Based on SNR analysis, interaction test and ANOVA, the optimal combination levels of process parameters for the lowest possible DIBL value were $A_2B_1$and $C_1$.

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**Table-14.** Results of ANOVA.

| Factor | DF | SSQ | MS | F-value | Factor effect on SNR (%) | Dominant/ Significant/ Neutral |
|---|---|---|---|---|---|---|
| A | 1 | 0 | 0 | 0 | 0 | Neutral |
| B | 1 | 1 | 1 | 8 | 48 | Dominant |
| N(AxB) | 1 | 0 | 0 | 0 | 0 | - |
| C | 1 | 1 | 1 | 4 | 27 | Dominant |
| M(BxC) | 1 | 0 | 0 | 0 | 0 | - |

**Verification test**

Verification test was conducted due to the optimal combination levels of process parameters, i.e. $A_2B_1C_1$ in the present study did not match any experiment of the orthogonal array in Table-11. The best combinational level setting of the process parameters for the $WSi_x/TiO_2$ channel vertical double-gate NMOS device predicted by Taguchi method is shown in Table-15.

The final procedure is to verify the decrease of DIBL value by simulating the device once again using the best level setting of the process parameters. The results of the final simulation of the device were recorded in Table-16.

**Table-15.** Overall best level setting of process parameters.

| Sym. | Process parameter | Units | Best Value |
|---|---|---|---|
| A | Substrate Implant Dose | atom/cm$^3$ | $1.03x10^{14}$ |
| B | Halo Implant Dose | atom/cm$^3$ | $2.82x10^{13}$ |
| C | Halo Implant Tilt | degree | 25 |

**Table-16.** Overall best level setting of process parameters.

| **DIBL** (mV/V) | | | | **SNR** (Higher-the-better) **in dB** |
|---|---|---|---|---|
| **DIBL$_1$** ($U_1V_1$) | **DIBL$_2$** ($U_1V_2$) | **DIBL$_3$ ($U_2V_1$)** | **DIBL$_4$** ($U_2V_2$) | |
| 1.552 | 1.675 | 1.566 | 1.605 | -4.08 |

The SNR for the device after the optimization approach was -4.08 dB. The value was within the predicted SNR range of -3.45 to -4.71 dB. The lowest possible DIBL value was observed to be 1.552 mV/V. Table-17 shows the comparison of DIBL values before the optimization, after optimization without the interaction test and after optimization with the interaction test. The final results after the optimization with the interaction test has produced the lowest DIBL value. There is a reduction of 29.8% in the DIBL value if compared to the DIBL value before optimization approach (2.168 mV/V). The DIBL value was observed to be further reduced by 12.02% by utilizing the optimization with the interaction test approach. The results have justified that the interaction test of Taguchi method is capable of figuring out the robust process recipe for a lower DIBL effect in vertical double $WSi_x$-based gate NMOS device.

**Table-17.** Comparison of the Results from Different Approaches

| Device characteristics | Before optimization | Optimization without the interaction test | Optimization with the interaction test |
|---|---|---|---|
| DIBL (mV/V) | 2.168 | 1.730 | 1.522 |

**CONCLUSIONS**

Based on the final results, it can be concluded that the DIBL value of the $WSi_x/TiO_2$ channel vertical double-gate NMOS device was successfully optimized by using both $L_{12}$ and $L_8$ orthogonal array of Taguchi method. The most dominant factors (process parameters) that were identified to contribute the most impact on the DIBL value are halo implant tilt angle and source/drain (S/D) implant where each of them contributes 24% and 16% of factor effect on SNR respectively.

The lowest DIBL value obtained from the Taguchi analysis without the interaction test was observed to be 1.730 mV/V. The DIBL value was observed to be further reduced down to 1.552 mV/V when the Taguchi analysis with the interaction test was applied. There is a slight reduction of 12.02% in the DIBL value compared to the result retrieved from the Taguchi analysis without the interaction test. The final results have justified that the interaction test of the Taguchi method was capable of finding the robust process recipe for lower DIBL value in $WSi_x/TiO_2$ channel vertical double-gate NMOS device.

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**ACKNOWLEDGEMENT**

The authors would like to thank to the Ministry of Higher Education (MOHE) and Faculty of Electronics and Computer Engineering (FKEKK), Universiti Teknikal Malaysia Melaka (UTeM) for sponsoring this study under the research grants (PJP/2014/FKEKK (6B)/S01341) and FRGS (RACE)/2012/FKEKK/TK02/02/2 F00148.

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