



Faculty of Electrical Engineering

**PERFORMANCE EVALUATION OF SPACE VECTOR
MODULATION (SVM) FOR MULTILEVEL INVERTERS**

Syamim Binti Sanusi

Master of Science in Electrical Engineering

2016

**PERFORMANCE EVALUATION OF SPACE VECTOR MODULATION (SVM)
FOR MULTILEVEL INVERTERS**

SYAMIM BINTI SANUSI

**A thesis submitted
in fulfillment of the requirements for the degree of Master of Science
in Electrical Engineering**

Faculty of Electrical Engineering

UNIVERSITI TEKNIKAL MALAYSIA MELAKA

2016

DECLARATION

I declare that this thesis entitled “Performance Evaluation of Space Vector Modulation (SVM) for Multilevel Inverters” is the result of my own research except as cited in the references. The thesis has not been accepted for any degree and is not concurrently submitted in candidature of any other degree.

Signature :

Name :

Date :

APPROVAL

I hereby declare that I have read this thesis and in my opinion this thesis is sufficient in terms of scope and quality for the award of Master of Science in Electrical Engineering.

Signature :

Supervisor Name :

Date :

DEDICATION

To my beloved mother, father and siblings

ABSTRACT

The Space Vector Modulation (SVM) technique has gained wide acceptance for many AC drive applications, due to a higher DC bus voltage utilization (higher output voltage compared with the Sinusoidal Pulse Width Modulation (SPWM)), lower harmonic distortions and easy digital realization. In recent years, the SVM technique was extensively adopted in multilevel inverters since it offers greater numbers of switching vectors for obtaining further improvements of AC drive performances. However, the use of multilevel inverters associated with SVM increases the complexity of control algorithm (or computational burden), in obtaining proper switching sequences and vectors. The complexity of SVM computation causes a microcontroller or digital signal processor (DSP) to execute the computation at a larger sampling time. This consequently may produce errors in computation and hence degrades the control performances of AC motor drives. This thesis reports the performance evaluation of SVM for two-level of VSI, three-level and five-level of Cascaded H-Bridge Multilevel Inverter (CHMI) and analyse in-depth the accuracy performances of SVM computation and the performance evaluation in variable speed drive systems (i.e. Direct Torque Control (DTC) using SVM). The SVM modulator is implemented using a hybrid controller approach, i.e. with combination between the DS1104 Controller Board and FPGA. In such way, the computational burden can be minimized as the SVM tasks are distributed into two parts, in which every part is executed by a single controller. This allows the generation of switching gates performed by FPGA at the minimum sampling time $DT_2 = 360 \text{ ns}$ to obtain precise desired output voltages, as verified via simulation and experimental results. Based on the accuracy performance analysis, it has revealed that the error of SVM computation in five-level inverter, even with a larger sampling time $DT_1 = 200 \mu\text{s}$, can be restricted at 6.25% from that obtained in two-level inverter. This allows the use of low-speed microcontroller or DSP to have satisfactory control performances, however, with the suggestion to use higher levels of inverters.

ABSTRAK

Teknik Modulasi Vektor Ruang (SVM) telah mencapai penerimaan yang luas bagi kebanyakan aplikasi pemacu ulang-alik AC, disebabkan penggunaan voltan arus terus DC yang lebih tinggi (keluaran voltan yang lebih tinggi berbanding dengan SPWM), herotan harmonik yang rendah dan memudahkan pembangunan perkakasan secara digital. Tahun-tahun kebelakangan ini, teknik SVM secara meluasnya telah digunapakai dalam penyongsang bertingkat kerana ia menawarkan bilangan pensuisan vektor yang banyak untuk mencapai lanjutan penambahbaikan bagi prestasi pemacuan AC. Walaubagaimanapun, penggunaan penyongsang bertingkat dikaitkan dengan SVM meningkatkan kerumitan bagi algoritma kawalan (atau beban pengiraan), dalam mendapatkan aturan dan vektor pensuisan yang baik. Kerumitan bagi pengiraan SVM mengakibatkan sebuah pengawal mikro atau pemproses isyarat digital (DSP) melaksanakan pengiraan pada pensampelan masa yang lebih tinggi. Ini seterusnya boleh menghasilkan ralat dalam pengiraan dan kemudiannya menurunkan prestasi kawalan bagi pemacu motor AC. Tesis ini melaporkan penilaian prestasi bagi SVM untuk dua-peringkatan penyongsang VSI, tiga-peringkatan dan lima-peringkatan CHMI dan analisa secara mendalam prestasi ketepatan bagi pengiraan SVM dan prestasi penilaian kawalan laju motor AC (iaitu Kawalan Langsung Dayakilas (DTC) menggunakan SVM). Pemodelat SVM dibangunkan menggunakan sebuah pendekatan pengawal hibrid, iaitu dengan kombinasi papan pengawal DS1104 dan FPGA. Dengan cara ini, beban pengiraan boleh diminimakan oleh kerana tugas SVM diagihkan kepada dua bahagian, yang mana setiap bahagian dilaksanakan oleh satu pengawal. Ini membenarkan penghasilan bagi get-get pensuisan yang dilakukan oleh FPGA pada pensampelan masa yang minimum $DT_2 = 360 \text{ ns}$ untuk mendapatkan kejituan keluaran voltan yang dikehendaki, seperti yang disahkan menerusi keputusan simulasi dan ujikaji. Berpandukan kepada analisa prestasi kejituan, ia telah mendedahkan bahawa ralat bagi pengiraan SVM dalam penyongsang lima peringkatan, walaupun dengan pensampelan masa yang besar $DT_2 = 200 \mu\text{s}$, boleh dihadkan pada 6.25% daripada yang diperolehi dalam penyongsang dua peringkatan. Ini membenarkan penggunaan bagi pengawal mikro atau DSP yang berkelajuan rendah untuk mempunyai kawalan prestasi yang memuaskan, tetapi dengan cadangan, kepada penggunaan penyongsang dengan peringkatan yang lebih tinggi.

ACKNOWLEDGEMENT

It is indeed a wonderful opportunity to thank and cheer for everyone who direct or indirect contributed towards the success of this thesis. First of all, I would like to express my gratitude to my supervisor Dr.Auzani bin. Jidin for the continuous support and help during work of the thesis. Without his precious advice and continuous support with patience it would be impossible for me to finish this project alone.

Next I would like to thanks to my lectures and my friends, especially to my colleagues from Power Electronics Design Group for their support and friendly atmosphere. I am greatly indebted to my family, who always stay by my side during my difficult times. Thanks for always giving an encouragement words and makes me did not easily give up. Furthermore, not to forget to everyone who involved me while finishing this research because been patient, supportive, understanding and shared the knowledge.

Above all, I thank Almighty Allah S.W.T for giving me this opportunity and strength to accomplish this task.

TABLE OF CONTENTS

	PAGE
DECLARATION	
APPROVAL	
DEDICATION	
ABSTRACT	i
ABSTRAK	ii
ACKNOWLEDGEMENT	iii
TABLE OF CONTENT	iv
LIST OF TABLE	vii
LIST OF FIGURES	viii
LIST OF APPENDICES	xii
LIST OF ABBREVIATIONS	xiii
LIST OF PUBLICATIONS	xvii
LIST OF ACHIVEMENTS	xviii
CHAPTER	
1. INTRODUCTION	1
1.1 Research Background	1
1.1.1 Significance of Research	3
1.2 Problem Statements	4
1.3 Objectives of Research	7
1.4 Scopes of Work	7
1.5 Research Methodology	7
1.6 Thesis Contributions	9
1.7 Thesis Outlines	10
1.8 Conclusion	11
2. OVERVIEW OF SWITCHING MODULATION STRATEGIES FOR VOLTAGE SOURCE INVERTERS	12
2.1 Introduction	12
2.2 Voltage Source Inverter (VSI) and Current Source Inverter (CSI)	12
2.3 Two-Level Three-Phase Voltage Source Inverter	18
2.3.1 Carrier-Based Sinusoidal Pulse Width Modulation (PWM)	19
2.3.2 Third Harmonic Injection Carrier-Based PWM	21
2.3.3 Carrier-Based PWM with Offset Addition	24
2.3.4 Space Vector PWM	26
2.4 Multilevel Inverters	29
2.4.1 Carrier-Based Sinusoidal Pulse Width Modulation (PWM)	32
2.4.2 Space Vector PWM	35
2.5 The Advantages of using SVM in Electrical Drive Systems	37
2.6 The Most Popular Application of SVM	41
2.7 Conclusion	43

3.	RESEARCH METHODOLOGY	44
3.1	Introduction	44
3.2	Space Vector Modulation for Two-Level Inverter	45
3.2.1	Simplified Two-Level Inverter Circuit	45
3.2.2	Mapping of Voltage Vector	47
3.2.3	Determination of Sector	51
3.2.4	Calculation of Angle within a Sector (θ_{si})	53
3.2.5	Calculation of On-Duration for Switching Vectors	57
3.2.6	Calculation of Duty Ratios	59
3.2.7	Generation of Switching States	63
3.2.8	Complete Control Structure of SVM for 2-level Inverter	65
3.3	Space Vector Modulation for 3-Level Cascaded H-Bridge Multilevel Inverters	68
3.3.1	Topology of Three-Level Cascaded H-Bridge Multilevel Inverter	68
3.3.2	Mapping of Vectors	70
3.3.3	Determination of Sector and Triangle	71
3.3.4	Calculation of On-Duration for Switching Vectors	78
3.3.5	Calculation of Duty Ratios	79
3.3.6	Generation of Switching States	79
3.3.7	Complete Control Structure of SVM for 3-level CHMI	83
3.4	Space Vector Modulation for 5-Level Cascaded H-Bridge Multilevel Inverter	86
3.5	Simulation Model of Space Vector Modulation	88
3.6	Description of Experimental Setup	97
3.6.1	DS1104 R&D Controller Board	97
3.6.2	Altera FPGA DEO Controller Board	101
3.6.3	Power Inverter and Gate Driver Circuits	103
3.6.4	Three-Phase and Series Connected Resistive and Inductive Loads	105
3.6	Conclusion	106
4.	RESULTS AND DISCUSSION	107
4.1	Introduction	107
4.2	Analysis of Accuracy	107
4.2.1	Evaluation of Accuracy Performance at Different Sampling Times	118
4.2.2	Evaluation of Accuracy Performance at Different Levels of Inverters	111
4.2.3	Evaluation of Accuracy Performance at Different Modulation Indices	117
4.3	Analysis of Performances of AC Motor Control	119
4.4	Analysis of Total Harmonic Distortion (THD) of Output Voltage	122
4.5	Conclusion	127

5.	CONCLUSION AND RECOMMENDATION	128
5.1	Conclusion	128
5.2	Recommendation	129
	REFERENCES	131
	APPENDICES A	142
	APPENDICES B	177
	APPENDICES C	209

LIST OF TABLES

TABLE	TITLE	PAGE
3.1	Look-Up Table for Mapping the Switching State.	63
3.2	List of Tasks for each Part in SVM of Two-Level Inverter	66
3.3	Look-Up Table for Mapping the Switching States ($S_{a1}S_{a2}S_{b1}S_{b2}S_{c1}S_{c2}$)	81
3.4	List of Tasks for each Part in SVM of Three-Level CHMI	84
3.5	Load Reactor Parameters	105
4.1	Numerical and Parameter Values used in SVM Computation for Mapping All the Vectors in Fig. 4.3 for (a) Two-Level Inverter (b) Three-Level CHMI and (c) Five-Level CHMI	115

LIST OF FIGURES

TABLE	TITLE	PAGE
1.1	Structure of DTC-SVM (as Proposed in (Lascu et al., 2000)	3
1.2	Simulation Results of Torque, Flux and Phase Voltage	6
2.1	Comparison of VSI and CSI in a Single-Phase Inverter, (a) Single-Phase Inverter Circuit, (b) Switching Gate Circuit, and (c) Simulation Results	15
2.2	Complexity of Control Structure in FOC of Induction Motor with the inclusion of CSI (as Proposed in (Xu and Novotny, 1992))	17
2.3	A Three-Phase Voltage Source Inverter (VSI)	18
2.4	Carrier-Based Sinusoidal Pulse Width Modulation (PWM) : (a) Implementation of Block Diagram (b) Simulation Results	20
2.5	Third Harmonic Injection Carrier-Based PWM: (a) Implementation of Block Diagram (b) Simulation Results	23
2.6	Carrier-Based PWM with Offset Addition : (a) Implementation of Block Diagram (b) Simulation Results	25
2.7	Space Vector PWM : (a) Phasor Diagram of \vec{v}_s^* (b) Switching Pattern for Mapping \vec{v}_s^* using Symmetrical SVM and Discontinuous SVM Approaches	28
2.8	Topologies of Multilevel Inverters for (a) Diode Clamped or Neutral Point Clamped, (b) Capacitor Clamped or Flying Capacitor and (c) Cascaded H-Bridge Multilevel Inverters	31
2.9	Carrier-Based SPWM for a Five-Level Multilevel Inverter : (a) IPD, (b) POD, and (c) APOD	34
2.10	Comparison Between (a) Two-Level Space Vector Diagram and (b) Three-Level Space Vector Diagram, e.g. for Sector I.	36
2.11	Comparison Between (a) Two-Level Space Vector Diagram	40

	and (b) Three-Level Space Vector Diagram, e.g. for Sector I.	
2.12	Structure of DTC-SVM (as Proposed in (Lascu et al., 2000))	42
3.1	Schematic diagram of Two-Level of Voltage Source Inverter (VSI)	46
3.2	Equivalent Circuit of the Inverter Shown in Fig. 3.1 (e.g. <i>a</i> -Phase Leg)	47
3.3	Mapping of Unit Vectors	48
3.4	Definition of Space Voltage Vector on the <i>d-q</i> Voltage Vector Plane	50
3.5	Voltage Vectors in the Two-Level Inverter Obtained in (3.10) and (3.11) for Every Switching State Possibility ($S_a S_b S_c$)	51
3.6	Definition of Angle within a Sector (θ_{si}) and the Switching Sequence and General Representation for Sector I	54
3.7	Definition of Angle within a Sector (θ_{si}) and the Switching Sequence and General Representation for (a) Sector I, (b) Sector II, (c) Sector III, (d) Sector IV, (e) Sector V, and (f) Sector VI	56
3.8	General Representation of Vector Diagram for Any Sector	57
3.9	Implementation of Space Vector Modulation using Two Sampling Times (a) Block Diagram (b) Typical Waveforms	61
3.10	Generation of Pre-Switching States	62
3.11	Generation of Switching Status (S_a , S_b and S_c) based on the Pre-Switching States and Duty Ratios for (a) Sector I, (b) Sector II, (c) Sector III, (d) Sector IV, (e) Sector V, and (f) Sector VI	64
3.12	Complete Block Diagram of SVM for 2-Level Inverter.	67
3.13	Topology Circuit of Three-Level Cascaded H-Bridge Multilevel Inverter	69
3.14	Simplified Three-Level H-Bridge Inverter (for any Phase)	69
3.15	Voltage Vectors in the Three-Level CHMI Obtained in (3.35) and (3.36) for Every Switching State Possibility	71

	($S_{a1}S_{a2}S_{b1}S_{b2}S_{c1}S_{c2}$)	
3.16	Definition of Triangle ($\Delta_j = \Delta_0, \Delta_1, \Delta_2$ and Δ_3) for Every Sector	73
3.17	Definition of Reference Voltage Vector for Every Triangle ($\Delta_0, \Delta_1, \Delta_2$ and Δ_3)	75
3.18	Determination of Triangular ($\Delta_0, \Delta_1, \Delta_2$ and Δ_3) for Every Sector	77
3.19	Generation of Switching Status ($S_{a1}, S_{a2}, S_{b1}, S_{b2}, S_{c1}$ and S_{c2}) based on the Pre-Switching States and Duty Ratios for Sector I in Every Triangle (a) Δ_1 , (b) Δ_2 , (c) Δ_3 and (d) Δ_4 .	82
3.20	Complete Block Diagram of SVM for Three-Level CHMI	85
3.21	Topology Circuit of Five-Level Cascaded H-Bridges Multilevel Inverter	87
3.22	Simplified Three-Level H-Bridge Inverter (for any Phase)	87
3.23	Definition of Triangle ($\Delta_j = \Delta_0, \Delta_1, \Delta_2, \dots, \Delta_{15}$) for Every Sector	88
3.24	Simulation Model of Space Vector Modulation (SVM) (e.g. for Three-Level CHMI)	90
3.25	Simulation Model of Three-Phase Generator (at <i>Subsystem1</i>)	91
3.26	Simulation Model of Three- to Two-Phase Transformation (at <i>Subsystem2</i>)	92
3.27	Simulation Model of Duty Ratios Calculator (at <i>Subsystem3</i>)	93
3.28	Simulation Model of Pre-Switching States Generator (at <i>Subsystem4</i>)	94
3.29	Simulation Model of Power Inverter Circuits for (a) Two-Level, (b) Three-Level, and (c) Five-Level	95
3.30	Experimental Setup	99
3.31	The Real-Time Interface (RTI) I/O Blocks Inserted into a Simulink Block Diagram which Connect the Function Model with the I/O Interfaces	100
3.32	Block Diagram of Blanking Time Generation for x -Phase and Any Leg	102
3.33	Timing Diagram of Blanking Time Generation for x -Phase and Any Leg	103
3.34	Photograph of FPGA, Gate Driver Circuits and Cascaded	104

	H-Bridge Multilevel Inverter (CHMI), e.g. for Five-Level	
3.35	Terco MV 1101 Load Reactor	105
4.1	Comparison of On-Duration or Pulse Width of Pre-Switching States For Different Sampling Times (a) $DT_2 = 1 \mu s$, (b) $DT_2 = 20 \mu s$ and (c) $DT_2 = 50 \mu s$	110
4.2	Region of Possible Location of Resultant Voltage Vector \bar{v}_s due to Inappropriate On-Duration for (a) Two-Level, (b) Three-Level and (c) Five-Level	113
4.3	Simulation Results of Resultant Voltage Vector \bar{v}_s for a given \bar{v}_s^* when Different Sampling Times $DT_2 = 1 \mu s$, $20 \mu s$ and $50 \mu s$ are Applied for (a) Two-Level, (b) Three-Level and (c) Five-Level Inverters	116
4.4	Comparison between Calculation and Simulation Results when $M_i = 0.9, 0.6$ and 0.3 for (a) Two-Level, (b) Three-Level and (c) Five-Level Inverters	118
4.5	Performance Analysis of AC Motor Control at Different Sampling Times DT_2 , for (a) Two-Level, (b) Three-Level and (c) Five-Level Inverters	121
4.6	Simulation and Experimental Results of Phase Voltage and its Frequency Spectrum when Modulation Index $M_i = 0.3$ for (a) Two-Level, (b) Three-Level and (c) Five-Level Inverters	124
4.7	Simulation and Experimental Results of Phase Voltage and its Frequency Spectrum when Modulation Index $M_i = 0.6$ for (a) Two-Level, (b) Three-Level and (c) Five-Level Inverters	125
4.8	Simulation and Experimental Results of Phase Voltage and its Frequency Spectrum when Modulation Index $M_i = 0.9$ for (a) Two-Level, (b) Three-Level and (c) Five-Level Inverters	126

LIST OF APPENDICES

APPENDIX	TITLE	PAGE
A	MATLAB Function Source Code Listings	147
B	VHDL Source Code Listing	177
C	Simulation Model of Direct Torque Control Space Vector Modulation (DTC-SVM) with Cascaded H-Bridge Multilevel Inverter	209

LIST OF ABBREVIATIONS

DTC	-	Direct torque control
IM	-	Induction motor
VSI	-	Voltage source inverter
SPWM		Sinusoidal pulse width modulation
FOC	-	Field oriented control
DSC	-	Direct self control
DT	-	Sampling period
AC	-	Alternating current
DC	-	Direct current
UPS	-	Uninterruptible power supply
CSI	-	Current source inverter
HVDC	-	High voltage direct current
MOSFET	-	Metal oxide semiconductor field effect transistor
DSP	-	Digital signal processor
ADC	-	Analog digital converter
DAC		Digital analog converter
FPGA	-	Field programmer gate array
SVM	-	Space vector modulated
UB	-	Upper band
LB	-	Lower band
IGBT	-	Insulated gate bipolar transistor
CHMI	-	Cascaded H-bridge multilevel inverter
NPCMI	-	Neutral point clamp multilevel inverter
FCI	-	Flying capacitor inverter
PWM	-	Pulse width modulator
THD	-	Total harmonic distortion
PI	-	Proportional integral
IPD	-	In-phase disposition

POD	- Phase opposition disposition
APOD	- Alternate phase opposition disposition
DTC-SVM	- Direct torque control space vector modulation
\bar{v}_s^*	- Reference voltage vector
v_{sd}^*, v_{sq}^*	- d and q components of the stator voltage in stationary reference frame
d, q	- Direct and quadrature of the stationary reference frame
v_m^*	- Voltage modulating signal
v_{tri}	- Triangular wave frequency
V_{l1}	- Desired fundamental output voltage
i	- Load current
i^*	- Current reference
$v_{aM}^*, v_{bM}^*, v_{cM}^*$	- Three phase sinusoidal voltage
M_i	- Modulation index
T	- Switching period
t	- On times duration
L	- Number of level
$V_{1,six-step}$	- Fundamental output of six-step voltage
\emptyset	- Phase shifts in inverter levels
θ_s	- Angle of reference voltage
θ_{si}	- Angle within Sector
d^r, q^r	- Real and imaginary and real of the rotor
i_s, i_r	- Stator and rotor current space vector in stationary reference frame
R_r, R_s	- Rotor and stator resistance
L_s	- Stator self-inductance
L_r	- Rotor self-inductance
L_m	- Mutual inductance
$\bar{\varphi}_s, \bar{\varphi}_r$	- Stator and rotor flux linkage space vector in reference frame
i_{rd}, i_{rq}	- d and q components of the rotor current in stationary reference frame
i_{sd}, i_{sq}	- d and q components of the stator current in stationary reference

	frame
v_{sd}, v_{sq}	- d and q-axis of the stator voltage in stationary reference frame
$\varphi_{sd}, \varphi_{sq}$	- d and q components of the stator flux in stationary reference frame
\bar{v}_s	- Voltage vectors
n	- Numbers of phase
i_a, i_b, i_c	- Current phase a,b and c
L	- Self-inductance
T_e	- Electromagnetic Torque
T_e^*	- References of torque
ε_T	- Output torque error
σ_T	- Output torque status
θ_r	- Angle within a sector
$v_{s\alpha}^*, v_{s\beta}^*$	α - and β -axis component of stator voltage
\bar{v}_{s0}^*	Voltage vector reference based on α_o - and β_o -axis plane
$v_{\alpha o}^*, v_{\beta o}^*$	α - and β -axis component of stator voltage of triangles
δ_{sr}	- Different angle between stator flux linkage and rotor flux linkage
V_{dc}	- DC link voltage
P	- Pairs of pole
ω_r	- Rotor electrical speed in rad/s
v_{dc}	- DC link voltage
ε_φ	- Output flux error
φ_s^*	- References of flux
φ_s	- Flux estimate
σ_φ	- Output flux status
σ	- Total flux leakage factor
S_{sa}, S_{sb}, S_{sc}	Pre-switching State
\bar{v}_{xN}	- Inverter phase voltage
v_{xN}	- Phase stator voltages
S_x	Switch gate
\bar{S}_x	Complementary switch gate

Δ_j	Number of triangle
\bar{v}_x	Voltage vector
si	Number of Sector
d_x	Phase duty ratio

LIST OF PUBLICATIONS

Journal Paper

Syamim Sanusi, Auzani Jidin, Tole Sutikno, Kasrul Abdul Karim, Mohd Luqman Mohd Jamil, Siti Azura Ahmad Tarusan," Implementation of Space Vector Modulator for Cascaded H-Bridge Multilevel Inverters", *International Journal of Power Electronic and Drive System (IJPEDS)*, Vol. 6, No. 4, December 2015, pp. 906~918., ISSN: 2088-8694.

Published Conference Proceeding

Syamim Sanusi, Zulkifli Ibrahim, Auzani Jidin , Mohd Hatta Jopri, Kasrul Abdul Karim, Md Nazri Othman " Implementation of Space Vector Modulation for Voltage Source Inverter," *Electrical Machines and Systems (ICEMS), 2013 International Conference on, 26-29 Oct. 2013*

Zulkifilie Bin Ibrahim, Md. Liton Hossain, **Syamim Binti Sanusi**, Nik Munaji Bin Nik Mahadi, Ahmad Shukri Abu Hasim, " Performance of Different Topologies for Three Level Inverter Based on Space Vector Pulse Width Modulation Technique," in *Clean Energy and Technology (CEAT) 2014, 3rd IET International Conference on. 2014*

Adeline Lukar Herlino, Auzani Jidin, Che Wan Faizal bin Che Wan Mohd Zalani, **Syamim Sanusi**, M.H Jopri, Mustafa Manap, " Comparative Study of Current Control Strategy for DC Motors," *Power Engineering and Optimization Conference (PEOCO), 2013 IEEE 7th International on, 3-4 June 2013.*

LIST OF ACHIVEMENTS

Exhibition and Award

Awarded UTeMEX 2013 **Gold medal** for the invention “PRO-SINE” at Expo Penyelidikan Dan Inovasi Utem 2012 (UtemEX) on 12 Dec 2013 , at Main Hall Utem.

Awarded UTeMEX 2014 **Bronze medal** for the invention “PRO-SINE” at Malaysia Technology Expo on 20-22 Feb 2014 , at PWTC, Kuala Lumpur.

CHAPTER 1

INTRODUCTION

1.1 Research Background

Voltage Source Inverters (VSI) have evolved as the most popular power conversion for many AC drive applications. The evolution of VSI is in line with the development of various Pulse Width Modulation (PWM) algorithms supported by the advent of solid state switching device technologies, fast digital signal processors, Field Programmable Gate Arrays (FPGA) and microcontrollers. Since a few decades ago, several PWM algorithms were developed to improve some performances of VSI such as high-power efficiency (Abu Bakar Siddique et al., 2015, Edpuganti and Rathore, 2015, Tong et al., 2015, Youssef et al., 2016), high-output voltage (Carrasco and Silva, 2013, Chai et al., 2016, Jana et al., 2013), and low-total harmonic distortion (THD) (Pramanick et al., 2015, Prieto et al., 2014). Apparently, the research about VSI has not reach to state of saturation up till now, as novel or simplified PWM methods is still continue to emerge for various topology inverter circuits and multilevel inverters (Gupta et al., 2016, Liu et al., 2016, Lopez et al., 2016, Narimani et al., 2016, Sakthisudhursun et al., 2016, Tan et al., 2016, Yi et al., 2016)]. Among various modulation strategies or PWM methods, the Space Vector Modulation (SVM) technique has received wide acceptance due to several advantages such as higher output voltages, lower THD, high-efficiency and flexible to be implemented in vector control systems (Chai et al., 2016, Kai et al., 2016, Liu et al., 2016, Thomas et al., 2015, Zheng et al., 2016, Zhifeng et al., 2010).