

Faculty of Electrical Engineering

HARMONICS MINIMIZATION OF A THREE PHASE CASCADED H-BRIDGE MULTILEVEL INVERTER

Afiqah Binti Sabari

Master of Science in Electrical Engineering

2016

C Universiti Teknikal Malaysia Melaka

HARMONICS MINIMIZATION OF A THREE PHASE CASCADED H-BRIDGE MULTILEVEL INVERTER

AFIQAH BINTI SABARI

A thesis submitted in fulfillment of the requirements for the degree of Master of Science in Electrical Engineering

Faculty of Electrical Engineering

UNIVERSITI TEKNIKAL MALAYSIA MELAKA

2016

C Universiti Teknikal Malaysia Melaka

DECLARATION

I declare that this thesis entitled "HARMONICS MINIMIZATION OF A THREE PHASE CASCADED H-BRIDGE MULTILEVEL INVERTER" is the result of my own research except as cited in the references. The thesis has not been accepted for any degree and is not concurrently submitted in candidature of any other degree.

Signature	:	
Name	:	Afiqah Binti Sabari
Date		:

APPROVAL

I hereby declare that I have read this thesis and in my opinion this thesis is sufficient in terms of scope and quality as a partial fulfillment of Master of Science in Electrical Engineering.

Signature

:....

Supervisor Name

:Assoc Prof Ir Dr Rosli Bin Omar

Date

•

DEDICATION

To my beloved mother and father

"I am only one, but I am one. I cannot do everything, but I can do something. What I can do I ought to do. And what I ought to do by the bless of ALLAH, I will do"



ABSTRACT

For more than two decades, multilevel inverter technology has drawn tremendous interest among researchers from industry and academia in recent years due to its superior performance. In this regards, the main objectives of this this thesis are to study, modeling, design and develop a prototype of a three-phase cascaded H-Bridge Multilevel inverter (CHB-MLI) based on Newton-Raphson technique that aims to analyze the performance of the inverter output for harmonic minimization. The source codes programming based on Newton-Raphson method was developed, and then stored into the Digital Signal Processing (DSP) TMS320F2812. The proposed controller based on Newton Raphson was applied to CHB-MLI. The optimization of this system had managed to minimize the harmonic contents of the inverter output. Besides, the experimental results of the developed prototype are discussed. In addition, the performance of the proposed system was compared between simulation and experimental results for both Optimization and Non-optimization techniques. The Optimization of this system had been capable in reducing the harmonic contents of the inverter output. Thus, optimization and Non-optimization of the CHB-MLI system had been successfully demonstrated in this study. Finally the development of a three phase CHB-MLI based on DSP, its controller and power electronic devices would be a challenging future research in minimize the content of harmonic of the inverter output.

i

ABSTRAK

Selama lebih dua dekad, teknologi penyongsang pelbagai peringkat telah menarik minat hebat sekali dalam kalangan para penyelidik dari industri dan ahli akademik sejak tahun kebelakangan ini akibat prestasinya yang unggul. Dalam konteks ini, objektif utama tesis ini untuk kajian, permodelan, rekabentuk dan membangunkan sebuah prototaip yang Jambatan-H Jujukan Berbilang Aras Litar Penyongsang (JHJ-BALP) untuk tiga fasa berdasarkan teknik Newton Raphson yang bertujuan untuk menganalisa prestasi litar penyongsang bagi pengurangan pengeluaran harmonik. Sumber kod pengaturcaraan berasaskan kaedah Newton Raphson telah dibangunkan, dan kemudian disimpan ke dalam Pemprosesan Isyarat Digital (PID) TMS320F2812. Pengawal yang dicadangkan adalah berdasarkan Newton Raphson dan ia digunakan untuk (JHJ-BALP). Pengoptimuman sistem ini telah berjaya untuk mengurangkan pengeluaran kandungan penyongsang harmonik . Selain itu, keputusan ujian prototaip dibangunkan juga telah dibincangkan. Di samping itu, prestasi sistem yang dicadangkan adalah dibanding antara simulasi dan uji kaji bagi memperoleh keputusan teknik pengoptimuman dan tidak-pengoptimuman. Pengoptimuman sistem ini telah berupaya mengurangkan kandungan keluaran penyongsang harmonik. Oleh itu, pengoptimuman dan tidak-pengoptimuman sistem (JHJ-BALP) telah berjaya dibuktikan dalam kajian ini. Akhirnya pembangunan tiga fasa (JHJ-BALP) berdasarkan (PID), pengawal dan peranti elektronik kuasa memberi cabaran dalam penyelidikan masa hadapan bagi mengurangkan kandungan pengeluaran penyongsang harmonik.

ACKNOWLEDGMENT

All praises be to Allah S.W.T, The Most Gracious, The Most Merciful for Guidance and Blessing. First of all, I would like to express my gratitude and special thanks to my supervisor and also my advisor Assoc Prof Ir Dr Rosli Bin Omar. I cannot say thank you enough for his tremendous support and help. I am very grateful for the opportunity to continue my study through a project he gave to me. Without his encouragement and guidance, this thesis would not materialize. An addition, thanks to Mr Azhar Bin Ahmad for his interest in this work and holding the post of my co-supervisor in this research. I am also very thankful to UTeM for sponsoring this research through the Malaysian Technical University Network (MTUN) with research Project Code: MTUN/2012/UTeM-FKE/4 M00012 and Fundamental Research Grant Scheme (FRGS) with research Project Code: FRGS(RACE)/2012/FKE/TK02/02/1 F00151 belonging to my Principal Supervisor. Other than that, I feel a deep sense of gratitude to my parents, Sabari Bin Siraj and Siti Marpungah Bt Sipon because for their encouragement and moral support during my studies at Universiti Teknikal Malaysia Melaka (UTeM). Last but not least, I would like to take this opportunity to express my gratitude to the people who have given me support in the successful to complete this research project.

TABLE OF CONTENTS

DECLARATION	
APPROVAL	
DEDICATION	
ABSTRACT	i
ABSTRAK	ii
ACKNOWLEDGEMENTS	iii
TABLE OF CONTENTS	iv
LIST OF TABLES	vii
LIST OF FIGURES	viii
LIST OF ABBREVIATIONS	XV
LIST OF SYMBOLS	xvi
LIST OF PUBLICATIONS	xvii

CHAPTER

1.	IN	TROD	UCTION	1
	1.1	Backg	round	1
	1.2	Proble	em Statement	2
	1.3	Object	tives of Research	4
	1.4	Motiv	ation of Research	4
	1.5	Scope	of the Research	5
	1.6	Contri	butions of the Research	6
	1.7	Thesis	Organization	6
2.	LIT	ERATI	URE REVIEW	8
	2.1	Introd	uction	8
	2.2	Multil	evel Inverter Topologies	8
		2.2.1	Diode-Clamped Multilevel Inverter	8
		2.2.2	Flying Capacitor Multilevel Inverter	12
		2.2.3	Cascaded H-Bridge Multilevel Inverter	15
		2.2.4	Advantages and Disadvantages of Multilevel Inverters	20
	2.3	The co	oncept of Harmonics Theory	22
		2.3.1	Definition of Total Harmonics Distortion	24
	2.4	Harmo	onic Sources	25
		2.4.1	Effect of Harmonic	26
		2.4.2	Harmonic Measurement	26
		2.4.3	Harmonic Spectrum	27
	2.5	Types	of Controllers and Modulations used in (MLI)	28
		2.5.1	Selective Harmonic Elimination Technique (PWM)	28
		2.5.2	Space Pulse Width Modulation	30
		2.5.3	Space Vector Pulse Width Modulation	31
	2.6	Summ	lary	36

2.6 Summary

3.	PRO)JECT	METHC	DOLGY	37
	3.1	Introd	uction		37
	3.2	Flow	chart of th	e project	37
		3.2.1	Stage 1		39
		3.2.2	Stage 2		39
			3.2.2.1	Construction of the Proposed CHB-MLI Scheme	39
			3.2.2.2	Simulation Model of the Three-Phase CHB-MLL based on MATLAB/SIMULINK	41
			3.2.2.3	Tuning Parameters of the Newton-Raphson Controller	44
		3.2.3	Stage 3		45
			3.2.3.1	Gate Drive for Switching the IGBT	45
			3.2.2.2	Printed Circuit Board (PCB) Fabrication Process Five-level (MLI)	47
			3.2.2.3	Three-phase Five-level CHB-MLI hardware	48
			3.2.2.4	Implementation of Controller Hardware Using	50
			~ .	Digital Signal Processor (DSP TMS320F2812)	
		3.2.4	Stage 4		55
	2.2	3.2.5	Stage 5		55
	3.3	Fourie	er Series		55
	3.4	Mathe	matical 1	echnique of Switching via Newton-Raphson	56
	3.5	A Har	dware Pro	btotype of a Three-phase 5-level CHB-MLI	55
	3.6	Protot	ype Deve	lopment of a Three-phase Experiment Circuits.	60
	3.7	Summ	nary		61
4.	RES	SULT A	AND DIS	CUSSION	62
	4.1	Simul	ation of C	HB-MLI	62
		4.1.1	Simulati Five-Le	ion Results for Optimization of a Three-Phase vel CHB-MLI model with mi=0.84	63
		4.1.2	Simulati Phase Fi	ion Results for Non-Optimization of a Three ive-Level CHB-MLI model with mi=0.68	70
		4.1.3	Simulati Phase Fi	ion Results for Non-Optimization of a Three ive-Level CHB-MLI model with mi=0.58	76
		4.1.4	Simulati Phase Fi	ion Results for Non-Optimization of a Three ive-Level CHB-MLI model with mi=0.48	82
		4.1.5	Simulati Phase Fi	ion Results for Non-Optimization of a Three ive-Level CHB-MLI model with mi=0.90	88
	4.2	Exper	imental R	esults of Three-Phase CHB MLI	94
		4.2.1	Optimiz Five-Le	ation Experimental Results a Three-Phase vel CHB-MLI with mi=0.84	95
		4.2.2	Non-Op Phase Fi	timization Experimental Results a Three ive-Level CHB-MLI with mi=0.68	102
		4.2.3	Non-Op Phase Fi	timization Experimental Results a Three ive-Level CHB-MLI with mi=0.58	108
		4.2.4	Non-Op	timization Experimental Results a Three	115

			Phase Five-Level CHB-MLI with mi=0.48	
		4.1.5	Non-Optimization Experimental Results a Three	121
	4.4	a	Phase Five-Level CHB-MLI with mi=0.90	107
	4.1	Sumn	hary	127
5.	CO	NCLUS	SION AND RECOMMENDATIONS	128
	FOI	R FUTI	URE RESEARCH	
	5.1	Introd	luction	128
	5.2	Concl	usion	128
	5.3	Autho	or's Contribution	129
	5.4	Future	e Works	130
RF	EFER	ENCE	S	131
AF	PEN	DICES		137
AF	PEN	DIX A	Datasheet Optocoupler HCPL 310A	137
AF	PEN	DIX B	Schematic Circuit	140
AF	PEN	DIX C	I - Source Code (0.84)	141
			II - Source Code (0.68)	146
			III- Source Code (0.58)	150
			IV -Source Code (0.48)	155
			V Source Code (0.90)	159

LIST OF TABLES

TABLE	TITLE	PAGE
2.1	Switching pattern for three-level diode-clamped inverter	11
2.2	Switching pattern for a five-level diode-clamped multilevel inverter	11
2.3	Switching Pattern: A five-level FC inverter	14
2.4	Switching vector pattern, phase voltages, and output	35
	line-to-line voltages	
3.1	List of the components for the IGBT gate drive	46
3.2	Switching Pattern for Five-Level Inverter	59
4.1	Results of THDv and THDi Optimization and Non- Optimization	92
	by Simulation	
4.2	Results of THDv and THDi Optimization and Non- Optimization	125
	by Hardware Experimental	

LIST OF FIGURES

FIGURE	TITLE	PAGE
2.1	Three-level diode-clamped inverter	10
2.2	Five-level diode-clamped multilevel inverter	10
2.3	A three-level FC inverter	13
2.4	A five-level FC inverter	13
2.5	An H-bridge multilevel inverter	15
2.6	Repeated zero-level switching pattern.	16
2.7	Swapped zero-level switching pattern	17
2.8	Phase output voltage waveforms of a five-level topology	18
	CHB-MLI with two separate DC sources.	
2.9	(a) Separated fundamental and harmonic waveforms,	23
	and (b) waveform resulting from summation	
2.10	Harmonic spectrum	28
2.11	A three-phase power-source inverter circuit	32
2.12	The voltage space vector and its components dq plane	34
3.1	Flowchart of the proposed methodology	38
3.2	The Proposed Topology of a Three-Phase CHB-MLI	40
3.3	MATLAB/SIMULINK 7.120 (R2012a)	42
3.4	Five-Level CHB- MLI Model	43
3.5	Current Measurement Five-Level CHB- MLI Model.	44
3.6	Switching Block model.	44
3.7	The design and the construction of the gate drive with CHB-MLI	46
3.8	The Development of a single-phase CHB-MLI	49

viii

3.9	The Development of a three-phase CHB-MLI	49
	with star connection load	
3.10	Digital Signal Processor (DSP) TMS 320F2812	50
3.11	TMS320F2812 Architecture	51
3.12	Switching pattern (5V)	52
3.13	Switching pattern (15V)	53
3.14	Switching pattern for S1, S2, S3 and S4 (15V)	54
3.15	Switching pattern for S5, S6, S7 and S8 (15V)	54
3.16	The Overall Experimental set-up for the Prototype of Five-Level	61
	CHB MLI Inverters.	
4.1	Upper Switches Timing Diagram for S1, S2, S3, and S4 at	64
	phase A with mi=0.84 for Θ_1 =17.060 and Θ_2 =43.530.	
4.2	Lower Switches Timing Diagram for S5, S6, S7, and S8 at	64
	phase A with mi=0.84 for Θ_1 =17.060 and Θ_2 =43.530.	
4.3	Upper Switches Timing Diagram for S1, S2, S3, and S4 at	65
	phase B with mi=0.84 for Θ_1 =17.060 and Θ_2 =43.530.	
4.4	Lower Switches Timing Diagram for S5, S6, S7, and S8 at	65
	phase B mi=0.84 for Θ_1 =17.060 and Θ_2 =43.530.	
4.5	Upper Switches Timing Diagram for S1, S2, S3, and S4 at	66
	phase C mi=0.84 for Θ_1 =17.060 and Θ_2 =43.530.	
4.6	Lower Switches Timing Diagram for S5, S6, S7, and S8 at	66
	phase C with mi=0.84 for Θ_1 =17.060 and Θ_2 =43.530.	
4.7	Output Optimization Phase Voltage 5-level inverter based	67
	of 5-level CHB-MLI with mi=0.84.	
4.8	Optimization Harmonic spectrum for voltage waveform output	68
4.9	Optimization Current Waveform Output of 5-level CHB-MLI	69
4.10	Optimization harmonic spectrum for current waveform output	70
	of 5-level of CHB-MLI with mi=0.84.	
4.11	Upper Switches Timing diagram for S1, S2, S3, and S4 at	71
	phase A with mi=0.68 for θ_1 =8.7740 and θ_2 =68.1550.	
4.12	Lower Switches Timing Diagram for S5, S6, S7, and S8 at	71

	phase A with mi=0.68 for θ_1 =8.7740 and θ_2 =68.1550.	
4.13	Upper Switches TiMIng Diagram for S1, S2, S3, and S4 at	72
	phase B with mi=0.68 for Θ_1 =8.7740 and Θ_2 =68.1550.	
4.14	Lower Switches TiMIng Diagram for S5, S6, S7, and S8 at	72
	phase B with mi=0.68 for Θ_1 =8.7740 and Θ_2 =68.1550.	
4.15	Upper Switches Timing Diagram for S1, S2, S3, and S4 at	73
	phase C with mi=0.68 for Θ_1 =8.7740 and Θ_2 =68.1550.	
4.16	Lower Switches Timing Diagram for S5, S6, S7, and S8 at	73
	Phase C with mi=0.68 for Θ_1 =8.7740 and Θ_2 =68.1550.	
4.17	Output Non-Optimization Voltage 5-level inverter mi=0.68	74
4.18	Non-Optimization Harmonic Spectrum for Voltage	75
	Waveform Output of 5-level CHB-MLI with mi=0.68	
4.19	Non-Optimization Harmonic Spectrum for Current	76
	Waveform Output of 5-Level CHB-MLI with mi=0.68	
4.20	Non-Optimization Harmonic Spectrum for Current	76
	Waveform Output of 5-Level CHB-MLI with mi=0.68	
4.21	Upper Switches Timing diagram for S1, S2, S3, and S4 at	77
	phase A with mi=0.58 for Θ_1 =17.9550 Θ_2 =77.9480.	
4.22	Lower Switches Timing Diagram for S5, S6, S7, and S8 at	78
	phase A with mi=0.58 for Θ_1 =17.9550 Θ_2 =77.9480.	
4.23	Upper Switches Timing diagram for S1, S2, S3, and S4 at	78
	phase B with mi=0.58 for Θ_1 =17.9550 Θ_2 =77.9480.	
4.24	Lower Switches Timing Diagram for S5, S6, S7, and S8 at	78
	phase B with mi=0.58 for Θ_1 =17.9550 Θ_2 =77.9480.	
4.25	Upper Switches Timing diagram for S1, S2, S3, and S4 at	79
	phase C with mi=0.58 for Θ_1 =17.9550 Θ_2 =77.9480.	
4.26	Lower Switches Timing Diagram for S5, S6, S7, and S8 at	80
	phase B with mi=0.58 for Θ_1 =17.9550 Θ_2 =77.9480.	
4.27	Output of Non-optimization Voltage 5-level inverter mi=0.58	81
4.28	Non-Optimization Harmonic Spectrum for Voltage	81
	Waveform Output of 5-level CHB-MLI with mi=0.58	

Х

4.29	Non-Optimization Harmonic Spectrum for Current	82
	Waveform Output of 5-level CHB-MLI with mi=0.58.	
4.30	Non-Optimization Harmonic Spectrum for Current	82
	Waveform Output of 5-Level CHB-MLI with mi=0.58.	
4.31	Upper Switches Timing Diagram for S1, S2, S3, and S4 at	83
	phase A with mi=0.48 for Θ_1 =26.6580 and Θ_2 =86.6580.	
4.32	Lower Switches Timing Diagram for S5, S6, S7, and S8 at	84
	phase A with mi=0.48 for Θ_1 =26.6580 and Θ_2 =86.6580.	
4.33	Upper Switches Timing Diagram for S1, S2, S3, and S4 at	84
	phase B with mi=0.48 for Θ_1 =26.6580 and Θ_2 =86.6580.	
4.34	Lower Switches Timing diagram for S5, S6, S7, and S8 at	85
	phase B with mi=0.48 for Θ_1 =26.6580 and Θ_2 =86.6580.	
4.35	Upper Switches Timing Diagram for S1, S2, S3, and S4 at	85
	phase C with mi=0.48 for Θ_1 =26.6580 and Θ_2 =86.6580.	
4.36	Lower Switches Timing Diagram for S5, S6, S7, and S8 at	86
	phase C with mi=0.48 for Θ_1 =26.6580 and Θ_2 =86.6580.	
4.37	Output Non-optimization Voltage 5-level inverter	87
	based on mi=0.48.	
4.38	Non-optimization Harmonic spectrum for voltage	87
	waveform output of 5-level CHB-MLI with mi=0.48	
4.39	Non-optimization harmonic spectrum for current	88
	waveform output of 5-level CHB-MLI with mi=0.48	
4.40	Non-optimization harmonic spectrum for current	88
	waveform output of 5-level CHB-MLI with mi=0.48.	
4.41	Upper Switches Timing diagram for S1, S2, S3, and S4 at	89
	phase A with mi=0.90 for Θ_1 =10 and Θ_2 =35.	
4.42	Lower Switches Timing Diagram for S5, S6, S7, and S8 at	90
	phase A with mi=0.90 for Θ_1 =10 and Θ_2 =35.	
4.43	Output of Non-optimization Voltage 5-level inverter mi=0.90	91
4.44	Non-Optimization Harmonic Spectrum for Voltage	90
	Waveform Output of 5-level CHB-MLI with mi=0.90	

4.45	Non-Optimization Harmonic Spectrum for Current	92
	Waveform Output of 5-level CHB-MLI with mi=0.90	
4.46	Non-Optimization Harmonic Spectrum for Current	92
	Waveform Output of 5-Level CHB-MLI with mi=0.90.	
4.47	Graph of THD Voltage Versus Modulation Index Based	94
	On Simulation Results	
4.48	Graph of THD Voltage Versus Modulation Index Based	94
	On Simulation Results	
4.49	Upper Switches Timing Diagram for S1, S2, S3, and S4	97
	at Phase A	
4.50	Lower Switches Timing Diagram for S5, S6, S7, and S8	97
	at phase A	
4.43	Upper Switches Timing Diagram for S1, S2, S3, and S4	97
	with mi=0.84 for Θ_1 =17.060 and Θ_2 =43.530.	
4.52	Lower Switches Timing Diagram for S5, S6, S7, and S8	98
	for Phase B	
4.53	Upper Switches Timing Diagram for S1, S2, S3, and S4	98
	for Phase C	
4.54	Lower Switches Timing Diagram for S5, S6, S7, and S8	99
	for Phase C	
4.55	Optimization of Voltage Output Waveform	
100		
	of 5-Level CHB-MLI	
4.56	Optimization Harmonic Spectrum of Voltage	101
	Output Waveform	
4.57	Optimization Voltage and Current Output Waveform of 5-Level	102
	CHB-MLI	
4.58	Optimization Harmonic Spectrum of Current Output Waveform	102
4.59	Upper Switches Timing Diagram for S1, S2, S3, and S4 at Phase A	103
4.60	Lower Switches Timing Diagram for S5, S6, S7, and S8 at Phase A	104
4.61	Upper switches Timing Diagram for S1, S2, S3, and S4 at	104

	Phase B with mi=0.68 for Θ_1 =8.7740 and Θ_2 =68.1550.	
4.62	Lower Switches Timing Diagram for S5, S6, S7, and S8 at Phase B	105
4.63	Upper Switches Timing Diagram for S1, S2, S3, and S4 at Phase C	105
4.64	Lower Switches Timing Diagram for S6, S7, and S8 at	106
	Phase C With mi=0.68 for Θ_1 =8.7740 and Θ_2 =68.1550.	
4.65	Non-optimization Voltage Output Waveform of 5-Level	107
4.66	Non-optimization Harmonic Spectrum of Voltage	107
	Output waveform of CHB-MLI with mi=0.68.	
4.67	Non-optimization Voltage and Current Output Waveform of 5-Level	108
4.68	Non-optimization Harmonic Spectrum of Current Output	109
4.69	Upper Switches Timing Diagram for S1, S2, S3, and S4 at Phase A	110
4.70	Lower Switches Timing Diagram for S5, S6, S7, and S8 at	110
	Phase A with mi=0.58 for Θ_1 =17.9550 and Θ_2 =77.9480.	
4.71	Upper Switches Timing Diagram for S1, S2, S3, and S4 at	111
	Phase B with mi=0.58 for Θ_1 =17.9550 and Θ_2 =77.9480.	
4.72	Lower Switches Timing Diagram for S5, S6, S7, and S8 at	111
	Phase B with mi=0.58 for Θ_1 =17.9550 and Θ_2 =77.9480.	
4.73	Upper Switches Timing Diagram for S1, S2, S3, and S4 at	112
	Phase C with mi=0.58 for Θ_1 =17.9550 and Θ_2 =77.9480.	
4.74	Lower Switches Timing Diagram for S5, S6, S7, and S8 at	112
	Phase C with mi=0.58 for Θ_1 =17.9550 and Θ_2 =77.9480.	
4.75	Non-Optimization Voltage Output Waveform of 5-Level CHB-MLI	113
4.76	Non-optimization Harmonic Spectrum of Voltage	114
	Output waveform of CHB-MLI with mi=0.58.	
4.77	Non-Optimization Current Output Waveform of 5-Level	115
	Output waveform of CHB-MLI with mi=0.58.	
4.78	Non-Optimization Harmonic Spectrum of Current	115
	Output waveform of CHB-MLI with mi=0.58.	
4.79	Upper Switches Timing Diagram for S1, S2, S3, and S4 at	116
	Phase A with mi=0.48 for Θ_1 =26.6580 and Θ_2 =86.6580.	
4.80	Lower Switches Timing Diagram for S5, S6, S7, and S8 at	117

xiii

	Phase A with mi=0.48 for Θ_1 =26.6580 and Θ_2 =86.6580.	
4.81	Upper Switches Timing Diagram for S1, S2, S3, and S4 at	117
	Phase B With mi=0.48 for Θ_1 =26.6580 and Θ_2 =86.6580.	
4.82	Lower Switches Timing Diagram for S5, S6, S7, and S8 at	118
	Phase B With mi=0.48 for Θ_1 =26.6580 and Θ_2 =86.6580.	
4.83	Upper Switches Timing Diagram for S1, S2, S3, and S4 at	118
	Phase C With mi=0.48 for Θ_1 =26.6580 and Θ_2 =86.6580	
4.84	Lower Switches Timing Diagram for S5, S6, S7, and S8 at	119
	Phase C With mi=0.48 for Θ_1 =26.6580 and Θ_2 =86.6580.	
4.85	Non-optimization Voltage Output Waveform of 5-Level CHB-MLI	120
4.86	Non-Optimization Harmonic Spectrum of Voltage Output Waveform	120
4.87	Non-optimization Voltage and Current Output	121
	Waveform of 5-Level CHB-MLI with mi=0.48	
4.88	Non-optimization Harmonic Spectrum of Current	122
	Output Waveform of CHB-MLI with mi=0.48	
4.89	Upper Switches Timing Diagram for S1, S2, S3, and S4	123
	with mi=0.90 for Θ_1 =10 and Θ_2 =3	
4.90	Lower Switches Timing Diagram for S5, S6, S7, and S8	123
	with mi=0.90 for Θ_1 =10 and Θ_2 =35	
4.91	Non-optimization Voltage Output Waveform of 5-Level CHB-MLI	124
4.92	Non-optimization Voltage Output Waveform of 5-Level CHB-MLI	124
	with mi=0.90	
4.93	Non-Optimization Harmonic Spectrum of Voltage Output Waveform	125
4.94	Non-optimization Current Output Waveform of 5-Level CHB-MLI	125
	with mi=0.90	
4.95	Non-optimization Harmonic Spectrum of Current Output	126
	Waveform of CHB-MLI with mi=0.90	
4.96	Graph of THD Voltage Versus Modulation Index based	127
	on Experiment Results	
4.97	Graph of THD Current Versus Modulation Index based	127
	on Experiment Results	

xiv

LIST OF ABBREVIATIONS

AC	Alternating Current
DC	Direct Current
CHB-MLI	Cascaded H-bridge Multilevel Inverter
FC	Flying Capacitor
NR	Newton Raphson
DSP	Digital Signal Processors
GUI	Graphic User Interface
IGBT	Insulated Gate Bipolar Transistor
PWM	Pulse Width Modulation
SVPWM	Space Vector Pulse Width Modulation
IEC	International Electric Code
РСВ	Printed Circuit Board

LIST OF SYMBOLS

- f AC power frequency
- f_s Sampling frequency
- f_{sw} Switching frequency
- *I* Current, absolute value
- *V_s* Voltage Source
- *V_{ref}* Voltage Source reference
- Θ Angle
- \sum Summation

xvi

LIST OF PUBLICATION

Journal

- Rosli Omar, Afiqah, Marizan Sulaiman, Krismadinata. "Harmonic Reduction of Cascaded H-bridge Multilevel Inverter Based on Newton-Raphson" International Journal of Applied Engineering ResearchISSN 0973-4562 Volume 10, Number 3 (2015) pp. 6569-6580.
- Mohammed Rasheed, Rosli Omar Afiqah Sabari, Marizan Sulaiman. " Validation of a Three-Phase Cascaded Multilevel Inverter Based on Newton Raphson(N.R) " Indian Journal of Science & Technology ISSN : 0974-5645 (Accepted)

Conference

 Afiqah Sabari, Rosli Omar, Marizan Sulaiman, Mohammed Rasheed, "Optimization and Non-optimization of H-bridge Cascaded Multilevel Inverter" IEEE conference publications, Clean Energy and Technology (CEAT) 2014, 3rd IET International Conference on Date 24-26 Nov. 2014.

xvii

CHAPTER 1

INTRODUCTION

1.1 Background

The multilevel inverter concept has been employed to decrease harmonic distortion (Gobinanth, K., & Mahendran, S., 2013) in the output waveform without decreasing the inverter power output. It has several advantages, such as lower switching frequency and switching losses, lower voltage device evaluation, lower harmonic distortion, high power quality waveform, higher efficiency, reduction of electromagnetic interference (EMI), and interfacing renewable energy sources, such as photovoltaic to the electric power grid (S. Suresh Kota, 2012). Nevertheless, at present, three common topologies of multilevel inverter have been proposed, which are diode-clamped, flying capacitors (FCs), and cascaded H-bridge (CHB) (Akshay K. Rathore, & zjoachim Hotlz, 2010).

Furthermore, the type of multilevel inverter that uses a single DC source rather than multiple sources is the diode-clamped multilevel inverter. Meanwhile, the FC type is designed by a series connection of capacitor-clamped switching cells.

1

Lastly, the CHB type, which can be series or parallel connected, also consists of a series of H-bridge cells to synthesize the required voltage from several separate DC sources, which are recoverable from batteries, fuel cells, renewable energy or ultra-capacitor (Panda, Kaibalya Prasad,

Sahu, Bishnu Prasad, & Samal, 2013). Besides, this CHB topology has the least components for a given number of levels (Colak et al., 2011). Thus, CHB is more advantageous among other multilevel inverter topologies. Moreover, an appropriate switching angle has to be generated by using optimizing techniques to control the switching frequencies of each semiconductor switches connected. Thus, insulator gate bipolar transistor (IGBT) is an example of semiconductor switches that are switched on and off in any ways to keep the percentage of total harmonic distortion (THD) to its minimum value. These switches also have low block voltage and high switching frequency.

1.2 Problem Statement

Multilevel inverters, an approach for harmonic cancellation, have gained worldwide interest. They provide an output with desired waveform that exhibits multiple-steps voltagelevels with minimum distortion. Besides, the modulation control signal is required in a multilevel inverter to generate the synthesized desired output waveform. This is to generate the desired fundamental frequency while minimizing higher-order harmonic content.

In fact, four control methods are commonly used in the multilevel inverters. These methods are traditional PWM control, selective harmonic minimization, space vector