Faculty of Manufacturing Engineering

DEVELOPMENT OF COPPER TO COPPER BONDING OPTIMIZATION ON LOW-K STRUCTURE INTEGRATED CIRCUIT DEVICE

Chan Swee Guan

Master of Manufacturing Engineering (Manufacturing System Engineering)

2016

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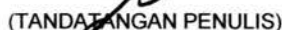

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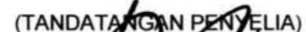

(TANDATANGAN PENYELIA)

Alamat Tetap:
No. A2-3, Block A, 2nd Floor,
Cheng Heights Resort Condominium,
75250 Melaka

Cop Rasmi:
ASSOC. PROF. IR. DR. PUVANASVARAN A/L A. PERUMAL
Faculty Of Manufacturing Engineering
Universiti Teknikal Malaysia Melaka
Hang Tuah Jaya
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DEVELOPMENT ON COPPER TO COPPER BONDING OPTIMIZATION ON LOW-K STRUCTURE INTEGRATED CIRCUIT DEVICE

CHAN SWEE GUAN

A thesis submitted

In fulfilment of the requirements for the degree of Master of Manufacturing Engineering (Manufacturing System Engineering)

Faculty of Manufacturing Engineering

UNIVERSITI TEKNIKAL MALAYSIA MELAKA

2016

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DECLARATION

I declare that this thesis entitled "Development on Copper to Copper Bonding Optimization on Low-k Structure Integrated Circuit Device" is the result of my own research except as cited in the references. The thesis has not been accepted for any degree and is not concurrently submitted in candidature of any other degree.

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APPROVAL

I hereby declare that I have read this dissertation/report and in my opinion this dissertation/report is sufficient in terms of scope and quality as a partial fulfilment of Master of Manufacturing Engineering (Manufacturing System Engineering).

Signature :

Supervisor Name :

ASSOC. PROF. IR. DR. PUVANASVARAN A/L A. PERUMAL
Faculty Of Manufacturing Engineering
Universiti Teknikal Malaysia Melaka
Hang Tuah Jaya
76100 Durian Tunggal, Melaka

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ABSTRACT

Wire bonding technology has been widely used in the semiconductor industry for interconnection between chip and lead frame or substrate. Gold (Au) is the most widely used metal for Integrated Circuit (IC) wire bonding because of its resistance to surface corrosion and high productivity through the Au ball bonding process. However, the upward trend in gold price has prompted the industry interest in gold wire replacement. Copper (Cu) would be one of the best selections as an interconnection material in semiconductor packaging because of its obvious advantages over gold in cost comparison. Cu wire also has lower resistivity where could offer improvement in circuit performance. Despite its material properties advantages, Cu wire bonding technology has still facing many technical challenges due to its characteristic. Copper are very corrosive. Oxidation could easily happen on copper wire and bond pad which cause poor interconnect. In order to solve the bondability issue of Cu wire bonding, the selection of wire capillary and bonding parameters are among key factor must be considered. Design of Experiment (DOE) and evaluations were carried out to have better understanding of this technology. Ball bond diameter, ball height, ball pull and ball shear are among key wire bonding responses been analysed. This development covered the impact analysis of bond pad and circuitry underneath using pad cratering method. Experiment results shown that all bonding responses are meeting targeted results even with additional welded area and cross-section check. One of the key findings was the pre-bonding and initial bonding parameters are crucial for good bondability in Cu-Cu bonding technology. This new understanding becomes a gate opener for further Cu-Cu package development.

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ABSTRAK

Teknology "wire bond" telah digunakan secara meluas dalam industri semikonduktor untuk sambungan antara cip dan rangka utama atau substrat. Emas (Au) adalah antara logam yang paling banyak digunakan dalam proses wire bond. Emas mempuyai kelebihan dalam rintangan hakisan permukaan dan produktiviti yang tinggi. Walau bagaimanapun, arah aliran harga emas telah mendorong industri untuk mencari penggantian wayar emas. Tembaga (Cu) akan menjadi salah satu pilihan yang terbaik dalam industri semikonduktor kerana kelebihannya yang jelas ke atas emas terutamanya pada perbandingan kos. Cu wayar juga mempunyai keringtangan yang lebih rendah di mana ia dapat memberi peningkatan prestasi litar. Walaupun kelebihan sifat-sifat bahannya, teknologi wire bond dengan Cu wayer masih menghadapi pelbagai cabaran teknikal disebabkan oleh ciri-ciri bahannya. Tembaga adalah sangat mengakis. Pengoksidaan mudah berlaku pada dawai tembaga dan bond pad tembaga yang menyebabkan kelemahan dalam interconnect. Untuk menyelesaikan isu bondability ini, pemilihan wayar, kapilari dan parameter wire bond adalah antara faktor penting perlu dipertimbangkan. "Design of Experiment" (DOE) dan eksperimen dijalankan untuk mendapat pemahaman yang lebih baik daripada teknologi ini. Diameter bebola, ketinggian bebola, kekuatan tarikan bebola dan kekuatan ricih bebola adalah antara respons utama yang telah dianalisis. Pembangunan ini juga meliputi analisis terhadap impak pada bond pad dan litaran di bawahnya dimana kaedah Pad Cratering digunakan. Hasil daripada kajian ini menyunjukkan semua respons utama mematuhi objectif yang disediakan. Antara penemuan penting adalah pre-bond and initial bonding adalah parameter yang penting sekali untuk teknologi Cu-Cu bonding. Kefahaman ini penting untuk perkembangan masa hadapan ikatan antara tembaga wayer pada pad tembaga.

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TABLE OF CONTENTS

	PAGE
DECLARATION	
DEDICATION	
ABSTRACT	**i**
ABSTRAK	**ii**
ACKNOWLEDGEMENT	**iii**
TABLE OF CONTENTS	**iv**
LIST OF TABLES	**vi**
LIST OF FIGURES	**viii**
LIST OF APPENDICES	**x**
LIST OF ABBREVIATIONS	**xi**
CHAPTER	
1. INTRODUCTION	**1**
1.1 Semiconductor Manufacturing	1
1.2 Background of the Study	4
1.3 Problem Statement	4
1.4 Objective of the Study	6
1.5 Scope of the Study	6
1.6 Significance of the Study	7
1.7 Report Outline	7
2. LITERATURE REVIEW	**8**
2.1 Wire Bonding	8
2.2 Copper Wire Bonding	9
2.3 Copper Wire Bonding with Coated Copper Wire	11
2.4 Copper Wire Bonding on Aluminium Bond Pad	12
2.5 Copper Wire Bonding on Gold or Nickel-based Bond Pad	14
2.6 Copper Wire Bonding on Copper Bond Pad	15
2.7 Summary	17
3. METHODOLOGY	**18**
3.1 Overview of Research and Experiment	18
3.2 Experiment Setup	19
3.3 Material and Test Vehicle Selection	21
3.4 Performance Measurement	23
3.4.1 Ball Diameter and Ball Height	24
3.4.2 Ball Pull	24
3.4.3 Ball Shear	25
3.4.4 Cratering Test	26
3.4.5 Visual Inspection	27
3.5 Summary	27
4. PRELIMINARY RESULTS AND EXPERIMENT PREPARATIONS	**29**
4.1 Pad Surface Treatment	29
4.2 Satging Evaluation	30
4.3 Bonding Capillary Selection	31
4.4 Free Air Ball Formation Study	32

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4.5 Summary 34
5.0 RESULTS AND DISCUSSIONS **35**
5.1 Feasibility Study Results 35
5.2 Design of Experiment 36
5.3 Key Lever for Cu-Cu Bonding 40
5.4 Validation Runs 43
5.5 Summary 48

6.0 CONCLUSION AND RECOMMENDATIONS **49**

REFERENCES **51**
APPENDICES **57**

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LIST OF TABLES

TABLE	TITLE	PAGE
1.1	Proposal Outline	7
2.1	Comparison of Three Wire Bonding Technologies	8
2.2	Wire Properties comparison between Gold and Copper (1.0mil)	10
2.3	Copper and Gold Wire Bonding Set-up Comparison	11
2.4	Bond Wire Comparison between bare Cu and Pd Coated Cu wire	11
3.1	Package and Material Variations	23
3.2	Targeted criterial for bondability study	28
4.1	Visual Inspection Result after Plasma Process	30
4.2	Visual Inspection Result after Staging on Wire Bonder	30
4.3	Validation result for FAB formation	33
4.4	FAB inspection results	33
5.1	Feasibility matrix for Cu-Cu bonding	36
5.2	Summary Results of DoE (a) Ball Pull (b) Ball Shear	37
5.3	Identified parameters for welded area enhancement	40
5.4	Result of 2-level key lever screening DOE	42
5.5	Ball diameter result after validation run	43
5.6	Ball height result after validation run	44
5.7	Ball pull result after validation run	44
5.8	Ball shear result after validation run	44

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5.9 Calculated welded area and cross-section result after validation run 45

5.10 Pad Cratering result after validation run 46

5.11 Cross-section result on validation run 47

6.1 Conclusion of this study 50

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LIST OF FIGURES

FIGURE	TITLE	PAGE
1.1	Overview of Semiconductor Manufacturing Processes, Front-end and Backend	2
1.2	Back-end Manufacturing Process Flow	3
1.3	Example of Leaded (Left) and Leadless (Right) Packages	3
1.4	Gold price from 2008 to 2013	5
2.1	Example of Aluminium Squeeze out in a Copper Ball Bond	14
3.1	2-level factorial design	19
3.2	Wire Bond DOE process Inputs and Outputs	20
3.3	Overview for Planned Experiment	21
3.4	Outlook of LQFP 176pins 0.5mm pitch	22
3.5	Ball Pull Test	25
3.6	Ball Shear Test	26
3.7	Pad Cratering	26
3.8	Example of Golf Ball and Necking above ball bond	27
4.1	FEA modeling results on CD39 and CD42 (a) Stress on Device (b) Stress on Formed ball	32
4.2	FAB inspection under SEM	33
5.1	DOE matrix with 3 bonding parameters with 2-level factorial	37
5.2	Cross-section from DoE Sample with gap	38
5.3	Welded area inspection after ball shear	38

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5.4	t-test result on bondability DoE	39
5.5	Predicted profiler for bondability DoE	39
5.6	Example of calculated welded area	42
5.7	SEM Inspection after validation runs	43

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LIST OF APPENDICES

APPENDICES	TITLE	PAGE
A	Gantt chart for Master Project 1	57
B	Scope of the study	58
C	Summary of Literature review on Copper Wire bonding	59
D	Flow Chart of Research Proposal Submission	68
E	Flow Chart of Planned Experiment	69

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LIST OF ABBREVIATIONS

PCB	-	Printed Circuit Board
Al	-	Aluminum
Au	-	Gold
Cu	-	Copper
QFP	-	Quad Flat Package
TSOP	-	Thin Small-Outline Package
BGA	-	Ball Grid Array
IC	-	Integrated circuit
DOE	-	Design of Experiment
PCC	-	Palladium Coated Copper
Cu-Cu	-	Copper wire bonding on Cu bond pad
LQFP	-	Low Profile Quad Flat Pack
WB	-	Wire Bond
FAB	-	Free Air Ball
EFO	-	Electronic Flame-Off
Pd	-	Palladium
HAST	-	Highly Accelerated Stress Test
PCT	-	Pressure Cooker Test
Ni	-	Nickel
Low k	-	Low Dielectric-Constant
XoAA	-	Probed and Bonded Over Active Area

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MIL-STD	-	Military Standard
ASTM	-	American Society for Testing and Materials
BoAA	-	Bond over Active Area
PoAA	-	Probe over Active Area
KOH	-	Potassium Hydroxide
NaOH	-	Natrium Hydroxide
DMAIC	-	Define–Measure–Analyse–Improve–Control
RSM	-	Response Surface Methodology
US	-	Ultrasonic Power
DI	-	Distilled
Ag	-	Silver
Pt	-	Platinum
BPO	-	Bond Pad Opening
OSP	-	Organic Surface Protection
SiN	-	Silicon Nitride
SiCN	-	Silicon Carbon Nitride
SiO	-	Silicon Oxide
AlO	-	Aluminum Oxide
Ar	-	Argon
H_2	-	Hydrogen
O_2	-	Oxygen
USG	-	Power
Min	-	Minimum
Max	-	Maximum
Std dev	-	Standard Deviation
HTS	-	High Temperature Storage
uHAST	-	un-bias Temperature Humanity Storage Test
TC	-	Thermal Cycling

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CHAPTER 1

INTRODUCTION

This chapter aims to introduce overview of semiconductor manufacturing processes covering both front-end and back-end production. As the project is focusing on back-end assembly, information on packages is descripted as well. With the brief introduction of semiconductor processes, both background of the study and problem statement are discussed. Objective, scope under study and significant of the study is covered under this chapter as well.

1.1 Semiconductor Manufacturing

The semiconductor production process can be divided into two progressive sub-processes commonly referred to front-end and back-end manufacturing which both contain many process steps. The entire process, both front-end and back-end production, is complex and requires sophisticated engineering and manufacturing expertise.

As shown in Figure 1.1, front-end production refers primarily to wafer fabrication, whereas back-end production refers to the assembly and test of individual semiconductors. Thus, in semiconductor manufacturing, integrated circuit (IC) packaging is the final stage of semiconductor device fabrication, in which the tiny block of semiconducting material is encased in a supporting case that prevents physical damage and corrosion. It is also known as a "package", supports the electrical contacts which connect the device to a circuit board.

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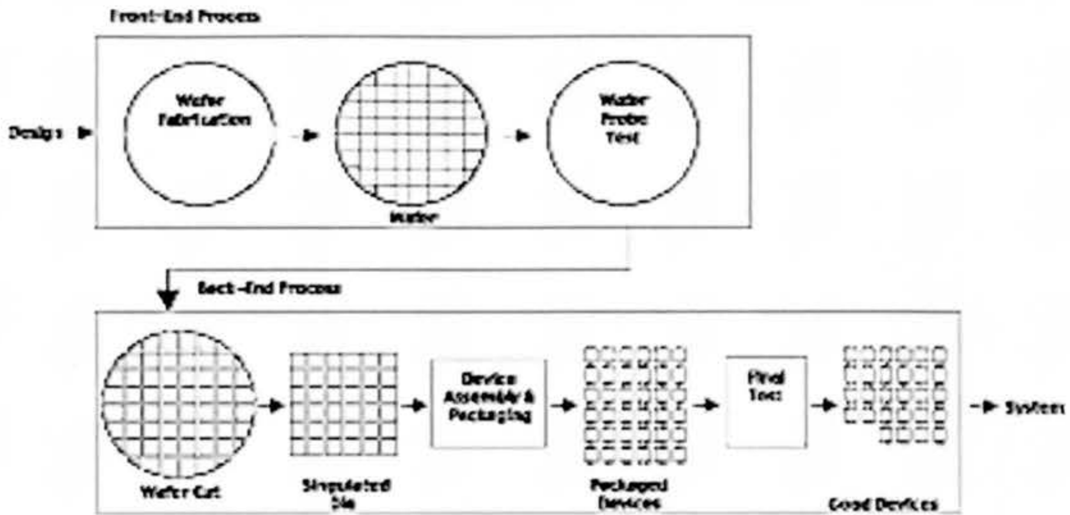

Figure 1.1: Overview of Semiconductor Manufacturing Processes, Front-end and Backend (Anonymous, Accessed on 14 December 2015)

The system under study is semiconductor integrated circuit in back-end assembly process technology. Back-end production refers to the assembly and test of individual semiconductors which the process flow are sketched in Figure 1.2. The assembly process is necessary to protect the chip, facilitate its integration into electronic systems, limiting electrical interference and enabling the heat dissipation from the device. Once the front-end production process is complete, the wafer is transferred to an assembly facility, where it is sawed into individual chips. These semiconductor chips are then individually attached by means of an alloy or an adhesive to a lead frame, a metallic device used to connect the semiconductor to a printed circuit board (PCB). Leads on the lead frame are then connected by aluminium (Al), gold (Au) or copper (Cu) wires to the input/output terminals on the semiconductor chip through the use of automated machines known as wire bonders. Each semiconductor device is then encapsulated in a plastic mold compound or ceramic case, forming the package. After assembly, semiconductors package are tested for different operating specifications, including functionality, voltage, current and timing.

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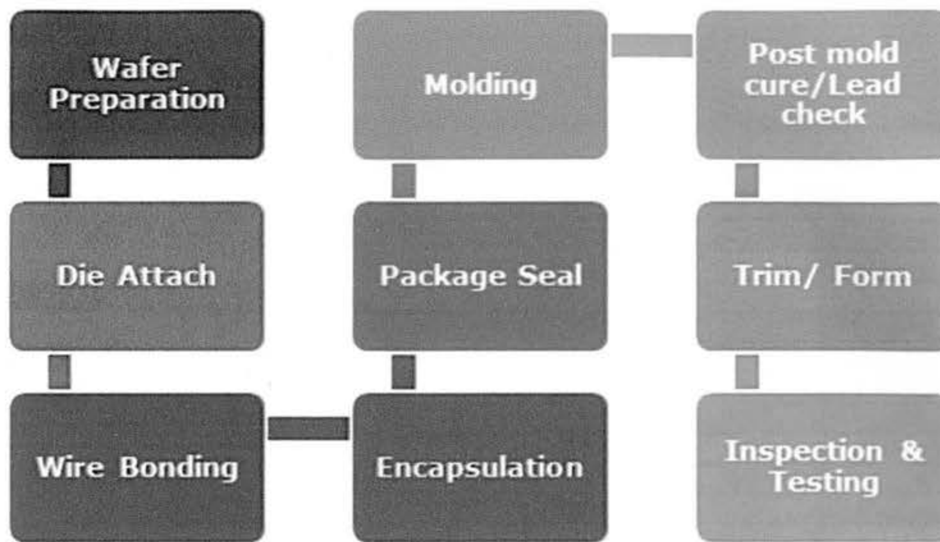

Figure 1.2: Back-end Manufacturing Process Flow

Generally, packaging could be divided into 2 main categories, leaded and leadless. Packaging with lead protruded from package called leaded package. Interconnect to circuit board are mainly done with surface mount technology. Examples of leaded packaging are Quad Flat Package (QFP) and Thin Small-Outline Package (TSOP) in Figure 1.3. Whereas, packaging without lead are commonly connected to circuit board with solder balls. Ball Grid Array (BGA) is the best example of leadless packages.

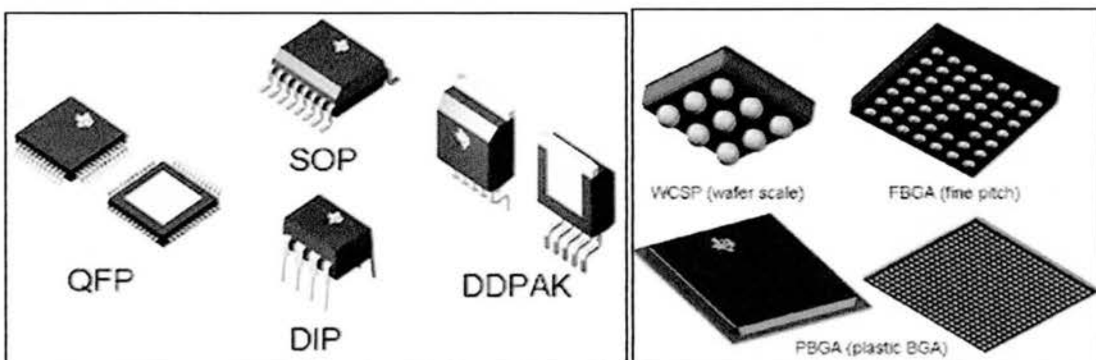

Figure 1.3: Example of Leaded (Left) and Leadless (Right) Packages

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1.2 Background of the Study

In the semiconductor and overall electronics industry, the move toward further miniaturizing of packages, components and modules while also increases their functionality. This trend challenges the back-end assembly process forwarding in high density packages and pushing the limits of equipment and process in terms of accuracy and speed, especially for the wire bond process.

Wire bonding is the method used to attach very fine wire from one connection pad to another, completing the electrical connection in an semiconductor or electronic device. Wire bonding is generally considered the most cost effective and flexible interconnect technology and is used to assemble the vast majority of semiconductor packages.

Different types of wires are used for the wire bond process: gold (Au), Aluminium (Al) and copper (Cu). Each material has its advantages and disadvantages and is bonded by a different method. As majority of integrated circuit (IC) are assembled with wire bonding process, it is crucial to understand this technology. This study is focusing on Cu wire bonding particularly on 40 nanometre node wafer technology with low-k material.

1.3 Problem Statement

Gold (Au) wire is the most widely used for IC wire bonding because of its resistance to surface corrosion and high productivity via the gold ball bonding process. However, the upward trend in gold price has urged the industry interest in gold wire replacement. According to Chauhan et al. (2014), gold price rose to double the price in year 2013 compared to year 2008. Figure 1.4 below shows the gold price from year 2008 to 2013.

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Figure 1.4: Gold price from 2008 to 2013 (Chauhan et al., 2014)

Copper would be one of the best selections as an interconnection material in semiconductor packaging because of its obvious advantages over gold. Copper wire offers significant cost advantage over gold wire. It is also an excellent replacement for gold wire due to its similar electrical properties. Copper wire has lower resistivity where could offer improvement in circuit performance as well. Similarly goes to copper bond pad compared to gold plated bond pad.

Despite material properties advantages, copper wire bonding technology has still facing many technical challenges due to its characteristic. Copper are very corrosive. Oxidation could easily happen on copper wire and bond pad which form copper oxide that act as barrier to interconnect (Descartin et al., 2013). Copper wire is relatively harder and brittle compared to gold wire which has high risk of damaging bond pads and circuitry underneath bond pad. Robust pad stack design needs to be developed to resolve this issue as well to prevent damage to circuitry underlying bond pad.

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In order to solve the bondability issue of cu wire bonding, the selection of wire types, wire capillary, bonding parameters are among key factor to be considered (Premkumar et al., 2008). Various options of protective layer on bare copper bond pad are planned to be evaluated as well. Design of Experiment (DOE) and experiment need to be carry out to have better understanding of this technology. This development shall cover the impact analysis of bond pad and circuitry underneath, especially fragile low-k material.

1.4 Objective of the Study

The main objectives of the study are the following:

1. To study on copper wire bonding in market and development of Copper Wire Bonding.
2. To explore the bondability between palladium coated copper (PCC) wire and copper bond pad coated with oxidation protective layer.
3. To evaluate and measure the performance output of Cu-Cu and impact of wire bonding process toward low-k material structure.

These activities are expected to be completed within 5 months. The detail Gantt Chart Planning is sketched and attached in Appendixes A.

1.5 Scope of the Study

This study is focusing on Copper wire bonding on Cu bond pad (Cu-Cu) bonding characterization, optimization and to understand the impact of bond structure underneath bond pad due to bonding process. Targeted test vehicle used will be latest 40nm node wafer technology in Low Profile Quad Flat Pack (LQFP), lead frame package platform. Reliability assessment is not planned in this study. Details scope of the study is outlined in K-chart format shown in and attached in Appendixes B.

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