Faculty of Electrical Engineering

MULTILEVEL THREE PHASE VOLTAGE SOURCE INVERTER WITH SIMPLE SPACE VECTOR PULSE WIDTH MODULATION

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DECLARATION

I declared that this thesis entitle "Three phase multilevel voltage source inverter" is the result of my own research except as cited in the references. The thesis has not been accepted for any degree and is not concurrently submitted in candidature of any other degree.

Signature :

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Date :

APPROVAL

I hereby declare that I have read this thesis and in my opinion this thesis is sufficient in terms of scope and quality for the award of Master of Science in Electrical Engineering.

Signature :

Name : PM Dr. Zulkifilie bin Ibrahim

Date :

DEDICATION

To my beloved elder sister

ABSTRACT

Multilevel inverter has brought a great revolution in many industrial applications. The performances of multilevel inverter depend on the suitable modulation technique and topology. There a number of modulation techniques and topologies are already developed during last three decades. The most popular multilevel inverter topology is cascaded h-bridge inverter due to not having any clamping diode or capacitor and better performances. But it requires several number of separated DC sources that increase complexity as well as system cost. Three phase cascaded multilevel inverters with reduced number of DC voltage sources are proposed in this research that requires only 2, 3, 4, 5 and 6 separated DC sources for three phase 3, 4, 5, 6 and 7-level. Three phase cascaded multilevel inverters with single DC voltage source are also proposed in this research. On the other hand, the most popular modulation technique is space vector pulse width modulation (SVPWM) because of their easier digital realization, over modulation, high switching frequency, better DC bus utilization and lower THD. The complexity of switching control algorithms for multilevel inverter is increasing with the number of level due to increasing the number of switching states in space vector diagram. This research simplifies the space vector diagram that reduces the switching states to 26 from 27, 56 from 64, 98 from 125, 152 from 216 and 218 from 343 for 3, 4, 5, 6 and 7-level SVPWM respectively. The simplified strategy used in the research, the lower weighted digit values of switching states are omitted because performance of the multilevel inverter depends on the more weighted digit value of switching states. However it still has a constraint of having different number of switching states for different sub switching triangle of each sector. Therefore, the best four different active switching states will be selected for each switching triangle that makes the overall PWM algorithm simpler. The proposed three phase cascaded multilevel inverters (CMLI) based on simple space vector pulse width modulation have been modeled, simulated and evaluated using MATLAB/SIMULINK. Simulation results based on the proposed technique demonstrated the significant improvement in terms of output voltage and THD. The inverters of each level have been implemented using a single eZdsp control board embedded with TMS320F2812 processor. The results obtained from the experimental investigation for 3, 4, 5, 6 and 7 level inverter are consistent with the results obtained from the simulation. The three phase 7-level CMLI demonstrated 10.69% THD that is closest the IEE519 standard of 10% THD.

ABSTRAK

Penyongsang pelbagai aras telah memberi revolusi yang besar didalam banyak aplikasi indsutri. Prestasi bagi penyongsang pelbagai aras bergantung kepada kesesuaian teknik modulasi dan topologi. Terdapat beberapa teknik modulasi dan topologi yang telah dibangunkan dalam tiga dekat yang lalu. Topologi penyongsang pelbagai aras yang paling popular adalah penyongsang h-jambatan lata kerana tidak memiliki diod pengapit atau kapasitor dan menghasilkan prestasi lebih baik. Tetapi ia memerlukan beberapa bilangan sumber DC voltan yang berasingan yang akan meningkatkan kerumitan dan juga kos sistem. Penyongsang pelbagai aras lata dengan penggurangan bilangan sumber DC telah dicadangkan dalam penyelidikan ini yang memerlukan hanya 2, 3, 4, 5 dan 6 sumber DC yang berasingan untuk tiga fasa 3, 4, 5, 6 dan 7 aras. Penyongsang pelbagai aras lata tiga fasa dengan sumber DC tunggal dicadangkan dalam penyelidikan ini. Selain itu, teknik modulasi yang paling popular adalah modulasi lebar denyut jenis vektor ruang (SVPWM) kerana ianya mudah direlisasikan secara digital, modulasi lebih had, frekuensi pensuisan yang tinggi, lebih baik penggunaan bas DC dan THD yang rendah. Kerumitan bagi algoritma kawalan pensuisan untuk penyongsang pelbagai aras adalah meningkat bersama dengan bilangan aras disebabkan oleh peningkatan bilangan keadaan pensuisan di dalam rajah vektor ruang. Penyelidikan ini memudahkan rajah vektor ruang yang mengurangkan keadaan pensuisan kepada 26 daripada 27, 56 daripada 64, 98 daripada 125, 152 daripada 216 dan 218 daripada 343 untuk 3, 4, 5, 6 dan 7 aras SVPWM. Strategi termudah yang digunakan dalam penyelidikan, nilai pemberat digit yang terendah akan dikeluarkan kerana prestasi pelbagai aras penyongsang bergantung keatas nilai digit pemberat bagi keadaan pensuisan. Walaubagaimanapun ia masih menghadapi kekangan yang mempunyai keadaan pensuisan yang berbeza untuk sub pensuisan segitiga bagi setiap sektor yang berbeza. Oleh sebab itu, empat keadaan pensuisan aktif terbaik akan dipilih bagi setiap sektor segitiga pensuisan yang menjadikan algoritma keseluruhan PWM menjadi lebih mudah. Penyongsang pelbagai aras lata (CMLI) tiga fasa yang dicadangkan adalah berdasarkan modulasi lebar denyut jenis vektor ruang mudah yang telah dimodel, disimulasi dan dinilai menggunakan MATLAB/SIMULINK. Keputusan simulasi berdasarkan kepada teknik yang dicadangkan telah menunjukkan penambahbaikan yang ketara dari segi voltan keluaran dan THD. Penyongsang bagi setiap aras telah pun dilaksanakan menggunakan satu papan eZdsp yang mempunyai pemproses TMS320F2812. Keputusan yang diperolehi dari kajian ujikaji untuk 3, 4, 5, 6 dan 7-aras penyongsang adalah sejajar dengan keputusan yang diperolehi dari simulasi. CMLI 7-aras tiga fasa menunujukkan 10.69% THD yang terdekat dengan piawaian IEE519 yang mempunyai 10% THD.

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Symbol		Description
m	-	number of level
V_a, V_b, V_c	-	three phase reference signals
V_{ab},V_{bc},V_{ca}	-	Three phase line to line voltages
V_α, V_β	-	α and β-axis voltages of Clark transformation
V_d, V_q	-	d and q-axis voltages of park transformation
S	-	Number of sector
V_{dc}	-	DC supply voltage
θ	-	Angle of each sector
γ	-	Angle between x-axis and rotating reference vector
V*	-	Rotating reference vector
∇	-	Number of triangle

LIST OF ABBREVIATIONS

Name		Description
DC	-	Direct Current
PWM	-	Pulse width modulation
SPWM	-	Sine pulse width modulation
THIPWM	-	Third harmonic injection pulse width modulation
SVPWM	-	Space vector pulse width modulation
2LSVPWM	-	2-level space vector pulse width modulation
2LSPWM	-	2-level sine pulse width modulation
3LSVPWM	-	3-level space vector pulse width modulation
3LSPWM	-	3-level sine pulse width modulation
4LSVPWM	-	4-level space vector pulse width modulation
5LSVPWM	-	5-level space vector pulse width modulation
6LSVPWM	-	6-level space vector pulse width modulation
7LSVPWM	-	7-level space vector pulse width modulation
CMLI	-	Cascaded multilevel inverter
CMLIs	-	Cascaded multilevel inverters
TPCMLI	-	Three phase cascaded multilevel inverter
TPCMLIs	-	Three phase cascaded multilevel inverters
DCLI	-	Diode clamped inverter
CCLI	-	Capacitor clamped inverter
CHBI	-	Cascaded h-bridge inverter
5LDCLI	-	5-level diode clamped inverter

3LCCLI	-	3-level capacitor clamped inverter
3LCMLI	-	3-level cascaded multilevel inverters
4LCMLI	-	4-level cascaded multilevel inverters
5LCMLI	-	5-level cascaded multilevel inverters
6LCMLI	-	6-level cascaded multilevel inverters
7LCMLI	-	7-level cascaded multilevel inverters
THD	-	Total harmonic distortion
MPWM	-	Modified Pulse Width Modulation
RPWM	-	Random Pulse Width Modulation
SHEPWM	-	Selective Harmonic Elimination Pulse Width Modulation
IGBT	-	insulated gate bipolar transistor
MI	-	Modulation index

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