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# Implementation of Carrier-Based Simple Boost Pulse Width Modulation (PWM) for Z-Source Inverter (ZSI) using Field Programming Gate Array (FPGA)

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**ABSTRACT:** In recent years, the research on the Z-source inverter (ZSI) has received a wide acceptance due to its attractive solution for example in the renewable energy interface that requires voltage boost capability. The conventional inverter circuit based on the SPWM technique for example does not able to fully utilize its DC input voltage to produce a greater output voltage. The ZSI shoot-through implementation in high switching frequency requires a processor with fast sampling and high precision. In simulation, this can be easily carried out with the available advanced engineering software. In the hardware implementation however, the processor used is not only handle the switching, but also needs to read the data obtained by the sensor, voltage and current control, information display etc. This limits the capacity that can be used to implement the switching fast sampling with high precision. The aims of this work are to implement high precision of carrier-based simple boost PWM for ZSI using FPGA and to verify its real time hardware implementation. The high precision of PWM control algorithm based on the FPGA platform is verified by comparing the simulation results with the experimental results for different modulation index and boost factor, and a good agreement is concluded. It is observed that the application of FPGA reduces complexity, increases speed and the design of the switching technique can be altered without having to modify the hardware implementation.

## 1. INTRODUCTION

Inverter has been widely accepted in the application where conversion from DC to AC is necessary. Either in a single phase or three phase, its application ranges from a low to high power application in various fields, e.g. renewable energy conversion, power supply and consumer electrical and electronics applications.

The conventional voltage source inverter (VSI) topology with a DC link voltage across the inverter is widely used but inability to produce an output voltage beyond its input becomes its main drawback. With the DC-DC boost converter in between the input source and the inverter, the voltage across the inverter can be easily be easily increased, but this has several drawbacks, for instance, the limitation in the gain of voltage boost before the inverter, additional components and complexity in control which contributes to losses and distortion [1-3].

As a solution to the above problems, the Z-source inverter (ZSI) [4-6] topology was first introduced, with a view of serving as a buck boost inverter in a single stage conversion. It offers a



higher voltage boost gain and eliminates overlapping problem between the inverter switches and a distortion in the inverter output current due to the introduction of the dead time [7-8].

In the aspect of hardware implementation, the ZSI [9] requires a high rate and speed processor to perform an accurate switching modulation. However, digital implementation such as digital signal processing (DSP) are expensive and contribute to a higher system complexity. Other option such as the use of analogue IC's or circuit which has a good linearity, but the analog circuit tend to introduce a noise problem which causes error and degrades modulation performance. This work proposes on the use of FPGA controller as a digital implementation to realize the switching control for the ZSI. The implementation of the shoot-through operation introduced during the zero states of the switching cycle requires a fast sampling and high precision and the FPGA is very much suitable for this purpose. In the next session, the basic introduction to ZSI is presented as well as a detail derivation of important equations governing the ZSI implementation. In section 3, the FPGA implementation is detailed and verification results through both simulation and experimental hardware is presented in section 4. The work is concluded in section 5. [10-14]

## 2. Z-SOURCE INVERTER (ZSI)

The Z-source inverter (ZSI) is an alternative topology based on the drawbacks identified in the existing traditional inverter. The traditional inverter topology can be classified into two categories; the voltage source inverter (VSI) and the current source inverter (CSI). Due to complexity, losses problem and higher cost, the CSI is less implemented compared to the VSI. In the application of DC to AC conversion however, the VSI has a drawbacks as follow; [5-6]

1. The obtainable output voltage range is limited by the input voltage and the effort to further vary the produced output e.g. adding the DC to DC converter, will require an added complexity and cost in the circuitries.
2. Vulnerability to the short circuit problem (shoot through) among the semiconductor devices used in the inversion circuitries caused by the switching overlapping or EMI noise interference.

Figure 1 shows the topology of Z-Source Inverter (ZSI). The main characteristic of the topology is the existence of impedance network formed by the inductors and capacitors between the source of input and the inverter stage. The existence of this impedance network will allow for a situation which is not allowed in the traditional VSI or CSI; the shoot-through or short-circuiting of the main switching circuit at the inverter stage. By intentionally creating the shoot-through situation, the ZSI inverter able to boost the input voltage to produce an output voltage that cannot be achieved by the traditional converter.[2-4]

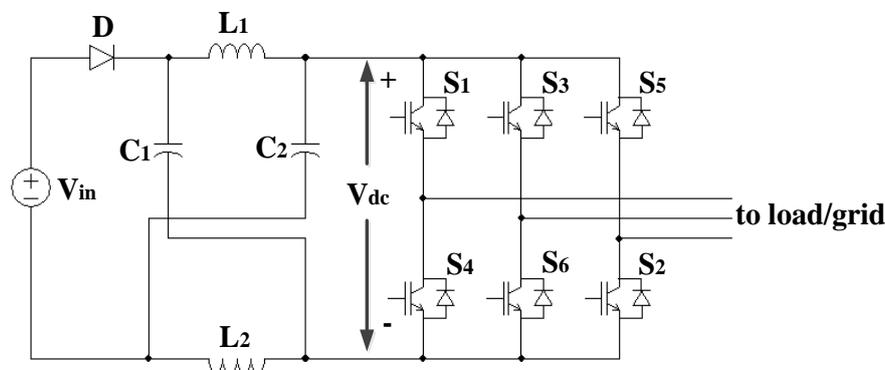


Figure 1 : Topology of Z-source inverter

### 2.1 Operating principle

The ZSI as shown in Figure 1 has two operating modes, namely the non-shoot-through (non-ST) mode and the shoot-through (ST) mode. The non-ST mode is similar to the conventional three phase inverter operation, when a non-zero voltage exists across the inverter legs. The ST mode is introduced during the zero state when all the three upper/lower switches are in OFF or ON condition with the voltage across the legs is zero. The current flow through at least one of the legs and with the addition of the inductor-capacitor (LC) network, the average voltage across the inverter legs is boosted. The boosted voltage level depends on the shoot-through time over one switching period. [2-3]

### 2.2 Circuit analysis Equivalent circuit

Figure 2 shows the equivalent circuit of the ZSI during both the non-ST and ST states. During the ST state in Figure 2 (a), the load terminal is shorted across any phase leg of the switching device, the sum of capacitor voltage  $V_{C1} + V_{C2}$  is higher than  $V_{DC}$ , causing the diode to be reverse-biased and the inductors are charged by the capacitors. As a result, equations (1.1) to (1.3) are obtained.

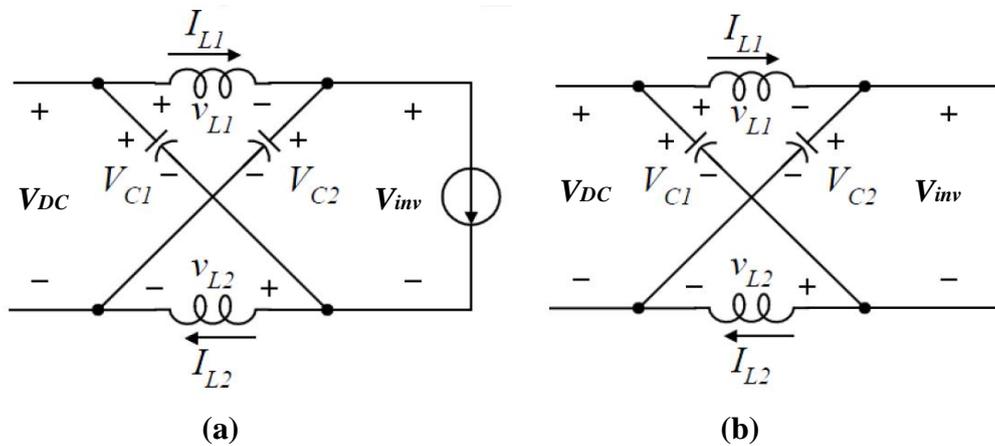


Figure 2: Equivalent circuit of ZSI during (a) shoot-through state and (b) non-shoot-through state

$$v_{in} = 2v_C \quad (1.1)$$

$$v_{L-sh} = v_L = v_C \quad (1.2)$$

$$V_{inv} = 0 \quad (1.3)$$

$V_{in}$  is the input voltage at the source,  $V_C$  is the voltage across both capacitors,  $V_{L-sh}$  is the inductor voltage during shoot-through and  $V_{inv}$  is the voltage across the inverter legs. The non-ST state is triggered when the input diode is turned on, the power source input (either current source or voltage source) and the inductors release energy to the load directly charging the capacitor. As a result, the dc-link voltage  $V_{inv}$  is boosted across the inverter. The following equations (1.4) to (1.6) are obtained during this operation with  $V_{L-nsh}$  is the inductor voltage during non-shoot-through.

$$v_{L-nsh} = v_L = V_{DC} - v_C \quad (1.4)$$

$$v_{inv} = v_C - v_L = 2v_C - v_{in} \quad (1.5)$$

$$v_{in} = V_{DC} \quad (1.6)$$

Defining  $T$  as a period of one switching cycle, in steady state circuit the average voltage,  $v_L T$  across the inductor over one switching period should be zero, and the relationship between ST and non-ST can be expressed as follows.

$$v_L T = v_{L-nsh} T_{nsh} + v_{L-sh} T_{sh} = 0 \quad (1.7)$$

$$v_{L-nsh} = v_L = V_{DC} - v_C \quad (1.8)$$

$$v_L T = (V_{DC} - v_C) T_{nsh} + v_{L-sh} T_{sh} = 0 \quad (1.9)$$

$$\frac{v_C}{V_{DC}} = \frac{T_{nsh}}{T_{nsh} - T_{sh}} \quad (1.10)$$

The peak DC-link voltage across the inverter can be written as below. Express the ideation in term of  $V_{DC}$

$$v_{inv} = 2v_C - v_{in} = \frac{2v_C - V_{DC}}{V_{DC}} (V_{DC}) = \left( 2 \frac{T_{nsh}}{T_{nsh} - T_{sh}} - 1 \right) (V_{DC}) = g V_{DC} \quad (1.11)$$

where  $g$  is the boost factor,

$$g = \frac{T_s}{T_{nsh} - T_{sh}} = \frac{1}{1 - 2 \frac{T_{sh}}{T_s}} = \frac{1}{1 - 2\delta} \geq 1 \quad (1.12)$$

and  $\delta$  is the shoot-through duty ratio over one switching cycle. The value of boosting factor is always more than unity and it produces a higher output voltage due to the shoot through states introduced within the switching states.

In the inverter circuit based on pulse width modulation (PWM) technique, the modulation index equation,  $M$  can be defined as

$$M = \frac{V_{ref}}{V_{TRI}} \quad (1.13)$$

where  $V_{ref}$  is the amplitude of sinusoidal control signal and  $V_{TRI}$  is the amplitude of the high frequency triangular signal. For the linear modulation  $M \leq 1.0$ , the fundamental output voltage at each phase  $V_{Xn,1}$  can be defined as in (1.14), where  $V_d$  is the voltage across the inverter input. As for the ZSI,  $V_d$  equals to  $V_{inv}$ , and combined with (1.11), the fundamental output voltage at the phase is defined as in (1.15).

$$v_{Xn,1} = M \frac{V_d}{2} \quad (1.14)$$

$$v_{Xn,1} = Mg \frac{V_{DC}}{2} \quad (1.15)$$

Figure 3 (a) shows the waveform of SPWM implementation for the conventional inverter and (b) shows how the shoot-through is implemented in the ZSI. In Figure 3,  $s_{x1}$  and  $s_{x2}$  represents the switching signal at the inverter phase. The inverter circuit is made up of three-phases with each containing two IGBTs. At each instant during one switching cycle, there are six combinations of switching which are  $(s_{c1}, s_{b2}, s_{a1})$ ,  $(s_{b2}, s_{a1}, s_{c2})$ ,  $(s_{a1}, s_{b1}, s_{c2})$ ,  $(s_{c2}, s_{b2}, s_{a2})$ ,  $(s_{b1}, s_{a2}, s_{c1})$ , and

( $s_{a2}, s_{c1}, s_{b2}$ ) and each of the switch conducts at 60 degree in sequence to produce the output phase sequence.

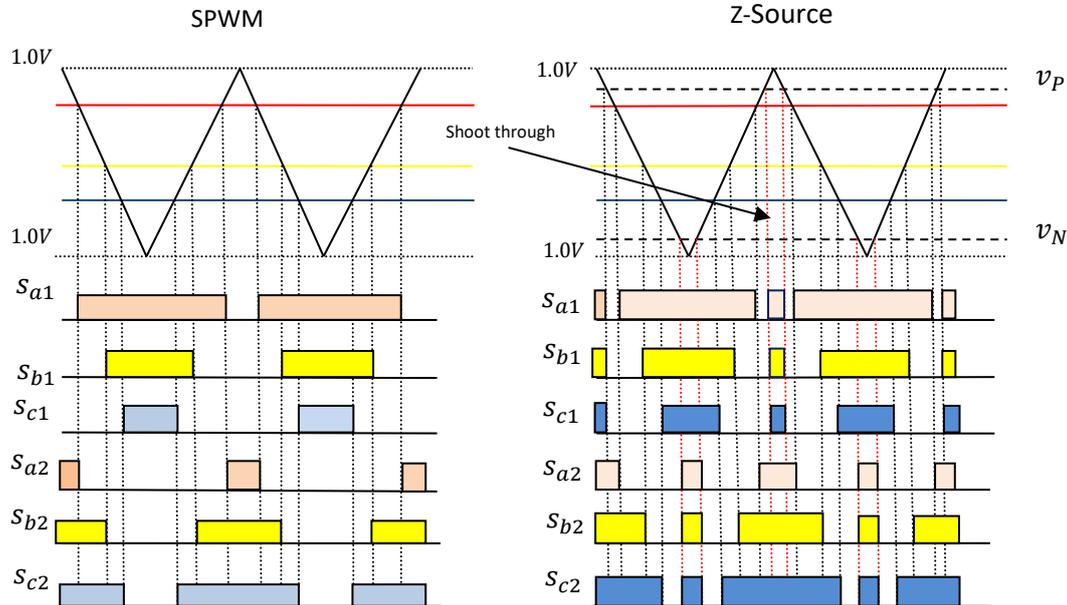


Figure 3 : Implementation of SPWM in (a) conventional inverter and (b) ZSI with shoot-through

As for the ZSI, shoot-through is carried out whenever all the upper/lower switches are in ON or OFF condition (zero states), forcing the complementary switches at each leg to ON. The time length of the shoot-through is limited by the preset  $v_P$  and  $v_N$  values.

### 3. Implementation with FPGA

Figure 4 shows the block diagram of an implementation flow of using the FPGA to realize the ZSI operation. In this experiment, FPGA board is used to generate the switching signal at higher rate of computation with high-linearity. Firstly, the ZSI model is simulated and the PWM control algorithm is performed using the MATLAB/Simulink at 1 MHz high sampling frequency. The PWM data is stored in the Matlab workspaces by connecting the switching signal of the control circuit to a workspace block in MATLAB/Simulink.

In the next step, the data from the simulation is executed by FPGA using the look-up table approach and carried out in the control switching coding performed by the FPGA. The size of the data store in lookup table is determined by the precision (number of bits) of the inputs. In this way, the total number of data stored is defined by one cycle time divided by sample time ( $T_s$ ). An important aspect at the time of the implementation of an algorithm in a FPGA, to match the sample time desired equal to the clock in FPGA, the sample time ( $T_s$ ) divided by maximum FPGA clock.

The Quartus II software is used to synthesize the VHSIC hardware description language (VHDL) code, to configure the data structure, compiling the coding of the Verilog code and load it onto the FPGA via USB blaster cable. [11-13] In the conventional inverter, the most common technique to prevent the shoot-through fault is by adding a delay or hold-off time between the ON switching of the high-side or lower side switch. This blanking time is required for conventional to prevent the short circuit. For ZSI however, the blanking time is unnecessary since the IGBT allows both upper and lower switches to turn ON simultaneously. The FPGA platform used is the Altera DE0 Cyclone IV board with clock speed of 50 MHz, as well as 8-Mbyte single Data Rate Synchronous Dynamic RAM memory chip that supports 16 bits data bus. [12-14]

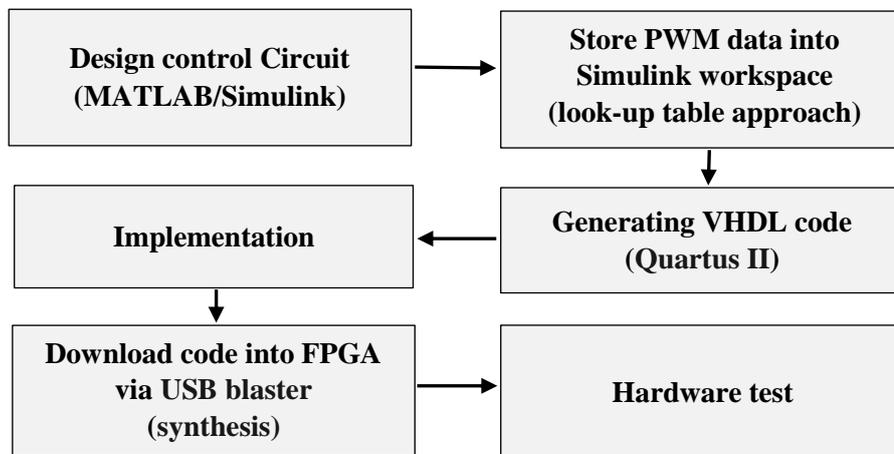


Figure 4: Block diagram of the implementation flow

#### 4. Results and discussion

In the verification stage, simulation is firstly carried out and the switching data is then used for the experimental work. The experimental work is carried out to demonstrate that the results from the FPGA based implementation of carrier-based simple boost PWM for the ZSI satisfactorily match the simulation results. Simulation of the Z-source inverter is carried out with the Matlab Simulink software and the parameters used are as in Table I.

Table I : Parameters used for Z-source inverter simulation

Parameter	Value
Input voltage	20 V
Switching frequency	5 kHz
Fundermntal frequency	50Hz (0.02s)
Maximum FPGA frequency	50MHz (20ns)
Sample time	1us
Load	10 k $\Omega$
Number of data stored in workspace	20000
Clock FPGA ratio	50:50

As a comparison, the operability of the Z-source inverter under different modulation index  $M$  and boost factor  $g$  is verified. Figure 5 and 6 shows precision results obtained from both simulation and experimental work at  $M = 0.9$  and  $0.6$ . The harmonics analysis of the output voltage is presented as well. It can be seen that the fundamental output voltage of the ZSI for both results shows a good agreement with each other. The results prove that the output voltage will increases with modulation index,  $M$ . Besides that, it also proves that, FPGA can produce precise output switching with small sample time up to 20ns within high speed.

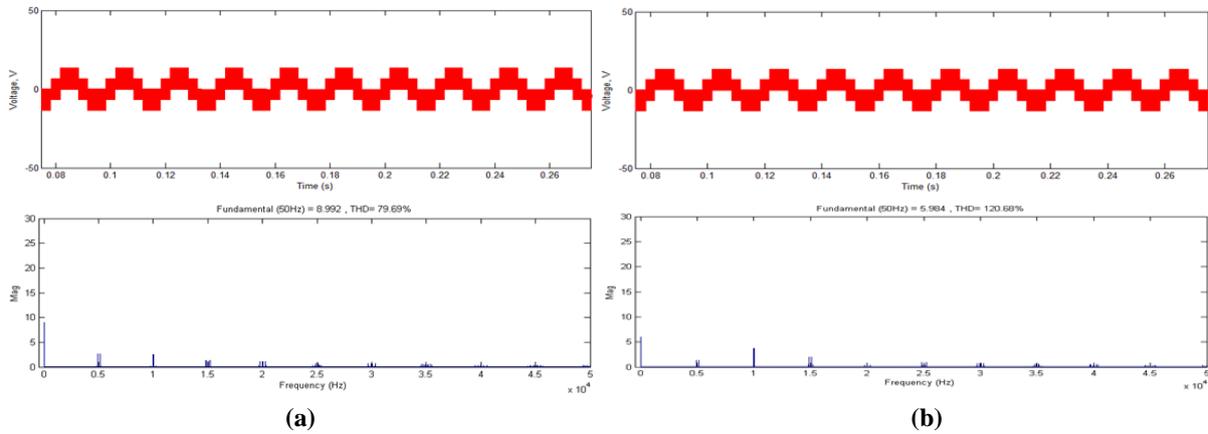


Figure 5: Simulation results of Z-source inverter of phase output voltage at (a)  $M = 0.9$  and (b)  $M = 0.6$

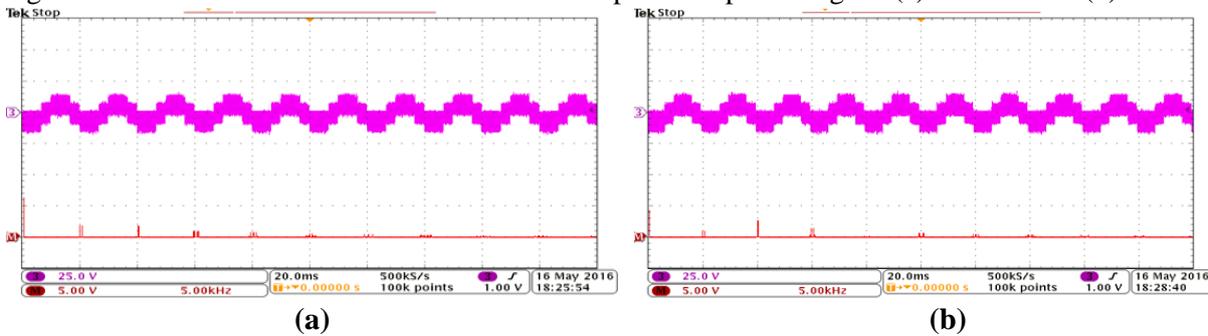


Figure 6: Experimental results of Z-source inverter for phase output voltage at (a)  $M = 0.9$  and (b)  $M = 0.6$

Figure 7 and 8 shows the the Z-source inverter operability under different boost factor; at  $g = 3.33$  and  $1.11$  under same modulation index  $M = 0.6$ . At  $g = 3.33$ , the fundamental peak phase output voltage is approximately 19 V for both simulation and experiment. While at  $g = 1.1$ , again both simulation and experient results a good agreement of approximately 6.5 V. Based on the results presented, it is shown that the FPGA based implementation of the ZSI satisfactorily agrees with the simulation carried out with the Matlab Simulink software.

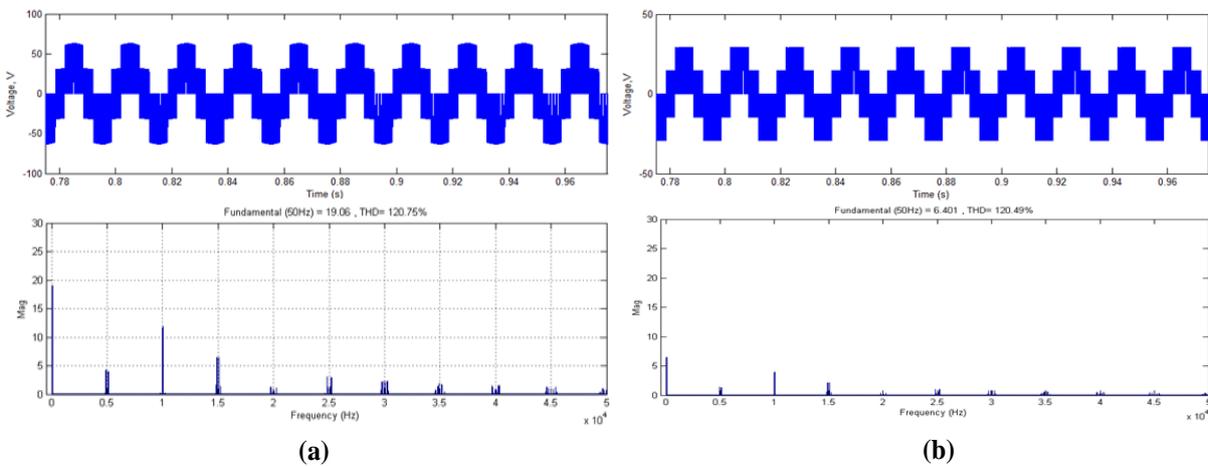


Figure 7 : Simulation results of Z-source inverter of phase output voltage at (a)  $g = 3.33$  and (b)  $g = 1.11$  with same  $M = 0.6$

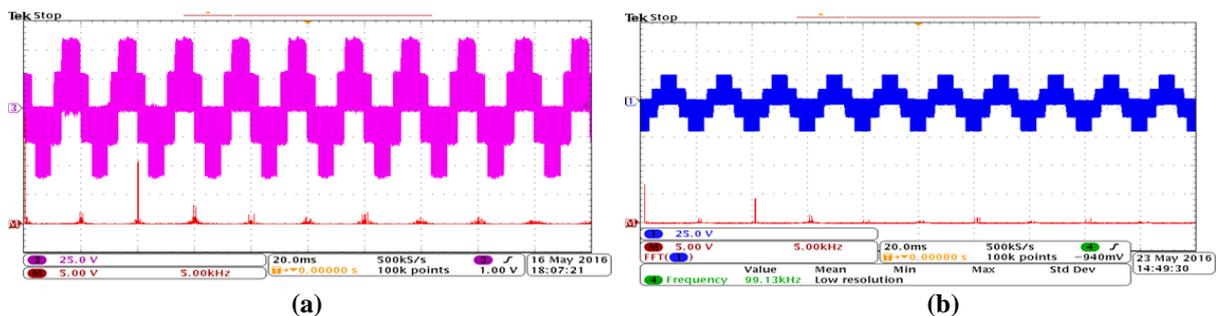


Figure 8 : Simulation results of Z-source inverter of phase output voltage at (a)  $g = 3.33$  and (b)  $g = 1.11$  with same  $M = 0.6$

## 5. Conclusion

This paper proposes on the use of FPGA to implement a carrier-based simple boost PWM for the Z-Source inverter. By using the FPGA, a fast sampling and with high precision switching can be realized, and results obtained from the simulation can be verified accordingly. Simulation of the ZSI is carried out at different modulation index and boost factor, and the results from the experimental works demonstrate a good agreement with the simulation results. It is observed that the application of FPGA reduces complexity, increases speed and the design of the switching technique can be altered without having to modify the hardware implementation.

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