Faculty of Manufacturing Engineering

MOLD FILLING PARAMETERS IN RESIN TRANSFER MOLDING FOR FLIP CHIP SEMICONDUCTOR PACKAGES

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Master of Manufacturing Engineering
(Manufacturing System Engineering)

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MOLD FILLING PARAMETERS IN RESIN TRANSFER MOLDING FOR FLIP CHIP SEMICONDUCTOR PACKAGES

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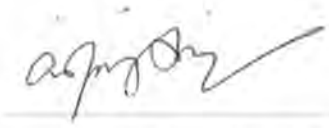
Signature : 

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DEDICATION

To my beloved parents, wife and two lovely kids.

ABSTRACT

Flip chip technology is always been the preferred option for semiconductor packaging technology due to its advantages in both material and manufacturing cost compare to wire bonding interconnect technology. Inversely, flip chip technology with chip flipped and attached to substrate provides a gap in between chip and substrate which cause resistances for molding compound to fill in. The incomplete filling allows air and moisture to be trapped into the gap and subsequently cause product functional failure when it is subject to reliability stress. Alternative approach which can be applied to counter this challenge is the application of capillary underfill (CUF). However, this approach applied higher manufacturing cost due to additional material and process needed. A conventional transfer molding process which offer less cost and processes is possible to counter this challenge. A detail understanding of the molding parameters is required to influence and improve the incomplete filling. An experiment designed using Design of Experiment (DOE) was carried out to evaluate the impact of the key parameters towards incomplete mold size. Key parameters which is temperature, transfer pressure and transfer time were selected as input factors of the DOE. Different chip sizes were covered in the DOE. Output response of the DOE was the incomplete mold size. A significance of each key parameter to the output response was studied. Transfer pressure appeared to be the most significant factor followed by the interaction between temperature and transfer pressure. A prediction model which consists of the significant input parameters was established and validated. The model was found to be fit to predict incomplete mold size within the input parameters range.

ABSTRAK

Teknologi flip chip lazimnya menjadi pilihan untuk pembungkusan semikonduktor kerana kelebihannya dalam penjimatan kos bahan dan pembuatan jika dibandingkan dengan teknologi sambungan wayar. Sebaliknya,terdapat satu jurang antara cip dengan substrat yang mejadi rintangan untuk pengisian kompound mold bagi teknologi flip chip dengan cip diterbalikkan dan dilampirkan kepada substrat. Pengisian yang tidak lengkap memholehkan udara dan kelembapan terperangkap dalam jurang dan seterusnya menyebabkan produk gagal berfungsi apabila dikenakan tekanan. Salah satu penyelesaian alternatif ialah menggunakan kapilari underfill (CUF). Akan tetapi, kaedah ini menggunakan kos pembuatan yang tinggi disebabkan penambahan bahan dan proses. Kaedah konvensional dengan proses transfer molding yang menggunakan kos dan proses yang rendah boleh menangani masalah ini. Pemahaman yang terperinci atas parameter molding diperlukan untuk mempengaruhi dan membaiki pengisian yang tidak lengkap. Satu eksperimen yang direka dengan menggunakan Design of Experiment (DOE) digunakan untuk mengkaji impak parameter utama ke atas pengisian tidak lengkap. Parameter utama termasuk suhu, tekanan dan kelajuan dipilih sebagai factor input. Cip dengan size berlainan dirangkumi dalam DOE. Respon output adalah size pengisian yang tidak lengkap. Kepentingan parameter utama ke atas respon output dikaji. Tekanan adalah factor utama diikuti oleh interaksi antara suhu dan tekanan. Model dengan input yang ketara dijanakan dan disahkan. Didapati model sesuai untuk menjangkakan saiz pengisian tidak lengkap di dalam julat yang dihadkan.

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CHAPTER 1

INTRODUCTION

1.1 Background of Study

Flip chip technology is always been the preferred option for semiconductor packaging technology due to its advantages in both material and manufacturing cost compare to wire bonding interconnect technology. Inversely, flip chip technology with chip flipped and attached to substrate provides a gap in between die and substrate which cause resistances for molding compound to fill in. The incomplete filling allows air and moisture to be trapped into the gap and subsequently cause product functional failure when it is subject to reliability stress. A conventional transfer molding process which offer less cost and processes is possible to counter this challenge.

Encapsulation or molding is a core process in semiconductor chip manufacturing. The main role of molding process is to encapsulate and protect the active area which include the chip, interconnects and leadframe from external damaging factors such as moisture and mechanical stress. Mold compound is used to encapsulate active region during molding process. Although several researches had been carried out to investigate the molding parameter factors causing incomplete mold filling, the experimental verification particularly on the flip chip package had not been demonstrated. This project is to investigate the influence of molding parameters on incomplete filling through experiment.

1.2 Problem Statement

Along with the growth of flip chip technology, mold filling under the flip chip is a concern topic that frequently being raised and discussed nowadays. Incomplete filling is the one of the common manufacturing defects for flip chip. Due to the package design construction with active chip circuitry surface facing narrow gap between the chip and bottom, the incomplete fill defects is even much critical. Several quality and reliability risks such as delamination, package cracking (pop-corning) and electro-migration potentially caused by incomplete mold or void (Ardebili & Pecht, 2009). Apart of the reliability concern, the incomplete filling also elevated the risk at solder joint (Braun et al., 2006).

The active region, between chip's surfaces to the bottom package surface, is the most difficult area for mold compound to fill in. The arrangement of the solder joints coupled with narrow clearance resist the large fillers that present in mold compound to fill in. On top of that, the viscosity of the epoxy resin increases when subject to high temperature. This causes poor mold compound wetting and adhesion to the surface in the active region. Furthermore, the development of flip chip packages towards continuous increment of solder joint quantity and pad arrangement complexity. This uneven solder joint and pad distribution allow air to be trapped in the active region during mold flow. Additional pressure and optimum mold compound rheology is needed to ensure air is removed in the active region (Khor et al., 2014).

On top of the difficulty to detect through optical inspection, x-ray or scanning acoustic microscopy (SAM), such defects also not able to be screened out effectively through tighten test limit during production. A very stringent and thorough reliability test which include temperature humidity bias (THB), autoclave (AC), temperature cycle (TC), high temperature operating life (HTOL) tests are required as captured in AEC-Q100 rev H

to assess the risk of such molding defects (Automotive Electronics Council, 2014). Therefore, thorough and detail parameter characterization is needed at the very beginning phase of the product introduction.

1.3 Objectives of the Study

The main objectives of this research:

i) To study the correlation of temperature, transfer pressure and transfer time towards incomplete mold fill

ii) To develop the correlation model based on experiment

iii) To validate the correlation model based on experimental data

1.4 Scope of the Study

This research project focused on the factors that influence incomplete mold on flip chip package. Three molding parameters namely temperature, transfer pressure and transfer time were selected to be evaluated. Package design construction, mold compound material and molding equipment were set to be constant in this evaluation.

Before molding process, samples were built using standard manufacturing process flow to reflect the actual production product performance. On top of that, samples also built using production process parameter and equipment to reduce the variation.

The correlations between each parameter to incomplete mold were analyzed. Statistical tool was selectively applied to compare the dominancy effect of each mold parameter. The significance influence of each and combination of mold parameters towards incomplete mold were determined.

A prediction model was generated base on the experiment results. The model was then validated using the optimized parameters, within and beyond the input parameters

range. Recommendation of mold parameters was outlined for incomplete mold control. Other contributing factors and responses that indirectly impact on the incomplete mold were discussed. Further study on the effects mold parameter are proposed at the end of the research.

1.5 Significance of the Study

With this research project, field of knowledge on mold parameter towards incomplete mold for flip chip is enhanced. This knowledge is essential and able to serve a fundamental for flip chip mold process window definition. This correlation enables robust and stable process control in manufacturing line. The optimization of the prediction model is the key enabler for continuous improvement to reduce incomplete mold defect in manufacturing line. Moreover, the knowledge also able to provide basic recommendation, guidance or design rule for molded flip chip package development. The corresponding incomplete mold size can be predicted at the design stage. This will eventually avoid unnecessary engineering resources on re-qualification effort and root cause analysis activities.

1.6 Project Planning

The research project activities and timeline are illustrated in Gantt chart in Figure 1.1. The scope, methodology and results are presented in the K-chart in Figure 1.2.

CHAPTER 2

LITERATURE REVIEW

2.1 Flip Chip Technology

Flip chip technology is widely used in the assembly of high performance devices and it can offer excellent advantages such as highest input-output density, enhanced electrical performance and better thermal characteristics (Kao et al., 2004). Figure 2.1 shows the comparison between conventional wire bond packages with flip chip packages.

Figure 2.1: Comparison between flip chip and wire bond package

2.2 Encapsulation of Flip Chip Packages

To encapsulate flip chip package, underfill is needed to fill up the gap under the chip. Much research on underfill has been done which indicate that encapsulation using underfill portrays outstanding package performance with several benefits. Among those, the most significant benefit is the capability of underfill to prolong the fatigue life of flip chip interconnects due to the Coefficient Thermal Expansion (CTE) mismatch between chip and bottom package surface. Without the underfill, the high CTE mismatch causes high stress on the flip chip interconnects especially during temperature cycle where the

interconnect extrusion occurs. On top of that, underfill protects the chip from external environment such as contaminants, humidity and moisture. Therefore, the reliability performances of flip chip packages are improved tremendously with the application of underfill.

The literature on Kao et al. (2004), Chen (2008) and Joshi et al. (2010) show a variety of approaches including capillary underfill (CUF) and mold underfill (MUF) to encapsulate the flip chip packages. Figure 2.2 shows the differences between the two most common types of encapsulation method on one of the flip chip package.

Figure 2.2: Comparison between capillary / no flow underfill with mold underfill

Previous studies indicate that capillary underfill shows better preference in terms of encapsulation method selection. This is because the properties of the capillary underfill material can be customized to the specific function such as narrow gap filling. 30-50um flip chip interconnect standoff height is the typical filing capability for capillary underfill which is much more superior as compare to the normal mold compound, 45-60um (Joshi et al. 2010). For capillary underfill approach, the underfill is dispensed to the periphery of flip chip with designed dispensing pattern and followed by capillary flows under the chip to fill the gaps between flip chip interconnects. Alternatively, underfill can be dispensed on the substrate prior the chip placed at the centre of the underfill and squeeze the underfill to fill up the gap. This approach is described in detail and named as no flow underfill (Wan et al. 2007). Although both approaches show excellence result in flip chip packaging, additional underfill material type instead of conventional mold compound is required. This

also leads to additional process and equipment needed for flip chip packaging. Furthermore, the compatibility of the underfill material with the mold compound material is another technical concern that needed to be addressed. This concern had been raised where the properties of underfill material needed to be optimized with the properties of the mold compound to prevent warpage which subsequently cause delamination (Zhang et al., 2005).

In the last few years there has been a growing interest in mold underfill encapsulation method. Unlike capillary underfill, mold underfill is using the mold compound, the encapsulation material, to fill up the flip chip interconnects area and at the same time encapsulate the entire package. With this, additional underfill material, process, equipment and manufacturing cycle time can be avoided. Several publications have appeared in recent years documenting the comparison between capillary underfill and mold underfill. The results obtained suggests that mold underfill flip chip ball grid array (FCBGA) significantly enhance stress performances to compare with enhanced heat sink FCBGA structure (Kao et al., 2004). It only has 0.10x-0.18x times bump shear stress. Mold underfill FCBGA structure has lower package warpage and the embedded heat sink is effective solution to reduce package warpage. For thermal simulation result, the passive heat sink is effectively to enhance thermal resistance about 38~45% and embedded heat sink mold underfill FCBGA structure shows better thermal performance than without embedded heat sink.

Similarly, it is also prefer to use mold underfill over capillary underfill due to mold underfill offers very promising packaging solution for mobile products such as lower material cost with higher process through put. This resulted the overall mold underfill assembly cost ~20% lower compare to capillary underfill (Joshi et al., 2010). Moreover, mold underfill also demonstrates an excellent reliability up to highly accelerated stress test

192 hours, temperature cycle 1000 cycle and high temperature storage 1000 hours (Joshi et al., 2010).

It has also found that mold underfill FCBGA provides superior solder bump protection and has a higher packaging reliability compared to the capillary FCBGA due to the fact that the molding compound possesses a low CTE and a high modulus (Chen, 2008). According to the simulation results, the maximum stress of the solder bumps, chip and packaging coplanarity of the novel mold underfill FCBGA are a significant improvement in comparison with the capillary underfill FCBGA. However, Chen commented the mold underfill material is more expensive than capillary underfill material which is contradicted to Joshi observation.

2.3 Challenges for Mold Underfill Flip Chip

For several years great effort has been devoted to the study of the challenges in semiconductor molding process. The major challenges on molding for multi-chip module (MCM) is wire sweep failure (Chang & Lee, 2015). With flip chip technology replace wire bond technology, these challenge is overcome. However, flip chip invites other encapsulation challenges. The common challenges are warpage, stress and incomplete mold which are highlighted by several researchers.

Due to the construction of flip chip package, warpage become a major manufacturing concern. Warpage is further elevated for pre-mold coreless substrate based on package where the possible solution is through low CTE with high modulus mold compound (Tang et al., 2014). Molded flip chip BGA (type C-F) structure has lower package warpage than EHS-FCBGA due to mold compound material properties, the higher

Young's modulus can offer enough stiffness to restrain the package warpage (Kao et al., 2004). The recent study, it is concluded that suppressing the thermal expansion of EMC by lowering CTE and raising Tg are effective to reduce package warpage fluctuation during reflow process (Tsuji et al., 2016). In another research, DSC measurement result shows the material cures faster at higher temperature. The molded underfill material can be cured in shorter time. From TMA results showed that as the filler content is increased, the CTE is decreased. As the filler particle size is decreased, the CTE is also decreased. So the CTE of molded underfill material is lower than capillary flow underfill and molding compound materials. Therefore, the CTE mismatch is lower to the substrate. The higher temperature would decrease the modulus of the material. The higher weight loss during curing process would increase the possibility of outgassing which creates the reliability concerns (Liu et al., 2001).

Aside from warpage, stress generated from flip chip technology is also another inherent design weakness for flip chip. This weakness leads to potential reliability failure when flip chip package subject to reliability stress. Previous research share the findings regarding reliability failure where corner cracks were observed on exposed chip mold underfill package after temperature cycle B even using different mold compound type (Kooi et al. 2004). The problem was mitigated through different package construction design. Alternatively, it is also claimed that specific optimized mold compound and underfill materials properties were developed for a flip-chip SIP land array package to counter the failure of pre-conditioning test (Zhang et al., 2005). This conclusion is supported by the findings of mold cap crack after temperature cycling on flip chip packages which is correlated with the mold compound properties (Braun et al., 2006).