Faculty of Electronic and Computer Engineering

OPTIMIZED FAST FOURIER TRANSFORM ARCHITECTURE USING INSTRUCTION SET ARCHITECTURE EXTENSION IN LOW-END DIGITAL SIGNAL CONTROLLER

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in fulfilment of the requirements of the degree of Doctor of Philosophy

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2018

DECLARATION

I declare that this thesis entitled "Optimized Fast Fourier Transform Architecture Using Instruction Set Architecture Extension In Low-End Digital Signal Controller" is the result of my own research except as cited in the references. The thesis has not been accepted for any degree and is not concurrently submitted in candidature of any other degree.

Signature : ……..

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Date : .....

APPROVAL

I hereby declare that I have read this thesis and in my opinion this thesis is sufficient in term of scope and quality for the award of Doctor of Philosophy.

Signature	: ……..
Supervisor Name	: Assoc. Prof. Dr. Soo Yew Guan
Date	: ……..

DEDICATION

To my beloved mother, father and my family

Sharatul Izah

Shahirah Ilyana

Shafiqah Irdina

Shahir Irsyad

ABSTRACT

Smart microgrids have emerged as a viable solution in case of emergency situations occurred at the main electricity grid. The main concern of a smart microgrid is the degradation of the power quality caused by harmonic distortion originated from the non-linear equipment. With the rapid development of power electronic technology, the increased of harmonic-producing loads in the smart microgrids necessitating a new digital signal controller architecture for the harmonic measurement system. While the current system configurations are directed towards the 32-bit architecture, it shows higher requirements in area footprint and multi-core setup. This thesis presents the design of a low-end digital signal controller architecture using instruction set architecture (ISA) extension for the implementation of the harmonic measurement system in a smart microgrid. A new architecture, called UTeMRISC, is developed from the baseline 8-bit microcontroller with the capability to perform signal processing applications such as Fast Fourier Transform (FFT). The architecture is improved using the Application-Specific Instruction Set Processor (ASIP) approach by extending the instruction set architecture to 16-bit length. Instruction set customization is implemented to enable the execution of computationally intensive tasks. The entire architecture is described in Verilog Hardware Description Language (HDL) and implemented on the Virtex-6 FPGA board. From the test programs, UTeMRISC has demonstrated faster execution times and higher maximum operating frequency while not significantly increased the core's resource utilization. Compared to the initial processor architecture, the support of extended ISA has increased the UTeMRISC core by 21.8% but at the same time allows to execute Fast Fourier Transform algorithm up to 5× faster. The combine effort of ISA extension and optimized instruction set generation results in up to 1 Mega sample per second, which translated to 66.8% increase of data throughput in the FFT algorithm when compared to a 32-bit architecture. This research proves that with comprehensive ASIP methodology and ISA extension, a low-end digital signal controller architecture is feasible and effective to be implemented in a harmonic measurement system for a smart microgrid.

ABSTRAK

Mikrogrid pintar telah menjadi penyelesaian yang berdaya maju andai berlaku kecemasan pada grid elektrik utama. Antara isu utama pada mikrogrid pintar adalah pengurangan kualiti kuasa disebabkan herotan harmonik yang bermula daripada peralatan tidak linear. Dengan perkembangan pesat teknologi elektronik kuasa, peningkatan beban yang menjana harmonik memerlukan satu senibina pengawal isyarat digital yang baharu untuk sistem pengukuran harmonik. Walaupun konfigurasi sistem semasa beralih kepada senibina 32-bit, sistem ini memerlukan ruang yang besar dan persiapan berbilang-teras. Tesis ini membentangkan rekabentuk pengawal isyarat digital bawahan menggunakan perluasan senibina set arahan (ISA) bagi perlaksanaan sistem pengukuran harmonik dalam mikrogrid pintar. Senibina baharu ini, dipanggil UTeMRISC, dibangunkan daripada dasar mikropengawal 8-bit dengan kemampuan untuk melaksanakan aplikasi pemprosesan isyarat seperti Jelmaan Fourier Cepat (FFT). Senibina ini ditambahbaik dengan menggunakan Pemproses Set Arahan Spesifik-Aplikasi (ASIP) dan meluaskan senibina set arahan kepada 16-bit. Penyesuaian set arahan dilaksanakan untuk membolehkan pelakuan tugas-tugas pengiraan yang intensif. Keseluruhan senibina dibangunkan dalam bahasa perihalan perkakasan (HDL) Verilog dan dilaksanakan pada papan FPGA Virtex-6. Berdasarkan program-program ujian, UTeMRISC menunjukkan masa pelakuan yang lebih pantas dan frekuensi operasi yang lebih tinggi di samping tidak menaikkan penggunaan sumber dengan nyata. Berbanding dengan senibina pemproses permulaan, sokongan perluasan ISA telah meningkatkan teras UTeMRISC sebanyak 21.8% tetapi pada masa yang sama perlaksanaan algoritma FFT adalah 5× lebih pantas. Gabungan perluasan ISA dan penjanaan set arahan yang optimum menghasilkan daya pemprosesan data sehingga 1 juta sampel per saat, bersamaan dengan kenaikan 66.8% daya pemprosesan data dalam algoritma FFT apabila dibandingkan dengan senibina 32-bit. Kajian ini membuktikan bahawa dengan kaedah ASIP yang komprehensif dan perluasan ISA, senibina pengawal isyarat digital bawahan adalah senibina tersaur dan efektif untuk dilaksanakan dalam sistem pengukuran harmonik bagi mikrogrid pintar.

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LIST OF ABBREVIATIONS

ALU	-	Arithmetic Logic Unit
ASIC	-	Application Specific Integrated Circuit
ASIP	-	Application Specific Instruction Set Computer
DSC	-	Digital Signal Controller
DSP	-	Digital Signal Processing
FPGA	-	Field Programmable Gate Array
HDL	-	Hardware Description Language
LUT	-	Look-up Table
MAC	-	Multiply-Accumulate
PC	-	Program Counter
RISC	-	Reduced Instruction Set Computer

LIST OF PUBLICATIONS

The research papers published during the course of this research are as follows: -

1. Salim, S. I. M., Soo, Y. & Samsudin, S. I., 2018. Instruction Set Extension of a Low-End Reconfigurable Microcontroller in Bit-Sorting Implementation. *International Journal of Electrical and Computer Engineering (IJECE)*, 8, pp. 2595-2601.
2. Salim, S. I. M., Soo, Y. & Samsudin, S. I. 2018. Application Specific Instruction Set Processor (ASIP) Design in an 8-bit Softcore Microcontroller. *Journal of Telecommunication, Electronic and Computer Engineering (JTEC)*, 10, pp. 57-61.
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CHAPTER 1

INTRODUCTION

1.1 Power Quality on Smart Microgrid System

In the power distribution field, microgrids are small-scale versions of the centralized electricity system. The main functions of microgrids are to generate, distribute and regulate the electricity to the end-users. Microgrids are defined as interconnected networks of distributed energy systems (loads and resources) that can function whether they are connected to or separate from the electricity grid (Farhangi, 2010). The flexibility in the implementation provides increase capacity, reliability and efficiency in the power distribution. In terms of deployment, microgrid is rapidly taking hold worldwide (Patel, 2018). Reportedly, there are 1,869 projects are currently operating, under development, or proposed across 123 countries in the fourth quarter of 2017. These projects representing a total capacity of 20.7 GW worldwide, and increase from 18GW recorded in the second quarter of 2016. The increase in power capacity indicated that the microgrid system is relevant and in demand for global deployment.

Microgrids have emerged as a powerful platform in power system community as a viable solution in case of emergency situations occurred at the main grid. Naturally, under critical or unforeseen circumstances where the main grid is unable to meet the demands because of catastrophes or uncertainties, a microgrid can be operated for reliable and continuous power supply. During normal operations, the microgrid enables load sharing with the main grid to offer efficient performance (Hare et al., 2016). The microgrids also

function as a complement to the existing electricity grid and coexist to provide more capabilities, functionalities and capacities.

Power quality has been instrumental in our understanding of improving the microgrid system. Power quality can be defined as a set of electrical boundaries allowing equipment to function in its intended manner with no significant loss of performance or life expectancy (Durdhavale and Ahire, 2016). In relation to the continuous demand for electricity, there is pressure on the utility to set up more generating plants and distribution capacity. Fundamentally, the power quality is compromised when any deviation from the perfect sinusoidal waveform occurred at the loads-end hence causing harmonic distortion. The issue of harmonic distortion that affects the power quality has received considerable critical attention as the number of harmonics-producing loads has increased in recent years (Sinha et al., 2016, Reddy and Barai, 2016, Durdhavale and Ahire, 2016, Bo and Jinhui, 2016, ZhiHui and JianShe, 2013).

A key aspect of micro-grids is the incorporation of sensing, control and communication technologies which lead to the emergence of smart microgrids. Mostly all micro-grids have a large penetration of renewable energy sources and power electronics converters. Non-linear loads such as computers, chargers, current limiters and various power electronics devices that are added to the smart microgrids contributed to the degradation in the quality of power supply. These components are the source of harmonics due to their non-linear property. The detection of harmonic components is conductive to the assessment of power quality (Ming and Jing, 2011). Therefore, it is important to monitor the total distortion level of these sources as faults and failures can occur in the microgrids without early warnings.

A primary concern of harmonics is that it is difficult to reduce. However, the power quality deteriorated because of the existence of the harmonics. Earlier failure of equipment

and losses in distribution systems could be impacted by the harmonics. Therefore, the harmonics should be detected at early stages (Durdhavale and Ahire, 2016). Moreover, with the number of harmonics-producing components in the smart microgrid setup is increasing from year to year, it is important to analyse the influence of these devices (in terms of harmonics) when making any additions or changes to a smart microgrid.

1.1.1 Power System Harmonic Measurement

In recent years, researchers have shown an increased interest in harmonic measurement to improve the power system. Proper detection and mitigation of power quality issues such as voltage sags, swell and harmonics have also been researched in recent times. The main target is to improve the computation to be more reliable and performed quick analysis (Sinha et al., 2016).

A lot of researches have been done on harmonic analysis, measurement and its mitigation techniques within the smart microgrid. Within these systems, one of the widely used algorithms harmonic analysis is the Fast Fourier Transform (FFT). Through FFT calculations, the amplitude of the fundamental frequency and the *n*th order harmonic are identified. The harmonic distortion also can be calculated using the ratio of the amplitude of the measured harmonic to the fundamental frequency.

The FFT algorithm is can be executed on the various platforms either by using general-purpose processors, dedicated microcontrollers or digital signal processors. Between these platforms, the execution of FFT algorithms produced a varying degree of accuracy and output throughput, depending on the processor's architecture and their programming capability. For example, a general-purpose processor would be able to run the FFT algorithm but at much lower speed when compared to digital signal processor's execution. The lack of speed is mainly due to the non-existence of complex-computational units, such as multiply-and-accumulate module, which is the main feature in the digital

signal processor's architecture. Nonetheless, the FFT algorithms still workable on the general-purpose processor but with the certain limitation that can be tolerated depending on the target application.

However, recent developments in ubiquitous devices have heightened the need for a low-cost and compact hardware to implement the signal processing needed to perform the harmonic measurements, especially in a smart microgrid system. The emergence of Internet-of-Things (IoT) has accelerated the integration of multiple sensors to a node in the smart microgrid. Therefore, the processor that powered the node needs to have the capacity to integrate various sensors and communication modules. The architecture also must handle the pre-processing task for the input signals while at the same time maintaining a small footprint and acceptable output performance.

The processing architecture limits the performance of the harmonic measurements. Deploying full-blown hardware in the smart microgrid field is impractical while implementing the intensive processing task on the low-end hardware would jeopardize the execution speed. It is favourable to have an architecture that supports computational tasks, and at the same time, it needs to be optimized in term of output accuracy, board size and data throughput. Recent trends in processor architecture have led to a proliferation of studies that enable such complex calculation to be performed in an embedded system. However, focusing on the smart micro-grids applications, specific configurations must be adhered to optimize the system's solution.

1.2 Simple FFT Algorithm for Microcontrollers

FFT is one of the most important algorithms in the world because it efficiently calculates the frequency components of time-varying signals. Even a small acceleration of the FFT algorithm greatly speed up the whole application. In most cases, the digital signal processor and other high-end platform are used as the executed platform to perform the

FFT algorithm periodically. Executing FFT in a high-end platform is acceptable if the targeted applications do not confine itself to the certain time-response requirement, accuracy points and board size limitation. However, for the smart microgrid application, several constraints need to adhere to the system. According to Sinha et al. (2016), a power system harmonic measurement device should have the three functions; (i) signal can be sampled in power at any time, (ii) it can quickly and accurately analyse parameters including voltage and current in the power, and, (iii) the analysis result can be displayed directly. In general, operating as a remote system from the main electricity grid, a smart microgrid system is beneficial in having a stand-alone and comprehensive main controller that is capable of processing and analysing real-time signal locally. These functions required optimum processor architecture that can execute complex calculation with minimal resource utilization.

Apart from hardware optimization, the FFT algorithm itself must be enhanced to match the low-end architecture that will be deployed in the smart microgrid. Suto et al. (2014) presented an algorithm of FFT which contains a reduced number of logical and elementary (addition, subtraction, multiplication) operations. It is also optimized to the low-level programming and hardware description language. The algorithm is well applicable in FPGAs, microcontrollers, digital signal controllers and any mini-computers which requires fewer resources but capable of delivering good performance in harmonic measurement. The customized algorithm opens up new possibilities in improving the FFT algorithm within limited resources, which suited to the requirement of the smart microgrid.

1.3 Processor Architecture

In order to accurately monitor real-time power harmonics and precisely grasp the harmonic wave, the harmonic measurement system mostly based on the combination of DSP and Advanced RISC Machine (ARM) processor (Rajagopal and Singaravelu, 2015,