Faculty of Electrical Engineering

MODIFIED CASCADED H-BRIDGE MULTILEVEL INVERTER USING PARTICLE SWARM OPTIMIZATION

Mohammed Rasheed Jubair Al-Hiealy

Doctor of Philosophy

2018

MODIFIED CASCADED H-BRIDGE MULTILEVEL INVERTER USING PARTICLE SWARM OPTIMIZATION

MOHAMMED RASHEED JUBAIR AL-HIEALY

A thesis submitted
in fulfillment of the requirements for the degree of Doctor of Philosophy

Faculty of Electrical Engineering

UNIVERSITI TEKNIKAL MALAYSIA MELAKA

2018

DECLARATION

I declare that this thesis entitled "Modified Cascaded H-Bridge Multilevel Inverter Using Particle Swarm Optimization" is the result of my own research except as cited in the references. The thesis has not been accepted for any degree and is not concurrently submitted in candidature of any other degree.

Signature : ….....

Name : Mohammed Rasheed Jubair Al-Hiealy

Date : ….....

APPROVAL

I hereby declare that I have read this thesis and in my opinion this thesis is sufficient in term of scope and quality for the award of Doctor of Philosophy.

Signature :……..……

Supervisor Name :Assoc. Prof. Ir. Dr. Rosli Bin Omar

Date :……...……..……

DEDICATION

To my beloved father, mother, brothers, sisters.

ABSTRACT

For more than two decades, multilevel inverters in different topologies and control strategies have been involved in many applications. In contrast to conventional three-level inverters, they are more efficient and better suited for applications requiring high power and high voltage levels. The current multilevel inverter topologies available in the market include diode clamped or neutral point clamped (NPC), capacitor clamped or flying capacitor (FC), and cascaded H-bridge (CHB). It is essential to produce an effective power converter from the perspective of cost, efficiency and output quality. These factors have lead to develop a new family of multilevel inverters known as modified CHB-MLIs of a single and three phases for five, nine and thirteen levels. This topology of the modified inverters requires fewer components compared to existing inverters (particularly in the higher levels) and requires fewer carrier signals and gate drives. Therefore, the overall cost and complexity are greatly reduced, particularly for higher output voltage levels. An important issue in the power electronic converters is the modulation control method in order to produce high quality output with a minimum distortion. As there exist many strategies for modulation, still the low-switching frequency technique is widely accepted in higher power applications. There are different optimization aims for different applications utilizing the low-switching frequency technique it is possible to increase the number of output voltage levels and produce a better sinusoidal output waveform and efficiency. The modified CHB-MLIs for five, nine and thirteen levels have a reduced number of DC power supplies and switches when compared to the conventional CHB topologies designed for the same number of voltage levels. The aim of this thesis is to investigate the performance of modified CHB-MLIs of a single and three phases for five, nine and thirteen levels based on cascaded multilevel inverter using low-switching frequency modulation scheme. The modulation method for obtaining the optimum switching angles based on Newton Raphson (NR) and Particle Swarm Optimization (PSO) control techniques have been proposed. A NR and PSO control techniques were presented for selective harmonics elimination (SHE) solution in a modified CHB-MLIs. These control techniques have been implemented through closed-loop control system using DSP TMS320F2812. In this thesis, the complete switching angles of the SHE has been developed by using a heuristic optimization technique namely PSO by solving the non-linear equation of the output voltage waveform and later validated with the conventional method NR. To validity of a low power prototype of the modified CHB-MLIs have been designed and implemented; analytical, simulation, and experimental results have been provided. The relative merits of the proposed modulation scheme based on the NR and PSO have been assessed based on modified inverters output quality and efficiency. Investigations of the proposed modulation scheme based on PSO have been revealed that the switching pattern of the adopted inverters has the capability of producing output voltage with minimal THD and high efficiency of the modified inverters. The results acquired from the simulation results the superiority of PSO over the conventional methods NR, where the THD reduction values in the three developed CHB-MLI namely five-level, nine level, and thirteen level are 15%, 7.8%, and 5.2%, respectively.

ABSTRAK

Lebih dari dua dekad penyongsang pelbagai peringkat dalam topologi dan kawalan strategi yang berbeda telah banyak terlibat dalam applikasi. Bertentangan dengan penyongsang tiga aras konvensional , penyongsang pelbagai aras adalah lebih cekap dan a mat sesuai penggunaannya untuk kuasa tinggi dan paras voltan tinggi.Topologi penyongsang pelbagai peringkat yang terdapat dipasaran sekarang adalah termasuk diod diapit atau titik neutral diikat(NPC),kapasitor diikat atau kapasitor terbang(FC) dan penyongsang pelbagai peringkat Jambatan-H sambungan LataCHB.Adalah amat penting untuk menghasilkan penyongsang kuasa yang berkesan dari segi persepektif kos,kecekapan dan kualiti keluaran.Faktor-faktor ini mempengaruhi untuk memajukan satu keluarga baru pengyongsang pelbagai aras yang dikenali sebagai penyongsang pelbagai peringkat Jambatan-H sambungan Lata (CHB-MLI) yang diubah suai untuk fasa tunggal atau tiga fasa bagi aras lima,Sembilan dan tigabelas. Topologi ini bagi penyongsang yang diubahsuai memerlukan kurang komponen berbanding penyongsang yang terdapat dipasaran sekarang(terutamanya untuk aras yang lebih tinggi) dan ianya memerlukan kurang isyarat pembawa dan pemacu pintu. Oleh sebab itu kos keseluruhan dan kerumitan dapat dikurangkan terutamanya untuk aras voltan keluaran tinggi. Isu yang lebih penting dalam elektonik kuasa ialah kaedah kawalan modulasi kearah menghasilkan keluaran kualiti tinggi dengan minimum keherotan.Seperti banyak strategi modulasi yang ada sekarang, teknik pengyuisan frekuensi rendah masih digunakan secara meluas untuk penggunaan kuasa tinggi. Terdapat perbezaan pengoptimun bertujuan untuk penggunaan yang berbeza dengan menggunakan teknik penyuisan frekuensi rendah. Adalah tidak mustahil untuk meningkatkan bilangan paras voltan keluaran dan menghasilkan gelombang dan kecekapan output sinusoidal yang lebih baik.CHByang telah diubahsuai untuk aras lima, sembilan dan tiga belas mempunyai bilangan bekalan kuasa DC dan suis yang dikurangkan apabila dibandingkan dengan topologi CHB konvensional yang direka untuk bilangan voltan yang sama. Tujuan tesis ini adalah untuk menyiasat prestasi CHByang diubahsuai untuk satu dan tiga fasa untuk aras lima, sembilan dan tiga belas berdasarkan penyongsang pelbagai peringkat dengan menggunakan skim modulasi frekuensi rendah. Kaedah modulasi untuk mendapatkan sudut pensuisan optimum berdasarkan teknik-teknik Newton Raphson (NR) dan Pengoptumunan kelompok zarah (PSO) telah dicadangkan. Teknik –teknik kawalan NR dan PSO telah dibentangkan untuk penyelesaian SHEdalamCHByang diubah suai. Teknik kawalan Penyongsang telah diubahsuai telah digunakan untuk peringkat lima hingga tiga belas aras bagi CHB-MLIs yang telah diubahsuai. Teknik kawalan ini telah dilaksanakan melalui sistem kawalan gelung tertutup menggunakan DSP. Dalam tesis ini, sudut pensuisan yang lengkap untuk penyelesaian penghapusan harmonik terpilih (SHE) diterbitkan menggunakan teknik pengoptimuman heuristik iaitu PSO dengan menyelesaikan persamaan tidak serentak dari gelombang voltan keluaran dan kemudian disahkan menggunakan teknik konvensional NR. Untuk mengesahkan kesasihan prototaip kuasa rendah CHB-MLIs yang telah dimodifikasi reka bentuk dan dilaksanakan; analisis, simulasi, dan keputusan experimen seperti disediakan.Kebaikan relatif skim modulasi yang dicadangkan berdasarkan NR dan PSO telah dinilai berdasarkan kualiti dan kecekapan keluaran penyongsang yang diubah suai. Penyelidikan skim modulasi yang dicadangkan berdasarkan PSO telah membuktikan bahawa sistem penyuisan penyongsang yang diterima pakai mempunyai keupayaan menghasilkan voltan keluaran denganTHDyang minimum dan kecekapan tinggi dalam penyongsang yang diubahsui. Keputusan diperoleh daripada hasil simulasi dari kelebihanPSOmelalui kaedah konvensional NR,di mana nilai pengurangan THD dalam tiga CHB-MLI yang dibangunkan iaitu tahap lima, sembilan tahap, dan tahap tiga belas adalah 15%, 7.8%, dan 5.2% secara keseluruhannya.

ACKNOWLEDGEMENTS

Thanks ALLAH

My utmost thanks and gratitude must first be offered to Almighty Allah for all his blessings, and in granting me good health throughout the duration of this research.

I would like to express my gratitude to my supervisor Assoc. Prof. Ir. Dr. Rosli Bin Omarand my co-supervisor Prof. Ir. Dr. Marizan bin Sulaimanfor their advice, encouragement, valuable ideas, guidance, and patience shown to me throughout this project. I appreciate their vast knowledge and skills.

I would also like to thanktheUniversiti Teknikal Malaysia Melaka (UTeM) for Zamalah award. I would also like to thank my family for the support they provided me through my entire life and in particular Father and Mother, without whose love, encouragement. I must also acknowledge my friends for their support and assistance to finish this thesis.

TABLE OF CONTENTS

	PAGE
DECLARATION	
APPROVAL	
DEDICATION	
ABSTRACT	**i**
ABSTRAK	**ii**
ACKNOWLEDGEMENTS	**iii**
TABLE OF CONTENTS	**iv**
LIST OF TABLES	**viii**
LIST OF FIGURES	**x**
LIST OF ABBREVIATIONS	**xxvi**
LIST OF PUBLICATIONS	**xxvii**
CHAPTER	
1. INTRODUCTION	**1**
1.1 Introduction	1
1.2 Problem Statements	5
1.3 Objectives of Research	6
1.4 Motivation of Research	7
1.5 Scope of Research	8
1.6 Contribution of Research	8
1.7 Thesis Outline and Organization	10
2 LITERATURE REVIEW	**12**
2.1 Introduction	12
2.2 Modelling PV Cell or Module	12
2.3 Characteristic PV Cell	16
2.4 Inverter for PV System	19
2.5 SCBased Energy Storage	21
2.5.1 SC Construction	22
2.5.2 SC Versus Battery	25
2.6 Overview to Converter for Multilevel Inverter Application	27
2.7 DC-DC Converter	27
2.7.1 Step-down (buck) Converter	28
2.7.2 Step-up (boost) Converter	31
2.7.3 Step-Down/Step-up (buck-boost) Converter	33
2.8 Inverters	35
2.9 Voltage Control of Single-Phase Inverters	36
2.9.1 Single-Pulse-Width Modulation	37
2.9.2 Multiple-Pulse-Width Modulation	38
2.9.3 Sinusoidal Pulse-Width Modulation	39
2.9.4 Modified Sinusoidal Pulse-Width Modulation	41

2.9.5 Phase-Displacement Control 41
2.10PV Inverters 43
2.11Maximum Power Point Tracking (MPPT) 43
2.11.1 Perturb and Observe (P&O) 44
2.11.2 Incremental Conductance (INC) 46
2.11.3Constant Voltage (CV) 49
2.12Multilevel Inverter Topologies 50
2.12.1 Multilevel Inverter Using Diode-Clamped 51
2.12.2 Flying Capacitors Multilevel Inverter 54
2.12.3 Multilevel Converter Using Cascaded-Inverterswith Separated DC Sources 58
2.12.4 Generalized Multilevel Inverters 62
2.12.5 Series-Stacked-Converter 63
2.12.6 Emerging Multilevel Inverter Topologies 64
2.12.7 Soft-Switched Multilevel Inverters 66
2.13Modulation Technique for Multilevel Inverter 67
2.13.1 Sinusoidal Pulse Width Modulation (SPWM) 68
2.13.2 Space Vector PWM 68
2.13.3 Multilevel SPWM 71
2.13.4Selective Harmonic Elimination (SHE)71
2.14 Global Optimization Methods 74
2.14.1 Particle Swarm Optimization 75
2.15Critical Review of Literature Studies 79
2.16Summary 91

3 RESEARCH METHODOLOGY 92
3.1 Introduction 92
3.2 Overall Research Methodology 93
3.3 PV System Modelling 96
3.4 Simulations of *I-V* Curves and *P-V* Curves 101
3.5 Analysis of the DC-DC Boost Converter 107
3.5.1 A Continues Conduction Mode (CCM) 108
3.6 Designed and Development of a DC-DC Boost converter 110
3.6.1 DC-DC Boost Converter Based on Matlab/Simulink Model 111
3.7 SC Model 112
3.7.1 Main Capacitance 114
3.8 The Modified CHB-MLIs 115
3.8.1 Five Levels Modified CHB-MLIs 115
3.8.2 A Single Phase Nine Levels Modified CHB-MLIs 117
3.8.3 A Single Phase 13-Levels Modified CHB-MLIs 118
3.9 Principle of a Modified CHB-MLIs 119
3.9.1 A Five-Level Modified CHB-MLIs 119

3.9.2 Nine-Levels Modified CHB-MLIs 123
3.9.3 13-Levels Modified CHB-MLIs 129
3.10NR Algorithm for Development Thirteen Levels Modified CHB-MLIs 137
3.11Particle Swarm Optimization (PSO) Technique 142
3.12Selective Harmonic Elimination (SHE) of Modified of Single and Three Phases 149
3.13Development of Selective Harmonic Elimination (SHE) 150
3.14Efficiency of Modified CHB-MLIs 154
3.15Simulink Model of the Modified CHB-MLIs 154
3.16Overall Simulation of the Proposed System 157
3.17Hardware Development of the Proposed Modified Five, Nine, and 13 CHB-MLIs158
3.17.1The Gate Drive for IGBT 159
3.17.2The Printed Circuit Board (PCB) 160
3.18Super Capacitor (SC) 167
3.19Hardware Implementation of DC-DC Boost Converter 168
3.20PV Simulator 169
3.21The Overall Experimental Set-up 170
3.22Summary 172

4RESULTS AND DISCUSSION 173
4.1 Introduction 173
4.2 Simulation results of PV Generation 173
4.3 Simulation of a DC-DC Boost Converter 176
4.4Simulation Results for Optimization of a single phase modified CHB-MLIs for FiveLevels model with MI= 0.949 based on NR and PSO techniques 180
4.5Simulation Results for Switching Angle Optimization of a Three-Phase of Modified CHB-MLIs for Five Levels Model with MI= 0.949 Based on NR and PSO Techniques 185
4.6 Simulation Results of Nine Levels Modified CHB-MLIs (MI=0.949) using NR and PSO Techniques. 194
4.7 Simulation Results of 13-levels Modified CHB-MLIs (MI=0.81) using NR and PSO Techniques 200
4.8 Experimental Results 209
4.9 Experimental Results of a Single Phase and Three Phase of Five Level Modified CHB-MLIs with MI Value Is Equal 0.949 Based on NR And PSOTechniquesTechniques 222
4.9.1Switching Angles and THD for Single Phase 5-Level Modified CHB-MLIs using NR and PSO Techniques 223
4.9.2Experimental Results of a Single Phase Five Levels Modified CHB-MLIs for (MI=0.949) which optimised by NR and PSOTechniques 224

4.9.3Optimization Experimental Results of a Three Phase Five Level of Modified CHB MLIs (MI=0.949) Based on NR and PSO Techniques 229
4.9.4Switching Angles and THD of a Single Phase 9-Levels Modified CHB-MLIs for using NR and PSO Techniques. 240
4.9.5Experimental Results of a Nine Levels ModifiedCHB-MLIs for (MI=0.949) using NR and PSO Techniques. 240
4.9.6Switching Angles and the Values of THD of single phase Thirteen levels a Modified CHB-MLIs for using NR and PSO Techniques. 246
4.9.7Optimization Experimental Results Thirteen Level Modified CHB-MLIs for (MI=0.81) using NR and PSO Techniques 247
4.10Efficiency of Modified CHB-MLI 256
4.11Summary 261

5 CONCLUSION AND RECOMMENDATION 262
5.1 Introduction 262
5.2 Conclusion 262
5.3 Achievements of Research Objectives 263
5.4 Recommendation of Future Works 264

REFERENCES 266
APPENDICES 282

LIST OF TABLES

TABLE	TITLE	PAGE
2.1	Summary of P&O MPPT algorithm	45
2.2	Diode-clamped 5-level converter voltage levels and their switch states	52
2.3	A possible switching combination for the 5-level flying capacitor converter	57
2.4	PSO Parameters Selection	79
2.5	Critical Review of Literature Studies and compare with proposal thesis.	79
3.1	Standard test condition.	101
3.2	Characteristics and specifications of PV module from datasheet.	102
3.3	Proposed boost converter parameters.	112
3.4	Various values of power (P (kW)).	114
3.5	Output voltages of five levels modified CHB-MLIs.	121
3.6	Output voltage of nine-levels modified CHB-MLIs.	124
3.7	Output voltages 13-levels modified CHB-MLIs.	132
3.8	The values of MI, switching angles, and THD for voltage of a modified CHB-MLIs for 13 levels based on NR techniques.	141
3.9	The values of MI, switching angles, and THD for voltage of a modified CHB-MLIs for nine-level based on NR techniques	141
3.10	The values of MI, switching angles and THD for voltage of a modified CHB-MLIs for five levels based on NR techniques.	141

3.11	The values of MI, switching angles and THD for voltage of a modified CHB-MLIs for 5, 9 and 13-levels based on PSO techniques.	145
3.12	Parameters of PSO.	145
3.13	Optimization of switching angle for different modulation index.	153
3.14	Switching angle for different harmonic elimination.	153
3.15	THD of the H-Brigid multilevel inverter for different levels.	162
3.16	System parameters proposed.	172
4.1	Simulation parameters of proposed boost converter.	176
4.2	The values of various output voltage based on duty cycle.	179
4.3	The different THD based on modulation index (MI).	208
4.4	Various MPP system efficiency of the PV simulator	222
4.5	The values of MI, switching angles, and THD for voltage of five levels modified CHB-MLIs which optimised by NR and PSO techniques.	224
4.6	The values of MI, switching angles, and THD for voltage of a nine -level modified CHB-MLIs based on NR and PSO techniques.	240
4.7	Voltage of a modified CHB-MLIs for 13-levels based on calculation NR and PSO techniques.	247
4.8	Overall values of MI, switching angles and THD for voltage of modified	255
4.9	Efficiency of the five-level modified CHB-MLI.	256
4.10	Efficiency of the nine-level modified CHB-MLI	258
4.11	Efficiency of the 13-level modified CHB-MLI.	259
4.12	Compare for different result based on THD.	260

LIST OF FIGURES

FIGURE	TITLE	PAGE
2.1	The equivalent circuits model for PV cell (a) The single -diode model; (b) The double-diode model.	12
2.2	The simplified equivalent circuit PV model.	13
2.3	I-V curve of a solar cell.	13
2.4	PV cell operating point.	14
2.5	Equivalent circuit diagram during open circuit condition.	14
2.6	Equivalent circuit diagram during short circuit condition.	15
2.7	Intersection of the Ipv-Vpv characteristic curve and the load characteristic.	16
2.8	I-V characteristics of a photovoltaic cell array for various values of irradiance S at a temperature of 250C, Case of KD135GX-LPU (Krismadinataa*, Nasrudin Abd. Rahima Hew Wooi Pinga, 2013).	17
2.9	I-V characteristics of a photovoltaic cell array for various values of temperature T at an irradiance of 1000W/m2, Case of KD135GX-LPU (Krismadinataa, Nasrudin Abd. Rahima Hew Wooi Pinga, 2013).	17
2.10	P-V characteristics of a photovoltaic cell array for various values of irradiance S at a temperature of 25 °C, Case of PV-UE125MF5 (Krismadinataa*, Nasrudin Abd. Rahima Hew Wooi Pinga, 2013).	18
2.11	Square waveform output voltage.	20

2.12	Modified or quasi sine waveform output voltage.	20
2.13	Sine waveform output voltage.	21
2.14	Double layer construction of a SC.	23
2.15	Equivalent circuit of SC	24
2.16	The Construction of Conventional capacitor	25
2.17	Ragone plot of various energy storage devices.	26
2.18	Circuit diagram of a buck converter	30
2.19	Waveforms of a buck converter inductor voltage VL, inductor current IL, capacitor ripple current Ie, and output current I0	30
2.20	Circuit diagram of a boost converter.	32
2.21	Waveforms of a boost converter inductor voltage VL, inductor current IL, capacitor ripple current Ic, and output current Io.	32
2.22	Circuit diagram of a buck-boost converter.	34
2.23	Waveforms of a buck-boost converter's inductor voltage VL, inductor	34
2.24	Single-phase bridge voltage source inverter (VSI).	35
2.25	Output voltage single-phase bridge inverter.	36
2.26	Load current and device conduction with inductive load.	36
2.27	Generation of gating signals and output voltage of a single-phase full bridge inverter through single-pulse-width modulation.	38
2.28	Generation of gating signals and output voltage of a single -phase full-bridge inverter by using multiple-pulse-width modulation.	39
2.29	Generation of gating signals and output voltage of a single-phase full bridge inverter by using sinusoidal-pulse-width modulation	40

2.30	Generation of gating signals and output voltage of a single-phase full bridge inverter by using modified sinusoidal pulse-width modulation.	41
2.31	Generation of gating signals and output voltage of single-phase full bridge inverters by using phase-displacement control.	42
2.32	Sign of the dP/dV at various positions on the power characteristic curve.	45
2.33	Flowchart of P&O MPPT algorithm.	46
2.34	Flowchart of INC MPPT method.	48
2.35	Module I-V curves with varying irradiance.	50
2.36	Diode-clamped multilevel inverter circuit topologies (a) Two-level inverter and (b) n-levels inverte	51
2.37	The node phase output voltage referred to the middle point of the DC bus v_{an} (a) for three levels (b) for five levels.	53
2.38	Capacitor-clamped multilevel inverter circuit topologies (a) Two-level inverter and (b) n-levels inverter.	56
2.39	Circuit diagram and phase voltage waveform of a cascaded-inverters based converter with separate DC sources; (a) circuit diagram and (b) waveform showing a 9-level converter phase voltage.	59
2.40	Cascaded inverter with three-phase cells.	60
2.41	Vector diagram of the systems with the fundamental voltages.	61
2.42	Generalised P2 multilevel inverter structure (P2 refers to the basic cell of a two-level phase leg).	63
2.43	The 2-level SSC with Isolation Transformer.	64

2.44	(a) and (b) a mixed-level hybrid cell configuration using the three-level diode-clamped inverter as the cascaded inverter cell and the waveform of the output phase voltage respectively.	65
2.45	Zero-voltage-switching capacitor-clamped inverter circuit.	67
2.46	Classification of multilevel modulation methods.	68
2.47	Space-vector diagram for two-level inverter.	70
2.48	Space-vector diagram for three-level inverter.	70
2.49	Space-vector diagram for five-level inverter.	70
2.50	A generalised for Selective Harmonic Elimination (SHE).	72
2.51	A positive half-cycle of a seven-level stepped waveform with different modulation indices. (a) High modulation index, (b) Middle modulation index.	74
2.52	PSO Search Space Trajectory (Poli, et.al, 2007)	76
3.1	Block diagram of the overall proposed system.	93
3.2	General flow of the research methodology.	94
3.3	Electrical equivalent circuit of a solar cellSource: (Thulasiyammal et al., 2013).	97
3.4	Current-Voltage (I-V) and Power-Voltage (P-V)	98
3.5	General MPPT procedure.	99
3.6	Flowchart of INC MPPT method.	100
3.7	PV module model for variable irradiance and constant temperature.	102
3.8	MATLAB/SIMULINK blocks of photovoltaic modelling.	103
3.9	Function block parameter for PV module model.	106
3.10	Circuit diagram of step-up DC/DC converter [Adel et al, 2008].	107

3.11	VL and iL waveforms for boost converter in CCM [Rashid., 2004].	108
3.12	The equivalent circuit of mode 1.	108
3.13	The equivalent circuit of mode 2.	109
3.14	A model of a DC-DC boost converter.	112
3.15	The basic circuit model of the SC (EPOCS).	113
3.16	Simulation model of SC.	113
3.17	A Single-phase five-levels modified CHB-MLIs.	116
3.18	A three-phase five-levels modified CHB-MLIs.	117
3.19	A single-phase nine-levels modified CHB-MLIs.	118
3.20	A single-phase thirteen-levels modified CHB-MLIs.	119
3.21	The proposed of a single phase five-levels Modified CHB-MLIs.	120
3.22	Switching pattern of a five-levels modified CHB-MLIs.	121
3.23	Switching operation modes of five-levels modified CHB-MLIs.	123
3.24	The proposed of a single phase nine-levels modified CHB-MLIs.	124
3.25	Switching pattern of nine-Levels modified CHB-MLIs.	125
3.26	Switching operating modes access of nine levels modified CHB-MLIs.	129
3.27	The proposed of a single-phase 13-levesls modified CHB-MLIs	130
3.28	Switching pattern thirteen levels modified CHB-MLIs.	131
3.29	Switching operating modes 13-levels modified CHB.	137
3.30	General flow-chart of NR of the modified CHB-MLIs.	139
3.31	Vab at low switching frequency of algorithm development for 13-levels modified CHB-MLIs.	142
3.32	Overall of angles for 5, 9 and 13-level inverter.	146
3.33	Convergence characteristic for 5, 9 and 13-level inverter.	147

3.34	General flow chart of PSO of a modified CHB-MLIs.	148
3.35	The phase voltage Vab.	151
3.36	Simulations of a three phase of modified CHB-MLIs for five-levels model.	156
3.37	Simulations of modified CHB-MLIs nine-levels model.	156
3.38	Simulations of modified CHB-MLIs thirteen-levels model	157
3.39	The construction of the gate drive of the modified CHB-MLIs.	160
3.40	The values of various number of level with THD	163
3.41	The development of a three-phase of five-levels modified CHB-MLIs.	163
3.42	The development of a single-phase of nine-levels modified CHB-MLIs.	164
3.43	The development of a single-phase of 13-levels modified CHB-MLIs.	164
3.44	DSP TMS 320F2812.	165
3.45	Experimental of input switching pattern of 5 v.	166
3.46	Experimental of output switching pattern of 15 v.	166
3.47	Experimental switching pattern for S1, S2, S3, S4, and S5, 15v.	167
3.48	The construction of the 75 SC module used in this study.	168
3.49	Prototype DC-DC boost converter.	169
3.50	PV Simulator model.	170
3.51	The overall experimental set-up for the prototype of the proposed modified CHB-MLIs system.	171
4.1	Module's I-V curves for various irradiances and constant temperature.	174
4.2	Module's P-V curves for various irradiances and constant temperature.	174
4.3	Module's I-V curves for various temperatures and constant irradiance.	175
4.4	Module's P-V curves for various module temperatures and constant irradiance.	175

4.5	Simulation input voltage equal 21.8v.	177
4.6	Simulation output voltage equal 68.5v.	177
4.7	Output voltage at D = 0.65.	177
4.8	Output voltage at D = 0.55.	178
4.9	Output voltage at D = 0.5.	178
4.10	Output voltage at D = 0.32.	179
4.11	The values of various output voltage based on duty cycle.	179
4.12	Simulation model of timing diagram of a five-level modified CHB-MLIs comprising bi-directional switch S5 and switches S1, S2, S3, and S4 with MI=0.949 using NR technique.	181
4.13	Five-level output phase voltage with MI=0.949 using NR technique.	182
4.14	Optimisation harmonic spectrum of the single-phase output	182
4.15	Simulation model of timing diagram of a modified CHB-MLIs comprising switches S1, S2, S3, and S4 and bi-directional switch S5 with MI=0.975 using PSO technique.	183
4.16	Optimisation of output voltage waveform of a five-level CHB -MLIs with MI=0.975 using PSO technique.	184
4.17	Harmonic spectrum of the optimisation of a single-phase output voltage waveform using PSO technique.	185
4.18	Simulation model of three-phase five-level timing diagram for S1, S2, S3, S4 and bi-directional S5 at phase A with MI=0.949 using NR technique.	186

4.19	Simulation model of three-phase five-level timing diagram for S1, S2, S3, S4 and bi-directional S5 at phase B with MI=0.949 using NR technique	186
4.20	Simulation model of three-phase five-level timing diagram for S1, S2,	187
4.21	Three-phase five-level output phase voltage at phases A, B, and C with MI=0.949 for θ1=14.63130 and θ2=41.34340 using NR technique.	188
4.22	Harmonic spectrum for output phase voltage at phase A waveform output of five levels with MI=0.949 using NR technique.	188
4.23	Three-phase five-level output line to-line voltage at phases A, B, and C with MI=0.949 for θ1=14.63130 and θ2=41.34340 using NR technique.	189
4.24	Harmonic spectrum for output line voltage at three–phase waveform output of five levels with MI=0.949 using NR technique.	189
4.25	Three-phase five-level timing switching diagram for S1, S2, S3, S4, and S5 at phase A with MI=0.975 for θ1=13.4043260 and θ2 =41.9085790 using PSO technique.	190
4.26	Three-phase five-level timing switching diagram for S1, S2, S3, S4, and S5 at phase B with MI=0.975 for θ1=13.4043260 and θ2 =41.9085790 using PSO technique	191
4.27	Three-phase five-level timing switching diagram for S1, S2, S3, S4, and S5 at phase C with MI=0.975 for θ1=13.4043260 and θ2 =41.9085790 using PSO technique.	191
4.28	Simulation results for a three-phase five-level output phase voltage at phases A, B, and C using PSO technique.	192

4.29	Harmonic spectrum for output phase voltage at phase A waveform output of five levels with MI=0.975 using PSO technique.	193
4.30	Simulation results for a three-phase five-level output line voltage at phases A, B, and C for θ1=13.4043260 andθ2 =41.9085790 using PSO technique	193
4.31	Harmonic spectrum of a three-phase modified CHB-MLIs for line-to -line voltage for five levels with MI=0.975 using PSO technique.	194
4.32	Timing diagram of a modified CHB-MLIs of nine levels for cell one comprising S1, S2, S3, S4, and S5 switches with MI=0.949 using NR technique.	195
4.33	Timing diagram of a modified CHB-MLIs of nine levels for cell two comprising S1, S2, S3, S4, and S5 switches with MI=0.949 using NR technique.	196
4.34	The optimisation of output voltage waveform of a nine-level modified CHB-MLIs with mi=0.949 which optimised switching angle NR technique.	197
4.35	Optimisation harmonic spectrum of output voltage waveform of a modified CHB-MLIs with MI=0.949 using NR technique.	197
4.36	Timing diagram of a nine-level modified CHB-MLIs for cell one comprising S1, S2, S3, S4, and S5 switches with MI=0.949 using PSO technique.	198
4.37	Timing diagram of a nine-level modified CHB-MLIs for cell Two comprising S6, S7, S8, S9, and S10 switches with MI=0.949 using PSO technique.	199

4.38	The output voltage waveform of a nine-level modified CHB-MLIs with MI=0.949 which optimised switching angle PSO technique.	199
4.39	Optimisation harmonic spectrum of output voltage waveform of a nine-level modified CHB-MLIs with MI=0.949 using PSO technique.	200
4.40	Switching Pattern of a Thirteen-Level Modified CHB-MLIs for Cell One Comprising S1, S2, S3, S4, and S5 switches with MI=0.81 using NR Technique.	201
4.41	Switching Pattern of a Thirteen-Level Modified CHB-MLI for Cell Two Comprising S6, S7, S8, S9, and S10 switches with MI=0.81 using NR Technique.	202
4.42	Switching pattern of a thirteen-level modified CHB-MLIs for cell three comprising S11, S12, S13, S14, and S15 switches with MI=0.81 using NR technique.	202
4.43	Optimisation of output voltage waveform of a thirteen-level modified CHB-MLIs with MI=0. 81 using NR technique.	203
4.44	The harmonic spectrum of output voltage waveform of modified CHB-MLIs with MI=0. 81 which optimised switching angle by NR technique.	204
4.45	Switching pattern of a thirteen-level modified CHB-MLIs for cell one comprising S1, S2, S3, S4, and S5 switches with MI=0.81 using PSO technique.	205
4.46	Switching pattern of a thirteen-level modified CHB-MLIs for cell two comprising S6, S7, S8, S9, and S10 switches with MI=0.81 using PSO technique.	205