EFFECT OF PAD ROUGHNESS ON SHEAR STRENGTH OF THIN SMALL LEADLESS PACKAGE

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MASTER OF SCIENCE IN MANUFACTURING ENGINEERING

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Faculty of Manufacturing Engineering

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ONG CHENG GUAN

A thesis submitted
in fulfillment of the requirements for the degree of Master of Science
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DECLARATION

I declare that this thesis entitled "Effect of Pad Roughness on Leadless Package's Shear Strength" is the result of my own research except as cited in the references. The thesis has not been accepted for any degree and is not concurrently submitted in candidature of any other master degree.

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APPROVAL

I hereby declare that I have read this thesis and in my opinion this thesis is sufficient in terms of scope and quality for the award of Master of Science in Manufacturing Engineering.

Signature :………………...

Supervisor Name :……………………….....................................

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DEDICATION

This thesis dedicated to my family and friends.

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ABSTRACT

Thin Small Leadless Packages (TSLP) have been manufactured to cater the current industry demand for a smaller electronic apparatus with a higher electrical performance. Previous studies showed the solder joint strength of leadless package with the printed circuit board (PCB) using Ni-P/Sn-0.5 Ag solder were influenced by soldering and reflow parameters. Nevertheless, scattered studies have been reported on the effect of surface roughness (R_a) of leadless package on its solder joint strength. The current study investigated effect of R_a of TSLP on the solder joint strength between the TSLP and PCB. In the current study, R_a of package's contact pad were varied using different Cu alloy leadframe materials (i.e. C194 and EFTECH-64) and etching process parameters (i.e. pH, specific Cu density and conveyor speed). This study also investigated the effect of Ni-P plating thickness and solder reflow conditions (i.e. temperature and duration) on the solder joint strength. Shear test was conducted on the soldered samples using Dage Series 4000 Bond Tester as per Infineon's Control Plan Specifications, with the shear strength data represented the solder strength values. Subsequently, the discussion of solder strength results were supported by the failure mode results of the shear test samples, generated by scanning electron microscopy (SEM, JOEL JSM-6360A) images and energy dispersive X-ray (EDX, JOEL JSM-6360A) analysis. An increase of Ni-P thickness on the etched samples reduced their R_a, thus resulted in a higher solder joint strength and smaller strength variation. Porous solder region in the soldered samples contributed to Mode 1 failure (i.e. fracture at solder region), which were exhibited by more than 80% of shear test samples. Only small percentages of shear samples showed Mode 2 (i.e. fracture at IMC and Ni-P layer interface) and Mode 3 (i.e. fracture at Ni-P and Ni bump interface). The percentage of Mode 2 and 3 failures were lower (i.e. composed of less than 5% of shear test samples) in low R_a samples. This could be explained by the improved solder wettability and strengthening of the IMC layer on the low R_a Ni-P plated samples.

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ABSTRAK

Thin Small Leadless Packages (TSLP) telah dihasilkan untuk memenuhi permintaan industri semasa bagi peralatan elektronik yang lebih kecil dengan prestasi elektrik yang lebih tinggi. Kajian terdahulu menunjukkan kekuatan gabungan pateri dengan papan litar bercetak (PCB) menggunakan pateri Ni-P/Sn-0.5 Ag dipengaruhi oleh parameter pematerian dan reflow. Walau bagaimanapun, kajian bertaburan telah dilaporkan mengenai kesan kekasaran permukaan (R_a) Leadless Packages pada kekuatan sendi soldernya. Kajian semasa menyiasat kesan R_a TSLP pada kekuatan sendi solder antara TSLP dan PCB. Dalam kajian semasa, pad sentuh pek pakej berbeza-beza menggunakan bahan api utama aloi Cu (contohnya C194 dan EFTECH-64) dan parameter proses etsa (iaitu pH, kepadatan Cu tertentu dan kelajuan penghantar). Kajian ini juga menyiasat kesan ketebalan plating Ni-P dan keadaan reflow solder (iaitu suhu dan durasi) pada kekuatan sendi pateri. Ujian shear dilakukan pada sampel yang dipateri menggunakan Dage Series 4000 Bond Tester seperti Spesifikasi Rancangan Kawalan Infineon, dengan data kekuatan ricih mewakili nilai kekuatan solder. Selepas itu, perbincangan keputusan kekuatan solder disokong oleh keputusan mod kegagalan sampel ujian ricih, yang dihasilkan oleh pengimbasan mikroskop elektron (SEM, JOEL JSM-6360A) dan analisis sinaran sinaran-X (EDX, JOEL JSM-6360A) . Peningkatan ketebalan Ni-P pada sampel teruk dikurangkan R_a mereka, sehingga menghasilkan kekuatan bersama solder yang lebih tinggi dan variasi kekuatan yang lebih kecil. Wilayah pateri pori-pori dalam sampel yang dipateri menyumbang kepada kegagalan Mode 1 (iaitu fraktur di kawasan solder), yang dipamerkan oleh lebih daripada 80% sampel ujian ricih. Hanya peratusan kecil sampel ricih menunjukkan Mode 2 (iaitu fraktur pada IMC dan antara muka lapisan Ni-P) dan Mode 3 (iaitu fraktur di antara Ni-P dan Ni bump). Peratusan mode 2 dan 3 kegagalan adalah lebih rendah (iaitu terdiri daripada kurang daripada 5% sampel ujian ricih) dalam sampel R_a rendah. Ini dapat dijelaskan dengan kelembapan pateri yang lebih baik dan pengukuhan lapisan IMC pada sampel plated R_a Ni-P rendah.

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LIST OF SYMBOLS

Symbol		Description
m	-	Meter
wt%	-	Percentage by weight
HRC	-	Rockwell Hardness
µm	-	Micrometer
C	-	Celsius
nm	-	Nanometer
m/min	-	Meter per Minute
g/cm^3	-	Gram per centimeter cube
g/L	-	Gram per Liter
vol%	-	Volume fracture
gmf	-	Gram meter force
kV	-	Accelerating Voltage

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CHAPTER 1

INTRODUCTION

1.1 Background

Semiconductor has been one of the rapid growing manufacturing industries. Year after year, main improvement to meet customers' demand is to shrink package dimension, pad size and pitches towards nano technologies. Therefore, the challenges for interconnect and assembly technology, which interface between semiconductor chip and external world, have steadily increased. Various Infineon Technologies' components are packed in advanced Quad Flat No-lead packages (QFN) for new application that emphasize size and weight reduction, good thermal and electrical properties as well. These platforms offer a versatility which allows either a single or multiple semiconductor devices to be connected together within a leadless package (Goh et al., 2014; Mario, 2006).

The company currently manufactures QFN-type Thin Small Leadless Packages (TSLP). Assembly process of TSLP (illustrated in Figure 1.1) is started with Ni bump on copper (Cu) alloy carrier. Later, the silicon chip is directly attached on Ni bump via eutectic, glue, or flip chip bonding process. If wire bonds are employed, it will bond to the remaining contact pads. Next, the chip and interconnect structures are encapsulated with halogen-free mold compound before the Cu alloy carrier is completely etched away. The remaining exposed nickel bumps are surface treated with electroless nickel immersion gold

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(ENIG) for assembly purposes. Finally, the packages are singulated and undergone electrical testing (Goh et al., 2014; Mario, 2006).

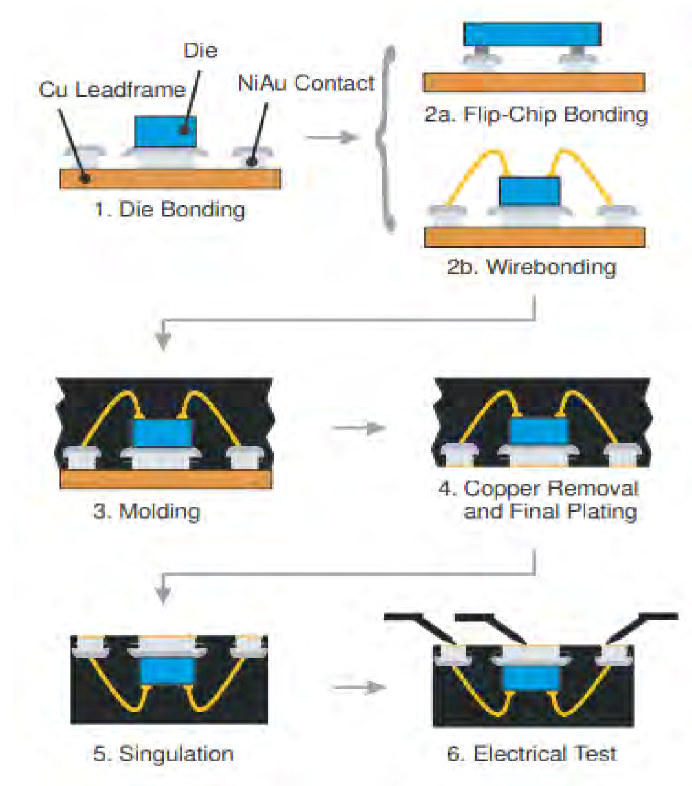

Figure 1.1: Conventional TSLP assembly process (Mario, 2006)

Electroless Nickel, EN is the first step of a two-step Electroless Nickel Immersion Gold (ENIG), i.e. surface finishing plating process for second level interconnection of TSLP packages. The ENIG has been extensively employed to protect copper circuit due to its excellent mechanical, electrical, corrosion and wear resistance properties (Tian et al., 2013; Kuo et al., 2006). EN process is an autocatalytic reduction reaction, where reducing agents are oxidized and Ni^{2+} ions are deposited onto the substrate surface. There are varieties of reduction agents involved in the EN plating and each reduction agent provides a special application need. According to Taheri (2003), the EN process is initiated on the

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substrate in three-dimension (3-D) growth process, and its deposition rate depends on diffusion of chemicals to the deposited surface and by-product (i.e. Hydrogen).

In semiconductor manufacturing, more than 90 % of the QFN packages use leadframe carrier as the main interconnection (Goh et al., 2014). In TSLP packages, EFECTH-64 Cu alloy carrier had been used as reliable interconnects between internal semiconductor chip and Ni bumps (as shows in Figure 1.1). EFTECH-64 Cu alloy carriers were used since introduction of innovation TSLP packages (Goh et al., 2014). Surface roughness, R_a set target during manufacturing TSLP packages were defined as 0.11 μm (since started manufacturing of TSLP). However, cost down of leadframe in semiconductor manufacturing process from EFTEH-64 to C194 Cu alloy shows inconsistence R_a during manufacturing of TSLP packages on existing process parameter (i.e. Figure 1.1, Step 4 Cu removal and final plating). Therefore, control of R_a of C194 Cu alloy carrier is required due to its low cost and at the same time to meets the robust packages requirement.

1.2 Problem Statements

Alkaline etching process is used to remove and expose Ni bump's surface on TSLP (Figure 1.2). Alkaline etchant (Cupric chloride, $CuCl_3$) from MacDermid Singapore PTE LTD was selected to etch Cu substrate (Figure 1.2, Step 2). The alkaline etchants have the capability of being chemically regenerated after reacting with targeted sites, thus ensuring a steady-state operation. However, the etching process (Figure 1.2, Step 2) produces rough bump surface. Previous studies argued that the substrate roughness had a profound impact on subsequent EN deposition of TSLP's bump (Figure 1.2, Step 3) in terms of their hardness, wear and corrosion properties (Sahoo and Das, 2011). Nevertheless, the effects

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of roughness on the shear strength of solder joint EN plated package have not been reported. It is believed that the substrate's rough surface affects mechanical strength of EN coating because of different number of activation sites (Sahoo and Das, 2011). Low roughness can be achieved through optimizing etching parameters, such as etching speed, pH and Cu specific density for different Cu alloy carriers (i.e. EFTECH 64 and C194 grades).

Previous studies have shown that solder or Ni-P interface undergoes phase transformation during reflow and thermal ageing cycle. At extending ageing time up to 1000 hours, mechnanical strength of Sn-Ag/Ni-P solder joint deteriorates due to the growth of intermetallic compound (IMC), such as Ni_3Sn_4 (He et al., 2005; Kumar and Chen 2006). This phenomenon somehow affects failure mode of the solder joint in mechanical shear testing. However, the understanding of IMC formation on the solder joint and the influence of Ni-P surface roughness and the corresponding bump on the shear strength are still lacking.

This work aims to assess shear strength of the Sn-Ag solder/Ni-P by varying surface roughness of TSLP's bumps. These findings should indirectly benefit Infineon in reducing manufacturing cost and further improve quality and product yield of its TSLP production.

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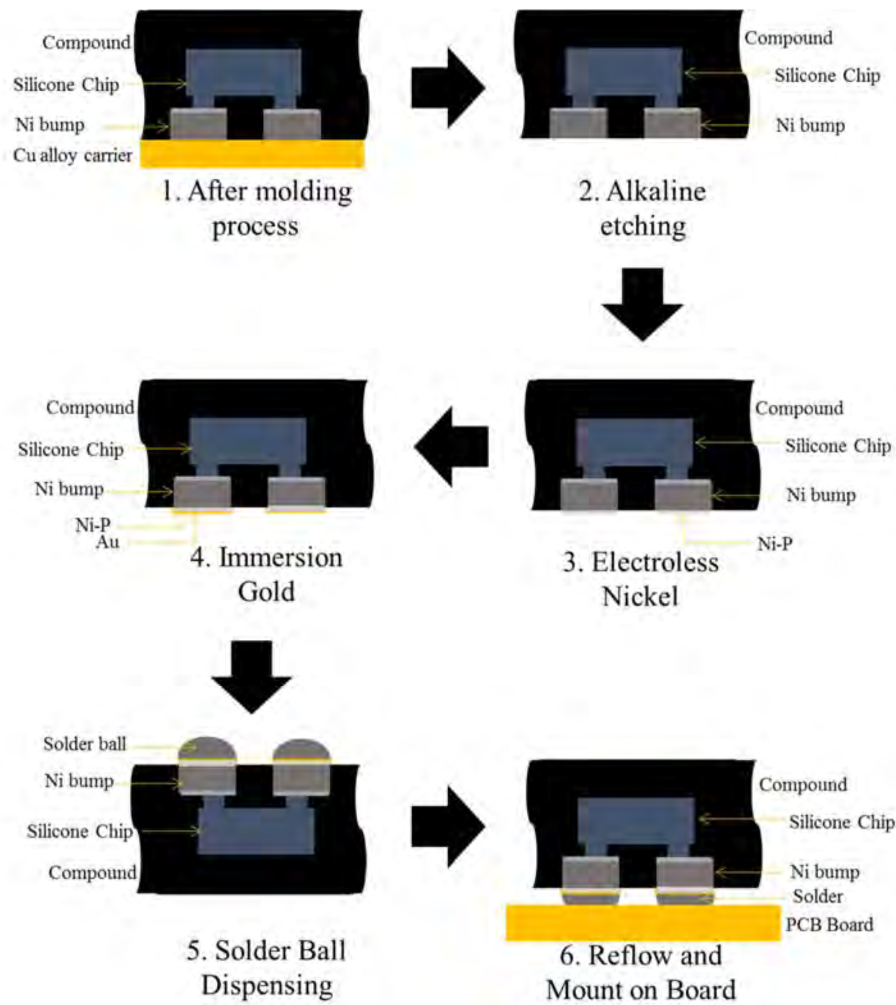

Figure 1.2: Infineon's finishing process flow of TSLP packages

1.3 The Research Objectives

i. To investigate the effects of cupric chloride etching parameters on surface roughness (R_a) of TSLP's Ni bump on C194 and EFTECH-64 Cu alloy carriers.

ii. To analyse the effect of surface roughness of Cu alloy carriers on the bonding capacity of Ni-bump in terms of determining interfacial shear strength.

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1.4 The Scope of Research

Current research focuses on the improvement of surface finishing process (i.e. Step 2 to 3 of Figure 1.2) of secondary interconnect of TSLP package. The surface roughness of Ni bump of TSLP was investigated in terms of four etching process factors: etching speed, etchant's pH and Cu specific density and Cu alloy carrier grade. Surface roughnesses of 0.11 µm from EFTECH-64 Cu alloy carrier were selected as benchmark target (studies done by Infineon). Next, product undergoes reflow process after solder ball dispensing (i.e. Step 5 and 6 of Figure 1.2).

The TSLP's solder joint shear strength correlations with Ni-P thickness and the bump's surface roughnesses were assessed aiming to understand statistical distribution of the measured data. Cross sectional microstructure and chemical element analysis on the fracture surface of post shear-shear test samples were investigated in order to understand the relationship of the fracture mode with shear strength.

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CHAPTER 2

LITERATURE REVIEW

Chapter 2 outlines the manufacturing process of TSLP process flow, namely the Cu etching and ENIG processes. Section 2.1 explains the fundamental of TSLP process flow. Then, Sections 2.2 and 2.3 describe the fundamental and mechanism of Cu etching and EN processes, respectively. Next, Section 2.4 gives a review and understanding of EN deposition influence at different surface roughness. Finally, shear strength mechanical studies done in Section 2.5.

2.1 Semiconductor Packaging: TSLP

TSLP is a novel and innovative leadless package concept from Infineon Technologies. This package concept enables operation at high frequency and mm-wave regions. The package has several advantages, such as small dimensions (Figure 2.1), shorter interconnects, excellent radio frequency (RF) capabilities and good thermal properties (Wojnowski et al., 2008; Ng et al., 2015). The following terminologies used to investigate the Ni bump, such as foot print, contact pad, interconnect and pin count.

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