



Faculty of Manufacturing Engineering

**REMOTE GLOBAL ALIGNMENT ERROR FOR CYCLE TIME
IMPROVEMENT OF PAD INDUCTOR LAYER**

Saandilian A/L Devadas

Doctor of Engineering

2018

**REMOTE GLOBAL ALIGNMENT ERROR FOR CYCLE TIME IMPROVEMENT
OF PAD INDUCTOR LAYER**

SAANDILIAN A/L DEVADAS

**A thesis submitted
in fulfillment of the requirements of Doctor of Engineering**

Faculty of Manufacturing Engineering

UNIVERSITI TEKNIKAL MALAYSIA MELAKA

2018


DECLARATION

I declare that this thesis entitled “Remote Global Alignment Error for Cycle Time Improvement of Pad Inductor Layer” is the result of my own research except as cited in the references. The thesis has not been accepted for any degree and is not concurrently submitted in candidature of any other degree.

Signature : 
Name : SAANDILIAN A/L DEVADAS
Date : 10 OCTOBER 2018

APPROVAL

I hereby declare that I have read this thesis and in my opinion, this thesis is sufficient in terms of scope and quality for the award of Engineering Doctorate.

Signature : 

Supervisor Name : ASSOC. PROF. DR. SHAJAHAN BIN MAIDIN

Date : 10/10/2018.

ABSTRACT

Lithography is the key process which transfers the pattern from mask (reticle) to wafer; and pad inductor layer is the last layer in photo masking. The cycle time for pad inductor layer has increased in Silterra Malaysia Sdn. Bhd., by 32% per month due to Global Alignment (GA) error. Meanwhile, engineering team taking long duration during troubleshooting of the lot at exposure and developing step. This is due to tool time constrain which requires a Process Engineer to perform this activity manually. Most of the lots undergo rework step which results in cost of per wafer to increase. The goal of this project is to reduce the cycle time for pad inductor layers by introducing "Remote Global Alignment Error" (RGAE) framework; in which this new framework will results in alternative flow. The methodology was designed if encountering global alignment error. During the process, the lot will automatically load in by "Remote Global Alignment Error" (RGAE) framework by selecting the rejected wafers going for exposure and developing process. This has eventually save more time for split wafers which will usually send for rework or run the lot manually. Few DOE test was conducted to compare the cycle time performance of the (RGAE) framework with the Manual Global Alignment (MGA) method. Furthermore, there main photolithography process (coat, exposure, develop), reject wafers and rework rate cycle time performance was also tested. In total, five test lots and five production lots selected to run the DOE test. All the cycle time data which was collected through this DOE test analyzed using Minitab 17 statistical software. The analyzed report shows that the cycle time for RGAE method could be achieved within 2 hours. This success could be achieved by allowing the rejected wafers to run automatically by using the alternative flow until the wafers successfully exposed. Furthermore, with the (RGAE) framework, the production can save time for split, rework, remask and merge all the wafers. The experimental result shows that (RGAE) framework able to provide fast solution by achieving 97% reduction of cycle time for pad inductor layer comparing to Manual Global Alignment (MGA) method.

ABSTRAK

Litografi adalah suatu proses utama yang memindahkan corak daripada reticle kepada lapisan wafer dan pad induktor merupakan lapisan terakhir di dalam hirarki Litografi. Kitaran masa untuk lapisan pad induktor menunjukkan peningkatan kerana mempunyai 32% daripada ralat penjajaran global (GA) sebulan di Silterra Malaysia Sdn Bhd. Dalam masa yang sama, masa kejuruteraan akan diambil lama untuk menyelesaikan masalah lot untuk menjalankan proses “expose” dan “develop”. Ini adalah kerana, masa penggunaan mesin terhad untuk digunakan oleh Jurutera Proses di dalam keadaan mod manual. Kebanyakan lot dihantar untuk kerja semula menyebabkan kos proses “wafer” meningkat. Matlamat projek ini adalah untuk mengurangkan masa kitaran untuk lapisan pad induktor dengan memperkenalkan rangka kerja yang dikenali sebagai “Remote Global Alignment Error” (RGAE) dengan aliran alternatif. Untuk itu, sebuah metodologi direka jika menghadapi ralat penjajaran global (GA). Semasa proses itu, lot akan secara automatik dimuatkan dengan menggunakan rangka kerja “Remote Global Alignment Error” (RGAE) dengan memilih “wafer” yang ditolak untuk proses “expose” dan “develop”. Melalui rangka kerja ini, membolehkan menjimat lebih banyak masa untuk memisahkan “wafer” yang biasanya akan dihantar untuk kerja semula atau menjalankan lot secara mod manual. Beberapa ujian DOE dijalankan untuk membandingkan prestasi masa kitaran rangka kerja (RGAE) dengan kaedah “Manual Global Alignment” (MGA). Selain itu, tiga proses photolithography utama (“coat”, “exposure”, “develop”), “wafer” yang ditolak dan kadar kerja semula untuk prestasi masa kitaran juga diuji. Secara keseluruhannya, lima lot daripada ujian dan lima lot daripada produk pengeluaran dipilih untuk menjalankan ujian DOE. Semua data masa kitaran yang dikumpulkan melalui ujian DOE ini dianalisis dengan menggunakan perisian statistik Minitab 17. Laporan analisis menunjukkan bahawa masa kitaran dengan untuk rangka kerja (RGAE) dapat dicapai dalam masa dua jam. Kejayaan ini dapat dicapai dengan membenarkan “wafer” yang ditolak untuk dijalankan secara automatik dengan menggunakan aliran alternatif sehingga “wafer” tersebut berjaya “expose”. Selain itu, dengan menggunakan rangka kerja (RGAE), syarikat dapat menjimatkan masa untuk memisahkan “wafers”, kerja semula, mengulang semula dan menggabungkan semua “wafer”. Hasil eksperimen menunjukkan bahawa rangka kerja (RGAE) dapat mampu memberikan penyelesaian yang cepat dengan mencapai 97% pengurangan masa kitaran untuk lapisan pada pad induktor yang membandingkan dengan kaedah “Manual Global Alignment” (MGA).

ACKNOWLEDGEMENTS

First and foremost, I would like to take this opportunity to express my sincere acknowledgment to my supervisor Assoc. Prof. Dr. Shajahan Bin Maidin from the Faculty of Manufacturing Engineering Universiti Teknikal Malaysia Melaka (UTeM) for his essential supervision, support and encouragement towards the completion of this thesis.

I would also like to express my greatest gratitude to my industrial supervisor Mr. Tritham Wara from Photolithography, Silterra Malaysia Sdn Bhd for his advice and suggestions in the evaluation of new Remote Global Alignment Error (RGAE) method. I gratefully acknowledge the funding sources that made my research work possible. I was funded by the Malaysian government through a MyBrain15 program for the financial support throughout this project.

Special thanks to Silterra Malaysia Sdn Bhd that provide a place for me to use tools for a run all the DOE and simulation to get the positive results and successfully complete my research.

Lastly, I would like to thank my family for all their love and encouragement. For my parents who raised me with a love of science and supported me in all my pursuits. Besides that, special thanks to most of all for my loving, supportive, encouraging, and patient wife Kavitha whose faithful support during the final stages of this research is so appreciated.

TABLE OF CONTENTS

PAGE

DECLARATION	
APPROVAL	
ABSTRACT	i
ABSTRAK	ii
ACKNOWLEDGEMENTS	iii
TABLE OF CONTENTS	iv
LIST OF TABLES	viii
LIST OF FIGURES	ix
LIST OF APPENDICES	xiv
LIST OF SYMBOLS	xv
LIST OF PUBLICATIONS	xvi
CHAPTER	
1. INTRODUCTION	1
1.1 Introduction	1
1.2 Motivation	8
1.3 Problem Statement	9
1.4 Research Objective	11
1.5 Research Contribution	11
1.6 Research Scope	11
1.7 Thesis Organisation	12
2. LITERATURE REVIEW	13
2.1 Introduction	13
2.2 Alignment of Three Dimensional Integration	15
2.3 Wafer-to-Wafer Alignment	17
2.4 Discussion of Previous Photolithography Alignment Methods	18
2.4.1 Transparent Substrate Method	19
2.4.2 Wafer Through Holes Method	20
2.4.3 Infrared Transmission Microscopy Method	21
2.4.4 Backside Alignment with Digitalized Image Method	22
2.4.5 Smart View Alignment Method	23
2.4.6 3D Align Method	25
2.5 Impact of Alignment Process for Via Density	26
2.6 Alignment Signal Behaviour Impacted on Contact and Metal Alignment Mark	28
2.7 Non-Zero Alignment Mark Overlay Penalty	34
2.8 Managing Non-Zero Alignment Overlay Penalty in Production	37
2.9 Define and Assign Alignment Strategies	40
2.9.1 Versatile Scribe-lane Primary Mark (VSPM)	42
2.9.2 Short Scribe-lane Primary Mark (SSPM)	43
2.10 Actual Marks Used for Alignment Mark	44
2.10.1 Alignment Mark of Color Dynamic	45
2.10.2 Color Dynamic and the Effect of Mark Rejection	48
2.10.3 Alignment Mark of Color Dynamic and the Effect on the Overlay	50

2.10.4	Smooth Color Dynamic Alignment Method for Twinscan	51
2.10.5	Improved performance with smooth color-dynamic	53
2.11	Misalignment Category	57
2.11.1	Thermal Induced Misalignment	58
2.11.2	Wafer Stress and Nonlinear Wafer Distortion	60
2.12	Rejected Wafers	60
2.13	What is Cycle Time?	63
2.14	Throughput (WPH)	65
2.15	Planning and Scheduling in Semiconductor Manufacturing	67
2.15.1	Linear and Non-Linear Programming Models	68
2.15.2	Simulation Models	69
2.16	Dispatching Rules	70
2.16.1	Dispatching Rule in Photolithography	73
2.16.2	Dispatching Rule in Parallel Machine with Sequence Dependent Setup Time	75
2.17	Capacity Modeling	76
2.17.1	Availability	77
2.17.2	Downtime	77
2.17.3	Manufacturing Efficiency	77
2.17.4	Operational Utilization	77
2.18	Aggregate Modeling Using Effective Process Times	78
2.19	Demonstrating Unscheduled Downs	81
2.20	WIP Reliance	83
2.21	Traceability	85
2.22	A Systematic Cycle Time Reduction Procedure for Enhancing the Competitiveness and Sustainability of a Semiconductor Manufacturer	86
2.23	Recognize the Controllable Elements That Effective Activity of the Cycle Time	91
2.24	Appropriate the Connection between the Controllable Elements and the Activities of Cycle Time	92
2.24.1	Design the Actions to Reduce the Activities of the Cycle Time	93
2.25	Classical Queueing Models for Toolsets	95
2.26	Silterra Manual Global Alignment (MGA) Method	98
2.27	Manual Global Alignment (MGA) Method Data Collection	99
2.27.1	Multiple Correlation Coefficients (MCC)	100
2.27.2	Delta Shift (8.0 to 8.8 shift)	101
2.27.3	Worst Wafer Quality (WWQ)	102
2.27.4	Mark Residuals	103
2.28	Summary	103
3.	METHODOLOGY	104
3.1	Introduction	104
3.2	Research Methodology	106
3.2.1	Phase 1: Modify Algorithm for Carrier Update	107
3.2.2	Phase 2: Develop New Coating Process Recipe	107
3.2.3	Phase 3: Develop New Scanner Process Recipe	108
3.2.4	Phase 4: Develop New Developing Process Recipe	109
3.2.5	Phase 5: Develop New Algorithm for Looping Process	110

3.3	Alignment for Manual Global Alignment (MGA) Method	111
3.4	Issues on Manual Global Alignment (MGA) Method	112
3.5	Manually Expose and Develop the Reject Wafers	113
3.6	Rework the Reject Wafers	114
3.7	Summary	115
4.	REMOTE GLOBAL ALIGNMENT ERROR (RGAE) FRAMEWORK	116
4.1	Introduction	116
4.2	Proposal Framework - Remote Global Alignment Error (RGAE)	117
4.3	Remote Global Alignment Error (RGAE) Framework's Features	118
4.4	Implementation	120
4.5	First Run	120
4.5.1	Lot with Swipe Badge	120
4.5.2	Pod Clamping	121
4.5.3	Recipe Control System (RCS)	122
4.5.4	Lot Track In	123
4.5.5	Creating Job at Tool	124
4.5.6	Job Processing Start	124
4.5.7	Job Processing Finish	125
4.5.8	Unloading Cassette	125
4.5.9	Pod Unclamped	126
4.6	Restage Lot to Run First GA Error Recipe (Auto Track In)	126
4.6.1	First Restage Lot – Clamping Pod	126
4.6.2	First Restage Lot – Recipe Control System (RCS)	127
4.6.3	First Restage Lot – Lot Track In	127
4.6.4	First Restage Lot – Create Recipe at Tool	128
4.6.5	First Restage Lot – Job Processing Start	129
4.6.6	First Restage Lot – Job Processing Finish	129
4.6.7	First Restage Lot – Unloading Cassette	130
4.6.8	First Restage Lot – Pod Unclamped	130
4.7	Forth Restage Lot	131
4.8	Summary	131
5.	RESULT AND DISCUSSION	132
5.1	Introduction	132
5.2	Performance of Manual Global Alignment (MGA) Method	133
5.2.1	Manual Global Alignment (MGA) Method Overall Process Performance	133
5.2.2	Reject Wafers from Manual Global Alignment (MGA) Method	135
5.2.3	Rework Rate from Manual Global Alignment (MGA) Method	136
5.2.4	Cycle Time Impact Base on Manual Global Alignment (MGA) Method	137
5.3	Performance of (RGAE) Framework	138
5.3.1	(RGAE) Framework for Overall Process Performance	138
5.3.2	Reject Wafers from (RGAE) Framework	140
5.3.3	Cycle Time Impact Base on (RGAE) Framework	141
5.4	Descriptive Statistics Test between (MGA) Method and (RGAE) Framework	142

5.5	Two-Sample T-Test and ANOVA Test between (MGA) Method and (RGAE) Framework	146
5.5.1	Two-Sample T-Test and Confidence Intervals for Cycle Time between (MGA) Method and (RGAE) Framework	147
5.5.2	Comparing Variance Test for CT between (MGA) and (RGAE) Framework	149
5.5.3	Comparing ANOVA Test for CT between (MGA) and (RGAE) Framework	152
5.6	Comparing ANOVA Test for Cycle Time between Processes (Coat, Exposure, Develop) in the (MGA) Method and the (RGAE) Framework	156
5.7	Cycle Time Comparison between (MGA) Method and (RGAE) Framework Using Production Lot	163
5.8	Summary	166
6.	CONCLUSION AND RECOMMENDATIONS FOR FUTURE RESEARCH	167
6.1	Introduction	167
6.2	Comparison between (MGA) Method vs (RGAE) Framework	170
6.3	Recommendations for Future Research	172
	REFERENCES	174
	APPENDICES	197

LIST OF TABLES

TABLE	TITLE	PAGE
2.1	The Group of Variant ID's Available for Each Basic Mark Type	41
2.2	Reject Wafers Due to Alignment Marks at ASML Scanner	61
2.3	Throughput Comparison on a Pad Inductor Layer	66
2.4	Data Collection by C18 Technologies Device	99
2.5	Data Collection by Percentage	100
5.1	Overall Process Performance for C18 Technologies Pad Inductor Layer	133
5.2	Data for Reject Wafers Using (MGA) Method	135
5.3	Data for Rework Rate Using (MGA) Method	137
5.4	Data for Cycle Time Rate Using (MGA) Method	128
5.5	Overall Process Performance for C18 Technologies Pad Inductor Layer	138
5.6	Data for Reject Wafers Using (RGAE) Framework	140
5.7	Data for Cycle Time Rate Using (RGAE) Framework	141
5.8	Cycle Time Comparison between the (MGA) Method and the (RGAE) Framework for Pad Inductor Layer	163
6.1	Difference between (MGA) Method and (RGAE) Framework	172

LIST OF FIGURES

FIGURE	TITLE	PAGE
1.1	Semiconductor Wafer Process Flow	2
1.2	Photolithography Process Flow	3
1.3	Photolithography Layer Sequence	4
2.1	Schematic Two Major 3-D Technology Platforms. Via-Last (top) and Via-First (bottom)	16
2.2	Optical Microscopy for Transparent Substrates Method	19
2.3	Wafer Through Holes Method by Using Optical Microscopy	20
2.4	IR Transmission Microscopy for IR Transparent Substrates	21
2.5	Optical Microscopy Using Front-to-Backside Alignment Marks	22
2.6	Smart View Alignment Method	24
2.7	3DAlign Method	25
2.8	Design Rule for Via of the Bond Pad	27
2.9	Cross Section View for Contact Alignment Mark	32
2.10	Cross Section View for Metal Alignment Mark	33
2.11	The VSPM (and SSPM) in Comparison with a Standard SPM	42
2.12	The Alignment Results from a Wafer Batch That Has Gone Through a CMP Process	49
2.13	The Overlay Results for an STI Process, Using Color 5 th Order Red Recipe	50
2.14	The Overlay Results for STI Process, Using 5th Order Color Dynamic Recipe	51

2.15	The Swing Curve Plots of WQ versus Mark Depth for the Red and Green Alignment Signals of the ATHENA Alignment System	52
2.16	The Shift in the Aligned Position for the Following Types Of Alignment Recipe: Smooth Color Dynamic (With Smooth Factor = 10), Color Dynamic, Single-Color Red, and Single-Color Green	54
2.17	Schematic of Various Misalignments	57
2.18	Thermal Expansion Errors Due to Temperature Differentials	59
2.19	Expansion Misalignments of the X and Y Directions	60
2.20	Calculation of Lot Cycle Time and the Throughput	63
2.21	WPH Calculation	65
2.22	WIP Dependency of EPTs	78
2.23	Combining EPT Observations with Status Data	82
2.24	An Aggregate Model with Explicitly Modeled Machine Failures	83
2.25	Utilization Dependency of EPTs	84
2.26	Overtaking Makes It Difficult To Match EPT Observations To Specific Lots	85
2.27	Silterra Manual Global Alignment (MGA) Alignment Method	99
2.28	Test Result for MCC	101
2.29	Test Result for Delta Shift	102
2.30	Test Result for Wafer Quality	102
3.1	Alignment Tree	105
3.2	Research Methodology	106
3.3	Global (Search) & Fine (EGA) Alignment	111
3.4	Difference between Course and Fine Wafer Alignment Marks	112
4.1	Proposal (RGAE) Framework	117
4.2	Wait for Swipe Badge	121

4.3	Verify User	121
4.4	Clamping Pod	122
4.5	Pod Clamped	122
4.6	Check RCS	122
4.7	Verify Track Recipe at Tool	122
4.8	Reticle Checking	123
4.9	Reticle and Layer Checking	123
4.10	Dispatch Lot for TrackIn	123
4.11	Loading Cassette	123
4.12	Check Slot Map Pass	123
4.13	Creating Track Job	124
4.14	Creating Jobfile in Scanner	124
4.15	Dispatch Lot for Track In	124
4.16	Loading Cassette	124
4.17	Dispatch Lot for Track In	125
4.18	Loading Cassette	125
4.19	Unloading Cassette	125
4.20	Lot on Hold	125
4.21	Pod Unclamped	126
4.22	Restaging Process	126
4.23	Clamping Pod	126
4.24	Verifying Track Recipe	127
4.25	Verifying Scanner Recipe	127
4.26	Reticle and Layer Checking	127
4.27	RMS Checking Successful	127

4.28	Dispatching Lot for Track In	127
4.29	Loading Cassette	127
4.30	Check Slot Map	128
4.31	Creating Track Job	128
4.32	Creating Scanner Job file	128
4.33	Job Processing Start	129
4.34	Exposure Job Start	129
4.35	Exposure Completed	129
4.36	Exposure Completed	129
4.37	Unloading Cassette	130
4.38	Incomplete Lot Process	130
4.39	Pod Unclamp	130
4.40	Wait for Removal	131
5.1	Total Exposure Process Time Using (MGA) Method	134
5.2	Reject Wafers by Percentage Using (MGA) Method	135
5.3	Rework Rate Using (MGA) Method	136
5.4	Cycle Time Rate Using (MGA) Method	137
5.5	Total Exposure Process Time Using (RGAE) Framework	139
5.6	Reject Wafers by Percentage Using (RGAE) Framework	140
5.7	Cycle Time Rate Using (RGAE) Framework	141
5.8	Descriptive Statistics Cycle Time between (MGA) and (RGAE) Framework	142
5.9	DS Boxplot	145
5.10	DS Individual Value	145
5.11	DS Summary (MGA) Method	145
5.12	DS Summary (RGAE) Framework	145

5.13	Two-Sample T-Test and Confidence Interval for Cycle Time	148
5.14	Boxplot Base on Two-Sample T-Test and Confidence Interval	148
5.15	F-Test	151
5.16	Bonett and Levene Test	151
5.17	F-Test Graph	151
5.18	Bonett and Levene Test Graph	151
5.19	One Way ANOVA Test for CT between (MGA) Method and (RGAE) Framework	153
5.20	One Way ANOVA Test for CT between (MGA) Method and (RGAE) Framework	154
5.21	Boxplot for Cycle Time	155
5.22	Interval Plot for Cycle Time	155
5.23	HSU Simultaneous Ninety Percentage of Confidence Interval	155
5.24	One Way ANOVA Test for Cycle Time between Coat, Exposure and Develop Process	157
5.25	Residual Plot for Cycle Time	158
5.26	Boxplot Test for Cycle Time between Coat, Exposure and Develop Process	159
5.27	Interval Plot Test for CT between Coat, Exposure and Develop Process	160
5.28	Tukey Plot Test for Cycle Time between Coat, Exposure and Develop Process	161
5.29	HSU is Plot Test for CT between Coat, Exposure and Develop Process	162
5.30	Cycle Time Comparison between (MGA) and (RGAE) Framework for Pad Inductor Layer	164
5.31	Cycle Time Reduction on the (RGAE) Framework Compared To (MGA) Method for Pad Inductor Layer	165

LIST OF APPENDICES

APPENDIX	TITLE	PAGE
A1	Process Details for Current Method - LOT A	197
A2	Process Details for Current Method - LOT B	198
A3	Process Details for Current Method - LOT C	199
A4	Process Details for Current Method - LOT D	200
A5	Process Details for Current Method - LOT E	201
B1	Process Details for RGAE Method - LOT A1	202
B2	Process Details for RGAE Method - LOT B1	203
B3	Process Details for RGAE Method - LOT C1	204
B4	Process Details for RGAE Method - LOT D1	205
B5	Process Details for RGAE Method - LOT E1	206
C1	Summary Process Details for Current Method	207
C2	Summary Process Details for RGAE Method	207

LIST OF SYMBOLS

μm	-	micrometer
L_{Pitch}	-	pitch
$L_{Overlap}$	-	minimum overlay
L_{Space}	-	distance
M_{Mean}	-	average
M_{Sdv}	-	standard deviation
$M_{Run-out}$	-	expansion
L	-	diameter

LIST OF PUBLICATIONS

Saandilian, D., Shajahan, M., Tritham, W., 2017. Remote Global Alignment Error for Cycle Time Improvement of Pad Inductor Layer. *In Journal of Advanced Manufacturing Technology (JAMT)*, 12(11).

Saandilian, D., Shajahan, M., Tritham, W., Nurul, H., Hong, L.K., 2016. Remote Global Alignment Error for Pad Inductor Layer to Improve Cycle Time. *In Proceedings of the 2016 International Conference on Industrial Engineering and Operations Management (IEOM)*, pp. 612.

CHAPTER 1

INTRODUCTION

1.1 Introduction

Semiconductor wafer fabrication is a procedure composed of many repeated sequential processes to produce complete electrical or photonic circuits. Examples include production of radio frequency (RF) amplifiers, LEDs, optical computer components and CPUs for computers.

Integrated Circuit (IC) is fabricating process for a various step sequence of chemical and photographic processes that performed on the wafer. A wafer or substrate fabricated on a thin slice of silicon is mainly used in most semiconductor chips companies. The various processes used to make an integrated circuit (IC) on the wafer are photolithography, resist removal, etching, layering, wafer cleaning and doping. Figure1.1 represents one cycle of the primary steps and their sequence.

On the other hand, May (2006) explained more details regarding layering techniques that used to grow thin layers of film on the wafer surface. Photolithography uses light to transfer a geometric pattern from a photomask to a light-sensitive photoresist on the substrate. The photoresist needs to be stripped away. Etching is the process of using strong acid to cut into the unprotected parts of a metal surface to create a design in the metal. Doping is the process of impurity atoms being used in order to define the electrical properties of this region. Cleaning is used to remove particulates and chemical impurities so contaminant-free surfaces can be obtained.

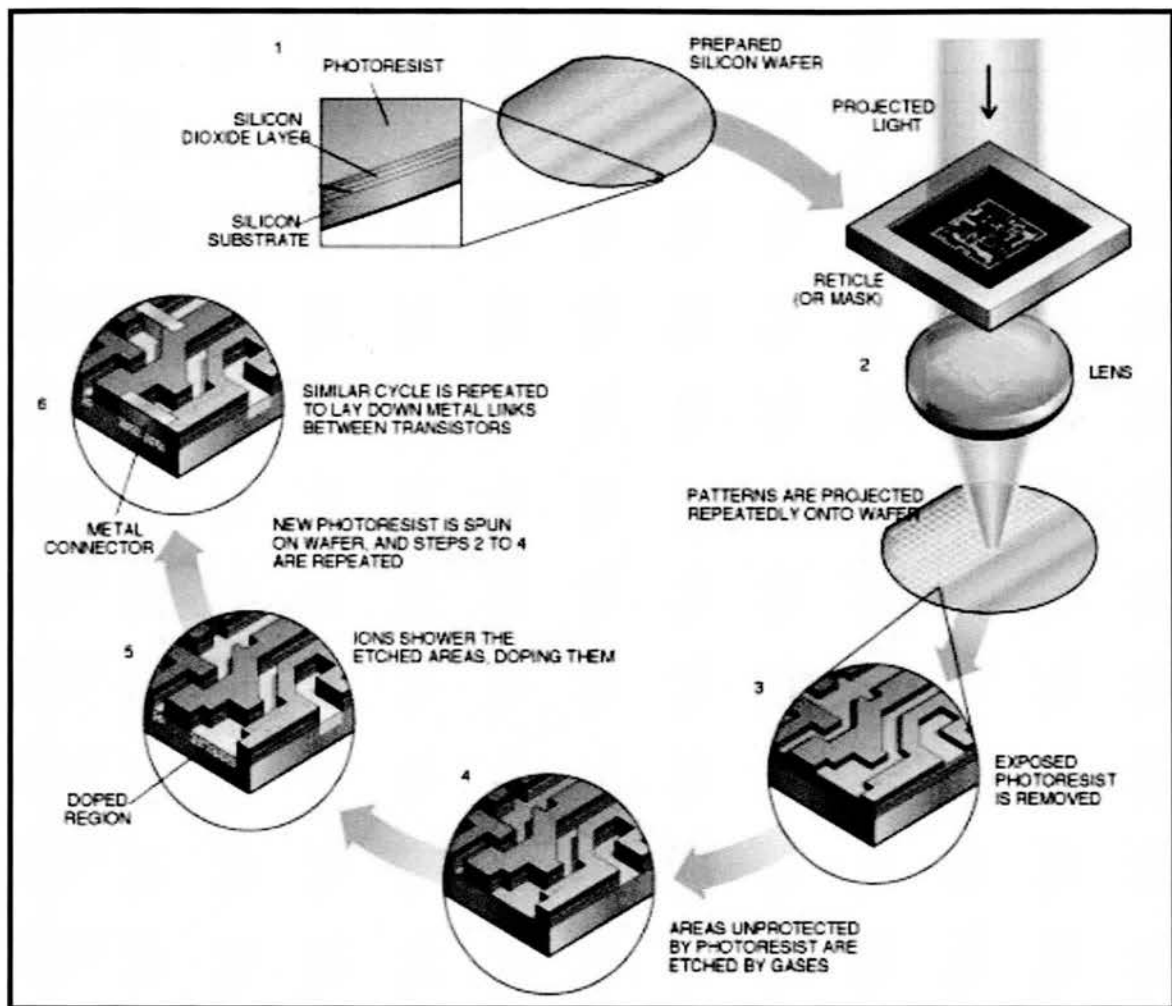


Figure 1.1: Semiconductor Wafer Process Flow (Spierings, 2013).

In the semiconductor wafer process, the photolithography process has the most expensive equipment and one of the bottleneck process compared to other wafer fabrication processes in the production line. Photolithography is the temporarily coat photoresist on wafer and transfers designed pattern to the photoresist. It is the core of the manufacturing process flow (Yen, 2012).

The goal of the photolithography process is to determine the high resolution, high photoresist sensitivity, precision alignment within 10 percentage of minimum feature size, precise process parameters control and low defect density (Lai, 2009).

The process sequence for photolithography is photoresist coating, alignment, exposure and photoresist developing the layer (Lucas, 1999). It requires high resolution, high sensitive, precise alignment and low defect density that contributes to high yield and good imaging. Figure 1.2 shows the photolithography process flow in wafer fabrication.

Figure 1.2: Photolithography Process Flow (Spierings, 2013).

The photolithography process flow is repeated for up to 30 times for one device (depending on technology and device). The repetition of this process normally requires different reticles (poly, contact, metal, via & pad inductor) which have different chrome patterns on it (Saandilian, 2016). However, some layers like some implant layers share the same reticle. Figure 1.3 shows that photolithography layer sequence flow. It starts from the first layer (island) until the last layer (pad inductor). The pad inductor or passivation layer is the last layer performed in photolithography to prevent physical damage (scratches) and as a barrier to mobile ion contaminants.

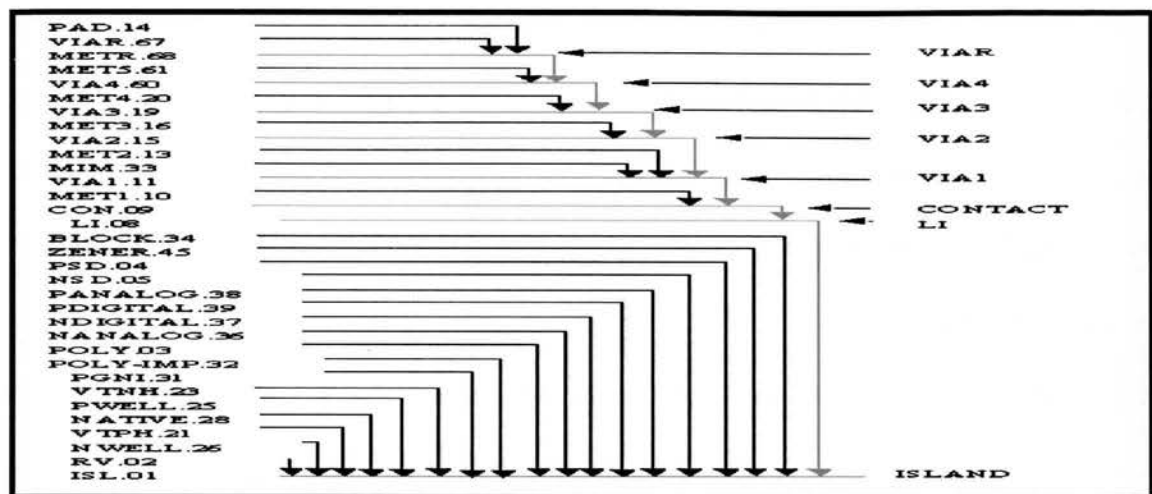


Figure 1.3: Photolithography Layer Sequence (Saandilian, 2016)

Alignment (overlay) is a key challenge process in photolithography since the minimum dimension of integrated circuits (ICs) has been shrinking (Zhang, 2013). Modern CMOS integrated circuits have almost 30 layers to be aligned perfectly to avoid misalignment. Alignment marks are placed on the wafer at the beginning of the process during the first level of photolithography. Furthermore, the good alignment mark can prevent misalignment that induces to reduce overall photolithography cycle time (Saandilian, 2016).

In wafer fabrication, reduction of cycle time is very important for all semiconductor process (Chen, 2013b). Cycle time consists of queuing time for reticle changes, tool downtime, engineering work, preventative maintenance, visual inspection time, production processing time and lot transportation time. The main objective of the cycle time is to have a shorter cycle time (Spierings, 2013).

One of a most important part of photolithography is a reduction of cycle time for pad inductor layer; since it is the last layer in photolithography (Saandilian, 2016). Manufacturing always gives high priority to pad inductor layer in determining not have any delay in the process.