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UNIVERSITI TEKNIKAL MALAYSIA MELAKA

Faculty of Manufacturing Engineering

REMOTE GLOBAL ALIGNMENT ERROR FOR CYCLE TIME IMPROVEMENT OF PAD INDUCTOR LAYER

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A thesis submitted
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2018

DECLARATION

I declare that this thesis entitled "Remote Global Alignment Error for Cycle Time Improvement of Pad Inductor Layer" is the result of my own research except as cited in the references. The thesis has not been accepted for any degree and is not concurrently submitted in candidature of any other degree.

Signature : ....

Name : SAANDILIAN A/L DEVADAS

Date : 10 OCTOBER 2018

APPROVAL

I hereby declare that I have read this thesis and in my opinion, this thesis is sufficient in terms of scope and quality for the award of Engineering Doctorate.

Signature : ....

Supervisor Name : ASSOC. PROF. DR. SHAJAHAN BIN MAIDIN

Date : 10/10/2018.

ABSTRACT

Lithography is the key process which transfers the pattern from mask (reticle) to wafer; and pad inductor layer is the last layer in photo masking. The cycle time for pad inductor layer has increased in Silterra Malaysia Sdn. Bhd., by 32% per month due to Global Alignment (GA) error. Meanwhile, engineering team taking long duration during troubleshooting of the lot at exposure and developing step. This is due to tool time constrain which requires a Process Engineer to perform this activity manually. Most of the lots undergo rework step which results in cost of per wafer to increase. The goal of this project is to reduce the cycle time for pad inductor layers by introducing "Remote Global Alignment Error" (RGAE) framework; in which this new framework will results in alternative flow. The methodology was designed if encountering global alignment error. During the process, the lot will automatically load in by "Remote Global Alignment Error" (RGAE) framework by selecting the rejected wafers going for exposure and developing process. This has eventually save more time for split wafers which will usually send for rework or run the lot manually. Few DOE test was conducted to compare the cycle time performance of the (RGAE) framework with the Manual Global Alignment (MGA) method. Furthermore, there main photolithography process (coat, exposure, develop), reject wafers and rework rate cycle time performance was also tested. In total, five test lots and five production lots selected to run the DOE test. All the cycle time data which was collected through this DOE test analyzed using Minitab 17 statistical software. The analyzed report shows that the cycle time for RGAE method could be achieved within 2 hours. This success could be achieved by allowing the rejected wafers to run automatically by using the alternative flow until the wafers successfully exposed. Furthermore, with the (RGAE) framework, the production can save time for split, rework, remask and merge all the wafers. The experimental result shows that (RGAE) framework able to provide fast solution by achieving 97% reduction of cycle time for pad inductor layer comparing to Manual Global Alignment (MGA) method.

ABSTRAK

Litografi adalah suatu proses utama yang memindahkan corak daripada reticle kepada lapisan wafer dan pad induktor merupakan lapisan terakhir di dalam hirarki Litografi. Kitaran masa untuk lapisan pad induktor menunjukkan peningkatan kerana mempunyai 32% daripada ralat penjajaran global (GA) sebulan di Silterra Malaysia Sdn Bhd. Dalam masa yang sama, masa kejuruteraan akan diambil lama untuk menyelesaikan masalah lot untuk menjalankan proses "expose" dan "develop". Ini adalah kerana, masa penggunaan mesin terhad untuk digunakkan oleh Jurutera Proses di dalam keadaan mod manual. Kebanyakan lot dihantar untuk kerja semula menyebabkan kos proses "wafer" meningkat. Matlamat projek ini adalah untuk mengurangkan masa kitaran untuk lapisan pad induktor dengan memperkenalkan rangka kerja yang dikenali sebagai "Remote Global Alignment Error" (RGAE) dengan aliran alternatif. Untuk itu, sebuah metodologi direka jika menghadapi ralat penjajaran global (GA). Semasa proses itu, lot akan secara automatik dimuatkan dengan menggunakan rangka kerja "Remote Global Alignment Error" (RGAE) dengan memilih "wafer" yang ditolak untuk proses "expose" dan "develop". Melalui rangka kerja ini, membolehkan menjimat lebih banyak masa untuk memisahkan "wafer" yang biasanya akan dihantar untuk kerja semula atau menjalankan lot secara mod manual. Beberapa ujian DOE dijalankan untuk membandingkan prestasi masa kitaran rangka kerja (RGAE) dengan kaedah "Manual Global Alignment" (MGA). Selain itu, tiga proses photolithography utama ("coat", "exposure", "develop"), "wafer" yang ditolak dan kadar kerja semula untuk prestasi masa kitaran juga diuji. Secara keseluruhannya, lima lot daripada ujian dan lima lot daripada produk pengeluaran dipilih untuk menjalankan ujian DOE. Semua data masa kitaran yang dikumpulkan melalui ujian DOE ini dianalisis dengan menggunakan perisian statistik Minitab 17. Laporan analisis menunjukkan bahawa masa kitaran dengan untuk rangka kerja (RGAE) dapat dicapai dalam masa dua jam. Kejayaan ini dapat dicapai dengan membenarkan "wafer" yang ditolak untuk dijalankan secara automatik dengan menggunakan aliran alternatif sehingga "wafer" tersebuat berjaya "expose". Selain itu, dengan menggunakan rangka kerja (RGAE), syarikat dapat menjimatkan masa untuk memisahkan "wafers", kerja semula, mengulang semula dan menggabungkan semua "wafer". Hasil eksperimen menunjukkan bahawa rangka kerja (RGAE) dapat mampu memberikan penyelesaian yang cepat dengan mencapai 97% pengurangan masa kitaran untuk lapisan pada pad induktor yang membandingkan dengan kaedah "Manual Global Alignment" (MGA).

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μm	-	micrometer
L_{Pitch}	-	pitch
$L_{Overlap}$	-	minimum overlay
L_{Space}	-	distance
M_{Mean}	-	average
M_{Sdv}	-	standard deviation
$M_{Run\text{-}out}$	-	expansion
L	-	diameter

LIST OF PUBLICATIONS

Saandilian, D., Shajahan, M., Tritham, W., 2017. Remote Global Alignment Error for Cycle Time Improvement of Pad Inductor Layer. *In Journal of Advanced Manufacturing Technology (JAMT),* 12(11).

Saandilian, D., Shajahan, M., Tritham, W., Nurul, H., Hong, L.K., 2016. Remote Global Alignment Error for Pad Inductor Layer to Improve Cycle Time. *In Proceedings of the 2016 International Conference on Industrial Engineering and Operations Management (IEOM)*, pp. 612.

CHAPTER 1

INTRODUCTION

1.1 Introduction

Semiconductor wafer fabrication is a procedure composed of many repeated sequential processes to produce complete electrical or photonic circuits. Examples include production of radio frequency (RF) amplifiers, LEDs, optical computer components and CPUs for computers.

Integrated Circuit (IC) is fabricating process for a various step sequence of chemical and photographic processes that performed on the wafer. A wafer or substrate fabricated on a thin slice of silicon is mainly used in most semiconductor chips companies. The various processes used to make an integrated circuit (IC) on the wafer are photolithography, resist removal, etching, layering, wafer cleaning and doping. Figure1.1 represents one cycle of the primary steps and their sequence.

On the other hand, May (2006) explained more details regarding layering techniques that used to grow thin layers of film on the wafer surface. Photolithography uses light to transfer a geometric pattern from a photomask to a light-sensitive photoresist on the substrate. The photoresist needs to be stripped away. Etching is the process of using strong acid to cut into the unprotected parts of a metal surface to create a design in the metal. Doping is the process of impurity atoms being used in order to define the electrical properties of this region. Cleaning is used to remove particulates and chemical impurities so contaminant-free surfaces can be obtained.

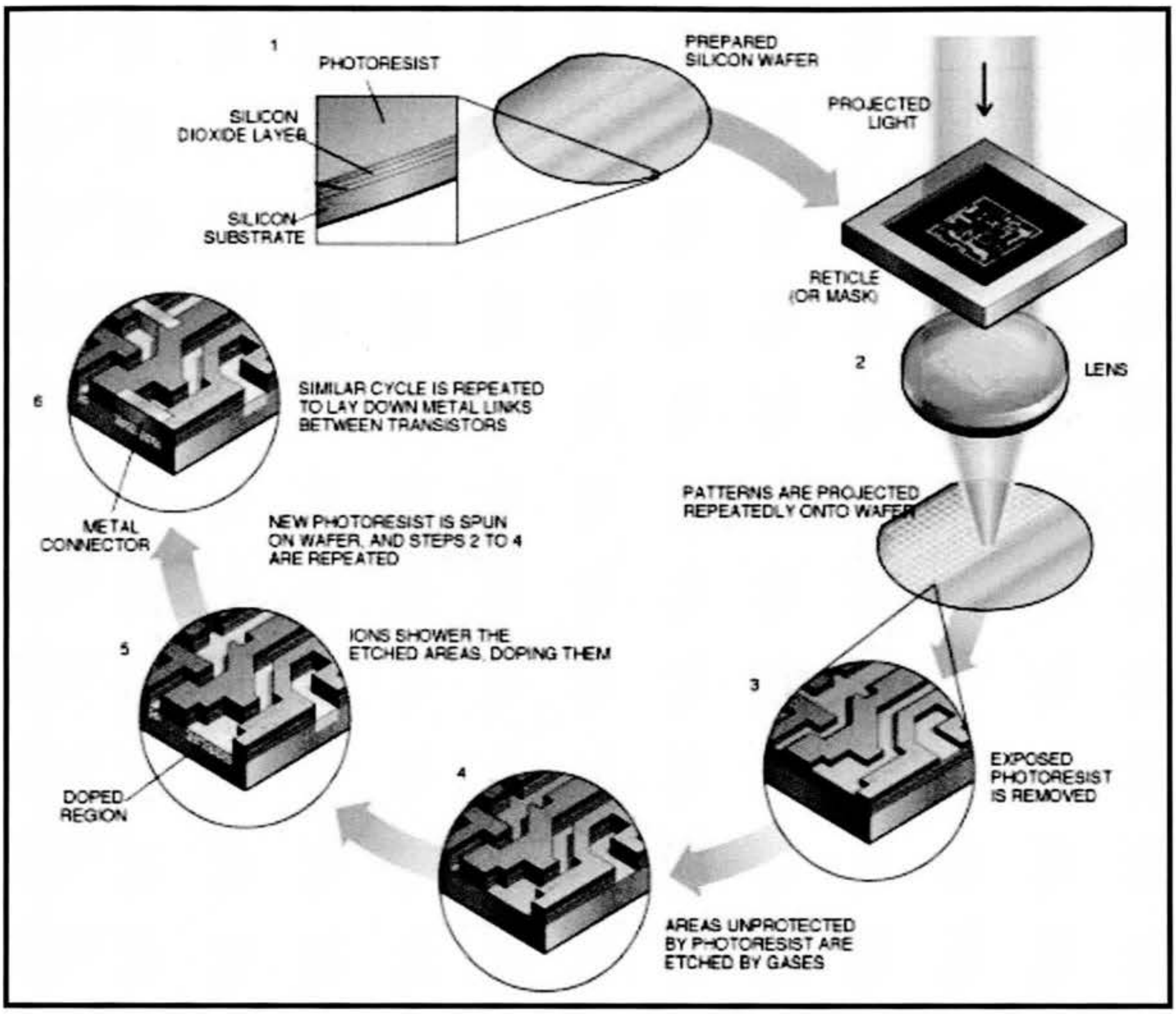

Figure 1.1: Semiconductor Wafer Process Flow (Spierings, 2013).

In the semiconductor wafer process, the photolithography process has the most expensive equipment and one of the bottleneck process compared to other wafer fabrication processes in the production line. Photolithography is the temporarily coat photoresist on wafer and transfers designed pattern to the photoresist. It is the core of the manufacturing process flow (Yen, 2012).

The goal of the photolithography process is to determine the high resolution, high photoresist sensitivity, precision alignment within 10 percentage of minimum feature size, precise process parameters control and low defect density (Lai, 2009).

The process sequence for photolithography is photoresist coating, alignment, exposure and photoresist developing the layer (Lucas, 1999). It requires high resolution, high sensitive, precise alignment and low defect density that contributes to high yield and good imaging. Figure 1.2 shows the photolithography process flow in wafer fabrication.

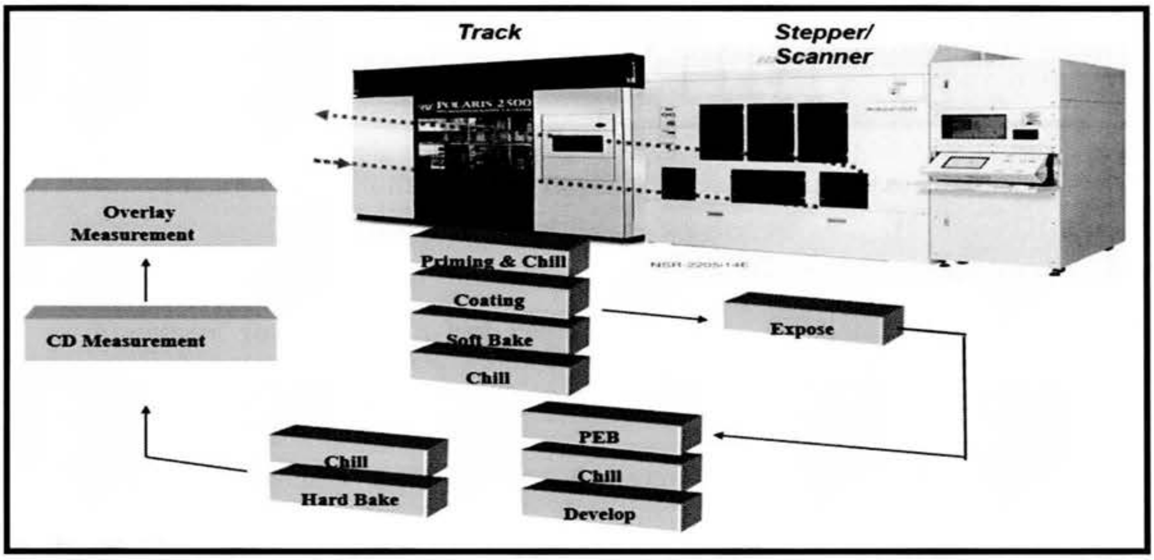

Figure 1.2: Photolithography Process Flow (Spierings, 2013).

The photolithography process flow is repeated for up to 30 times for one device (depending on technology and device). The repetition of this process normally requires different reticles (poly, contact, metal, via & pad inductor) which have different chrome patterns on it (Saandilian, 2016). However, some layers like some implant layers share the same reticle. Figure 1.3 shows that photolithography layer sequence flow. It starts from the first layer (island) until the last layer (pad inductor). The pad inductor or passivation layer is the last layer performed in photolithography to prevent physical damage (scratches) and as a barrier to mobile ion contaminants.

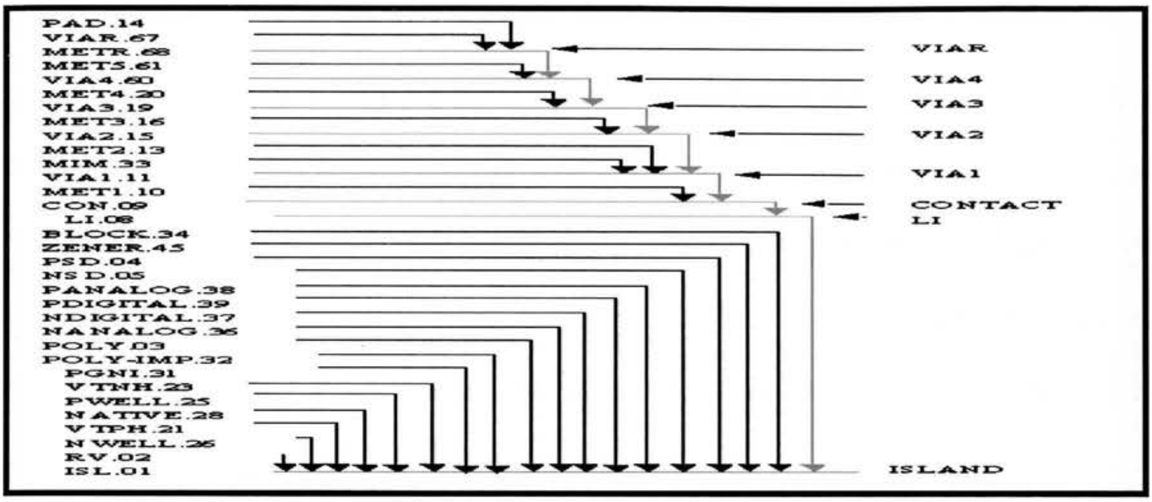

Figure 1.3: Photolithography Layer Sequence (Saandilian, 2016)

Alignment (overlay) is a key challenge process in photolithography since the minimum dimension of integrated circuits (ICs) has been shrinking (Zhang, 2013). Modern CMOS integrated circuits have almost 30 layers to be aligned perfectly to avoid misalignment. Alignment marks are placed on the wafer at the beginning of the process during the first level of photolithography. Furthermore, the good alignment mark can prevent misalignment that induces to reduce overall photolithography cycle time (Saandilian, 2016).

In wafer fabrication, reduction of cycle time is very important for all semiconductor process (Chen, 2013b). Cycle time consists of queuing time for reticle changes, tool downtime, engineering work, preventative maintenance, visual inspection time, production processing time and lot transportation time. The main objective of the cycle time is to have a shorter cycle time (Spierings, 2013).

One of a most important part of photolithography is a reduction of cycle time for pad inductor layer; since it is the last layer in photolithography (Saandilian, 2016). Manufacturing always gives high priority to pad inductor layer in determining not have any delay in the process.