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3.3V DC Output at -16dBm Sensitivity and 77% PCE Rectifier for RF Energy Harvesting

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ABSTRACT

This paper presents a high voltage conversion at high sensitivity RF energy harvesting system for IoT applications. The harvesting system comprises bulk-to-source (BTMOS) differential-drive based rectifier to produce a high efficiency RF energy harvesting system. Low-pass upward impedance matching network is applied at the rectifier input to increase the sensitivity and output voltage. Dual-oxide-thickness transistors are used in the rectifier circuit to maintain the power efficiency at each stage of the rectifier. The system is designed using 0.18µm Silterra RF in deep n-well process technology and achieves 4.07V output at -16dBm sensitivity without the need of complex auxiliary control circuit and DC-DC charge-pump circuit. The system is targeted for urban environment.

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1. INTRODUCTION

In recent years, much attention has been placed on the Internet of Things (IoT) technology. IoT refers to the vast network of physical devices that are connected to the internet via built-in sensors, software and necessary electronic circuits allowing the devices to send, receive and exchange data [1-2]. The 'Things', for example home appliances are put into home network and can be controlled by using voice, remote control or smartphone via the internet. In large-scale deployment area such as Smart Cities, billions of sensors are needed to control the 'Things'. These wireless sensor nodes are normally powered by batteries which are known for its limited lifetime and the use of batteries in large area network are not practical as it involves the cost of purchase, maintain and dispose of large amount of batteries [3]. There are also few cases where the application of batteries are not feasible such as device that is used to monitor a structure or the environment (e.g. volcano) due to the need of recharging or replacing the battery. As the alternative solution to the limitations of batteries, energy harvesting system is used to power the IoT devices.

Energy harvesting is a process of harnessing energy from ambient environment and converts the energy into electricity to power electrical or electronic devices [4]. Energy from sunlight, vibration, radio frequency (RF) [4-5] and etc. is captured, to be used directly or accumulated and stored in a storage component like a battery or a capacitor for a period of time for later use. RF energy has very less power density compared to other energy sources and can be easily integrated into a small chip making it suitable for IoT applications [6]. Furthermore, RF energy is available for almost everywhere and anytime thanks to the

growing of radio wave sources such as wireless LAN transmitters (Wi-Fi) [7], TV [5][7-9], FM/AM radio, mobile base stations [5][9] and mobile devices [5]. RF energy is a form of differential alternating current (AC) sources and rectifier is required to convert the differential signal captured by antenna into single direct current (DC). The output of rectifier will be passed to few circuits to form a reliable output before the output signal can be used for electronic circuits. Due to low density of the harvested RF source from ambient environment, it is important to achieve an energy harvester system with high sensitivity. This paper is organized as follows: Section 2 discusses principle of RF energy harvesting system and reviews the previous designs of rectifier for energy harvesting. Section 3 introduces the architecture and characteristic of the proposed system. Section 4 presents the simulation results and discussions of the proposed circuits followed by the conclusion in Section 5.

2. RF ENERGY HARVESTING WORKING PRINCIPLE AND DESIGN REVIEW

2.1. Rectifier

Figure 1 shows the typical RF energy harvesting system. RF energy is captured by antenna and converted into DC voltage by rectifier. Typically, the output voltage produced by rectifier is small and decreases as the sensitivity increases due to the nature of antenna that captures very small energy [6]. Therefore, impedance matching is applied between the antenna and rectifier to provide maximum energy transfer to the circuit [10-12]. The sensitivity of rectifier determines the capability of a rectifier to be operated when very small energy is available in the surrounding. High sensitivity allows efficient transmission of energy at greater distances from RF sources [13]. Due to the small output voltage produced by rectifier, DC-DC charge pump is used to boosts the output voltage to a higher usable voltage level [7][14]. The voltage then is regulated by voltage regulator to provide a stable DC voltage that is independent to input voltage and load current.

The efficiency of rectifier is critical in designing RF energy harvesting system. High efficiency rectifier reduces power dissipated during the RF-DC conversion. Rectifier efficiency is defined by the power conversion efficiency (PCE) factor as in Eq. (1) where Ploss is the conduction power losses in the rectifier. The efficiency depends on threshold voltage (V_{th}), channel resistance (r_{on}), leakage current and current drive capability of rectifier [6]. Low V_{th}, r_{on}, leakage current and high driving capability reduce the voltage drop across the rectifier, thus increasing the efficiency.

$$\text{PCE}, \eta\% = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{out} + P_{loss}} \times 100 \quad (1)$$

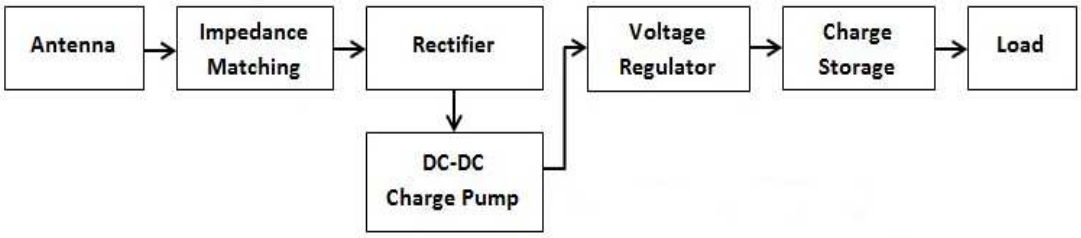


Figure 1. RF energy harvesting system

The low V_{th} and leakage current can be achieved by applying differential-drive rectifier (DDR) circuit as shown in Figure 2. DDR consists of 4 transistors with cross-connected gate structure to form a complimentary bridge rectifier. The gate of transistors is actively biased by differential mode signal at two nodes, Vx and Vy [15]. When Vx is positive, M_{n2} and M_{p1} are in forward bias and act as small on-resistance causing the V_{th} of the devices to decrease effectively [15]. The transistors will turn-on when Vx reaches the V_{th}. On the other hand, as Vy is negative, M_{n1} and M_{p2} are in reverse bias causing the V_{th} of the transistors to increase, reducing the reverse leakage current. The differential signal applied at both of the input of rectifier allows both low V_{th} and leakage current to be achieved simultaneously, increasing the efficiency and sensitivity. The output voltage produces by DDR is defined as in Eq. (2) where V_{RF} is the input AC signal and V_{drop} is the voltage loss across the transistor during circuit operation.

$$V_{DC,\,out} = 2V_{RF} - V_{drop} \quad (2)$$

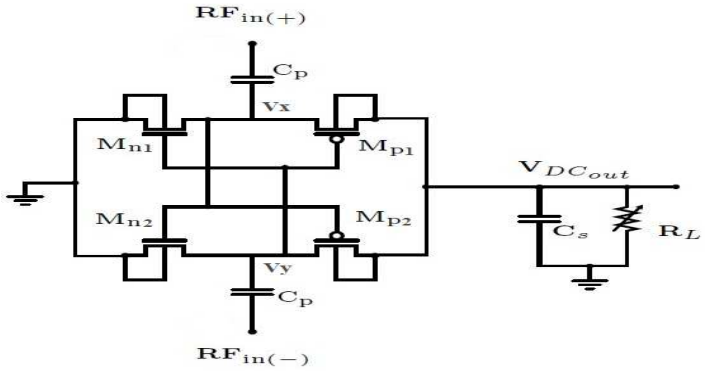


Figure 2. Differential-drive rectifier (DDR)

2.2. Design Review

There are few types of rectifier architectures have been proposed for the application of RF energy harvesting. For example, Dickson multiplier or also known as voltage multiplier has been used by [16] as shown in Figure 3 to convert the RF signal into DC. In order to achieve high sensitivity rectifier, all of the transistors used in the rectifier are operated in weak inversion. One parallel inductor or a shunt inductor is applied between the antenna and the rectifier to work as voltage boosting circuit to further increase the sensitivity. The rectifier is designed with few types of transistors include zero V_{th} transistor (ZVT), zero V_{th} transistor with thick oxide (ZVTDG), low V_{th} transistor (LVT), normal V_{th} transistor (NFET) and 3.3V I/O transistor with thick oxide (NFET33) rectifiers with different numbers of stages to differentiate the effects of the V_{th} to the sensitivity. At -22.1dBm and 10-stages with ZVT technique, the rectifier able to produce an output voltage of 1V. -32.1dBm sensitivity is achieved at 50-stages rectifier with LVT technique and producing 1V output voltage. Although the rectifier has very high sensitivity, the output however is small and not adequate to supply electronic circuit that requires 3.3V supply voltage. It also has too many stages which consumed large area and space. Another way to increase to output voltage is by increasing the load however this might greatly decreases the efficiency considering large voltage loss experienced by the rectifier as the number of stage increases as shown by Eq. (3).

$$V_{out} = 2N(V_{RF} - V_{drop}) \quad (3)$$

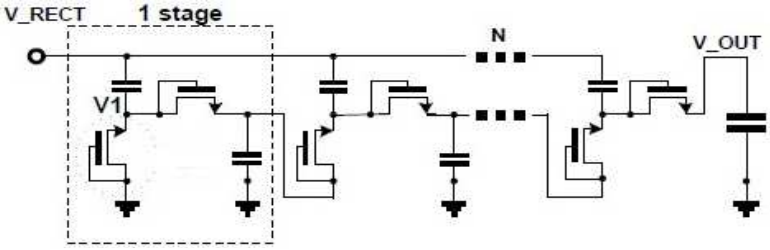


Figure 3. Dickson multiplier [16]

Ref [17] proposed an enhance voltage multiplier circuit by implementing bulk-biased or dynamic threshold MOSFET (DTMOS) to the rectifier to reduce the V_{th} of the transistor thus decreasing the voltage loss across the rectifier. The rectifier is cascaded to 3-stage to increase the output voltage. At 900MHz and -2.3dBm sensitivity, the rectifier produced an output of 1.2V with 48% power efficiency. In DTMOS transistor, the bulk which usually connected to the source in conventional transistor is connected to the gate or the drain of the transistor, as shown in Figure 5. This has forcing the body-to-source voltage (V_{bs}) to be equal to gate-to-source voltage (V_{gs}). When $V_{gs} = V_{bs} = 0$, the V_{th} is high, causing the leakage current to reduce. When $V_{gs} = V_{bs} = V_{max}$ (amplitude of input signal), the source and the substrate is in forward bias forcing the V_{th} to drop.

Although DTMOS transistor has low V_{th}, its operating voltage however is limited to its V_{th} [18][19]. This is due to excessive increase in leakage current when the applied voltage exceeds the V_{th} [18][19]. This type of rectifier also introduces large voltage drop across the rectifier as the stage of the rectifier increases. Further increasing in load resistor or stage of the rectifier to increase the output will greatly decrease the efficiency making it not suitable for high sensitivity with large output voltage rectifier.

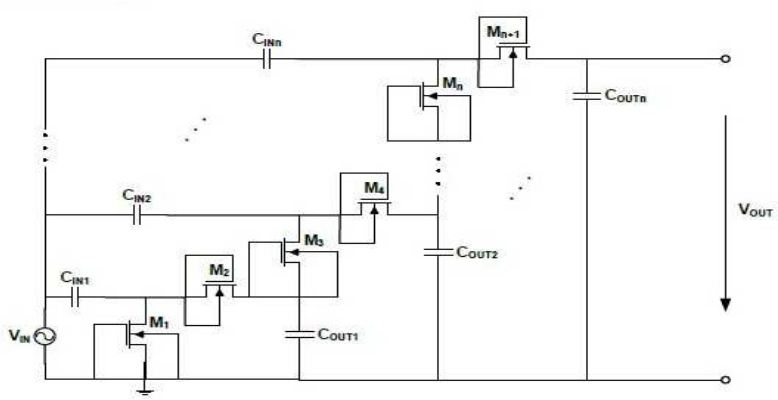
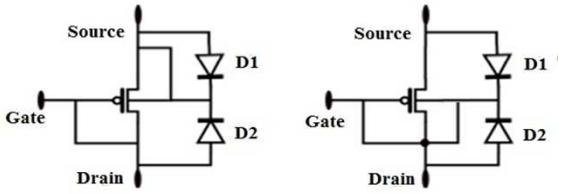


Figure 4. DTMOS voltage multiplier [17]



(a) (b)

Figure 5. (a) BTMOS and (b) DTMOS transistors

Ref [20] also had proposed an enhanced Dickson voltage multiplier rectifier by applying ultra-low power (ULP) diode. ULP diode composes of a pair of PMOS and NMOS transistors where the gate of PMOS transistor is connected to the source of NMOS transistor and vice versa. The body of the NMOS is connected to the lowest potential node while the body of PMOS is connected to the highest potential node. The structure of the ULP diode is shown in Figure 6. As the diode is positively biased, both the NMOS and PMOS transistors are operate in forward bias with forward current similar to the conventional MOS diode. In reverse bias operation, the source terminals of both transistors are connected together and the transistors are operated in subthreshold region. As the reverse voltage increased, the current increases with the increase in drain-to-source voltage (V_{ds}). As the cut-off of V_{gs} increase, the current then decreases exponentially reducing the leakage current and maintaining a good forward current. At 900MHz operating frequency, the proposed 3-stage Dickson multiplier with ULP diode produces 0.214V output at -10dBm sensitivity with 17.74% efficiency.

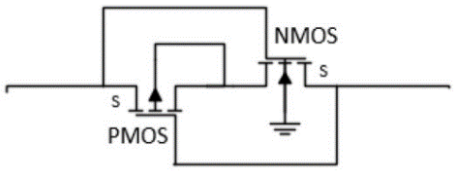


Figure 6. Ultra-low power (ULP) diode [20]

Another improvement on voltage multiplier performance has been made by ref [21]. 5-stage voltage multiplier that operates at 900MHz and 50Ω input source are used in the reseach work. The output of the rectifier is connected to a voltage regulator to generate a constant DC output voltage. DTMOS-type transistor is used in the rectifier to reduce the V_{th}. A shunt inductor and a series inductor as shown in Figure 7 are connected between the antenna and the rectifier to increase the sensitivity of the circuit. The rectifier produces an output voltage between 1.8V to 2V at -18dBm with 18.08% efficiency. A voltage limiter is applied between the rectifier and the voltage regulator to avoid the transistors in the regulator from breaking down. As the rectifier starts to operate, the output voltage of the rectifier increases slowly until it achieved the desired output voltage. The output voltage is then regulated by the proposed voltage regulator. Very low

efficiency is expected to be achieved by this rectifier to generate the 3.3V DC voltage due to the large voltage drop across the rectifier during circuit operation.

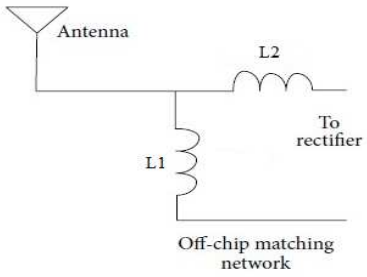


Figure 7. Shunt and series inductor impedance matching for RFEH [21]

Figure 8 shows the DDR schematic proposed by ref [22]. The rectifier is cascaded to 5-stage and operates at 915MHz. An off-chip series inductor is applied at the rectifier's input to resonate the capacitance from the rectifier and boosts the quality factor ($Q_{-factor}$) in order to achieve high efficiency rectifier. At -3dBm sensitivity, the rectifier achieves 66% power efficiency and produces 4V DC output voltage. In comparison with the previous rectifier discussed in this section, this proposed rectifier produces better efficiency and high output voltage. The output voltage is adequate to power low-power electronic devices. The sensitivity however is low, and the circuit will not be able to operate when very little RF signal is available in the surrounding. Increasing the load resistor able to increase the sensitivity however this costs the power efficiency. The rectifier is designed using standard 0.35µm process technology. High output voltage generated by this rectifier might damaging the device because the output has exceeded the transistor's breakdown voltage [22].

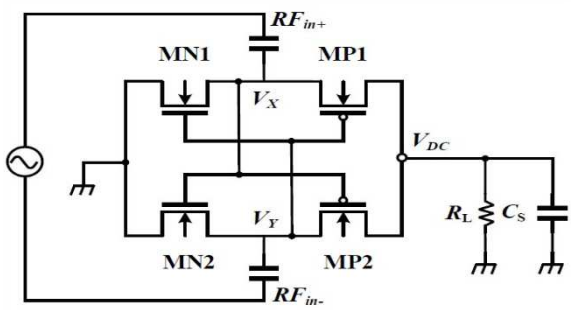


Figure 8. Differential-drive based rectifier [22]

Ref [23] proposed a double rail differential-drive rectifier with an enhance DTMOS body biasing technique as shown in Figure 9 and Figure 10. In this rectifier, the bulk of the PMOS transistors (P1 – P4) are dynamically biased with positive DC voltage and the bulk of the NMOS transistors (N1 – N4) are connected to the source. The positive and negative rails in the double-rail rectifier produce a symmetric output DC voltage. For the positive rail the bulk of the PMOS is connected to DC_{in} while for the negative rail the bulk of the PMOS is connected to DC_{out}. The rectifier operates at 953MHz frequency and achieves 69.5% efficiency at 5.2dBm sensitivity and 2kΩ load resistance. A maximum of 3.5V output voltage is produced at this sensitivity and efficiency. Although the rectifier has good power efficiency and able to generates 3.5V output voltage, the sensitivity however is too low. In order to obtain higher output voltage at higher sensitivity, larger load resistor is required. However, further increasing in load resistance reduces the efficiency. Furthermore, DTMOS transistor has lower V_{th} and leakage current thus providing better efficiency when compared to the conventional bulk-to-source transistor. However, this ability is limited by the transistor's V_{th} as DTMOS transistor's body current increases excessively when V_{gs} exceeds the V_{th} [18][19]. Generating large DC voltage at higher sensitivity will greatly decrease the rectifier's efficiency.

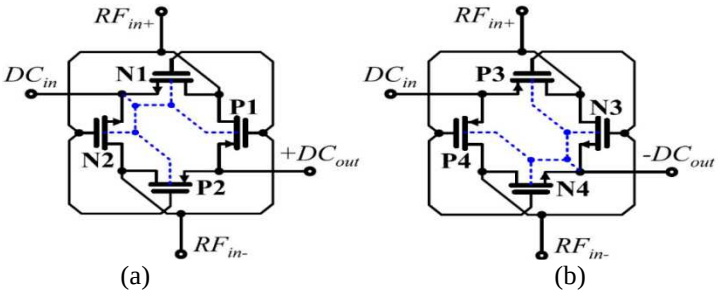


Figure 9. (a) Positive and (b) Negative DDR with lower DC Feeding Body Biasing Technique [23]

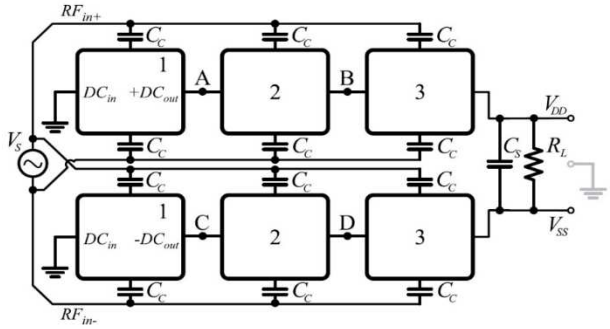


Figure 10. 3-Stage Double-Rail DDR [23]

3. PROPOSED RF ENERGY HARVESTING SYSTEM

3.1. Dual-gate-thickness Differential-drive Rectifier

Due to the ability of differential-drive based rectifier providing both low V_{th} and leakage current simultaneously, the proposed rectifier is designed by implementing bulk-to-souce (BTMOS) differential-drive based rectifier cascaded in to 6-stage to achieve high DC output voltage at high sensitivity. Typically, the rectifier is designed by using thin-oxide transistor as it has small channel length, r_{on} and fast switching speed which are very important in achieving high efficiency rectifier. However, the physical ability and structure of this transistor is limited by the voltage operation such that its gate and drain voltage are limited to 1.8V only [24]. Further increasing in operating voltage applied to this transistor may cause to poor transistors' performance and breakdown.

For high voltage operation, thick-oxide transistor should be used. Thick-oxide transistors have much thicker gate-oxide-layer and longer channel length allowing it to operate at much higher voltage than the thin-oxide (between 3.3V to 5V) [22]. It has lower speed performance when compared to the thin oxide but has lower leakage current which is beneficial in maintaining the efficiency of the rectifier.

The proposed rectifier is divided into two parts as shown in Figure 11. The first three stages are designed by using the thin-oxide transistors and the next three stages are designed by using thick-oxide transistors. Both types of transistors are used in this proposed circuit to achieve better efficiency at each stage of the rectifier since thin-oxide and thick-oxide transistors have the best performance at lower voltage and higher voltage operation respectively.

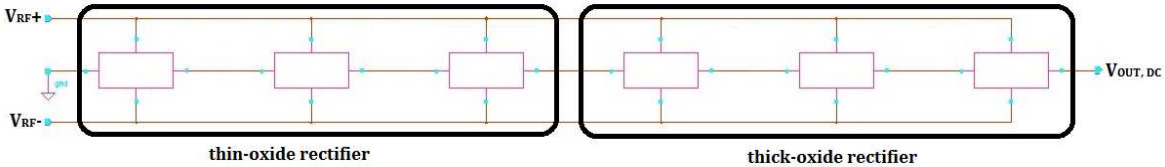


Figure 11. Proposed differential-drive rectifier

3.2. Low-pass Upward Matching Network

In ideal case where the system is lossless, maximum voltage is transferred from the source to the rectifier, resulting high sensitivity system. Practically, the impedance of the source and rectifier impedance is not the same and voltage losses are presented in the circuit [25]. If source resistance is higher than the main

circuit, most power ends up being reflected at the source. To force the rectifier impedance to be equal as the source, low-pass upward matching network is used to deliver a pumped-up voltage from the source to the rectifier. The circuit is said to achieve maximum power transfer when the rectifier impedance is equals to the source resistance (R_S) as shown in Eq. (4) where Z_S is the source impedance and Z_R* is the complex conjugate of the rectifier. $R_{\_RECT}$ and $jX_{\_RECT}$ is the rectifier resistance and reactance respectively.

$$Z_S = Z_R^*, Z_R^* = R_{\_RECT} + jX_{\_RECT} \quad (4)$$

Low-pass upward matching network shifts upward the impedance of $R_{\_RECT}$ to be identical as the R_S. Figure 12(a) shows the modelling diagram of DDR and its resistance and reactance with a low-pass upward L-matching network. Since the rectifier mainly composes of transistors, its reactance typically consists of capacitance which carries the negative reactance ($C_{\_RECT}$) [25]. To eliminate this negative reactance, a positive reactance is needed. This is shown in Figure 12(b). The inductor, $L_{\_RECT}$* which has positive reactance, will resonate the negative reactance of the $C_{\_RECT}$ leaving only the identical source and rectifier resistances.

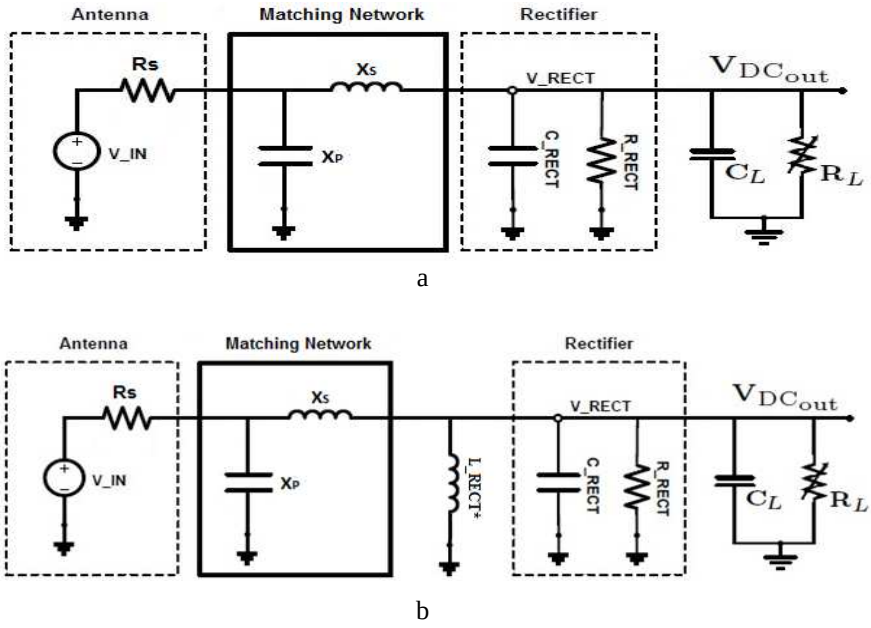


Figure 12. (a) DDR's resistance and capacitance model with low-pass upward matching network, (b) DDR's resistance and capacitance model with impedance matching network and resonating inductor, $L_{\_RECT}$*

The matching circuit consists of parallel capacitance (X_P) and series inductance (X_S) and sees terminations with only R_S and load resistor (R_L) present. The quality factor (Q-factor), X_S and X_P can be calculated as in Eq. (5), (6) and (7) respectively. As shown in Figure 12(b), X_S is in series with $L_{\_RECT}$*. Therefore, the total positive reactance, X_{S_Total} is calculated as in Eq. (8) where f_S is the source frequency, C_P is the capacitor in parallel, L_S is the inductor in series and X_{L_RECT} is the inductance of $L_{\_RECT}$*.

$$Q_{-factor} = \sqrt{\frac{R_S}{R_{\_RECT}} - 1} \quad (5)$$

$$X_P = \frac{R_S}{Q_{-factor}} = \frac{1}{2\pi f_S C_P} \quad (6)$$

$$X_S = Q_{-factor} R_{\_RECT} = 2\pi f_S L_S \quad (7)$$

$$X_{S\_Total} = X_S + X_{L\_RECT} \quad (8)$$

4. RESULTS AND ANALYSIS

The circuit is designed using 0.18µm Silterra RF CMOS in deep n-well technology. The system is designed to match a 50Ω source impedance at 900MHz input frequency that is capable to produce at least 3.3V DC voltage at minimum of -15dBm sensitivity. RF deep n-well transistor type is used in the rectifier circuit to isolate the substrate of the NMOS from its origin substrate to form a bulk-source transistor.

4.1. Proposed Rectifier

The performances of the proposed rectifier circuit are shown in Figure 13 and 14 for schematic and post-layout simulation respectively. The rectifier achieves the highest PCE of 78.76% with 3.904V output voltage for pre-layout simulation and 77.07% of PCE with 4.067V output voltage for post-layout simulation at -16dBm sensitivity.

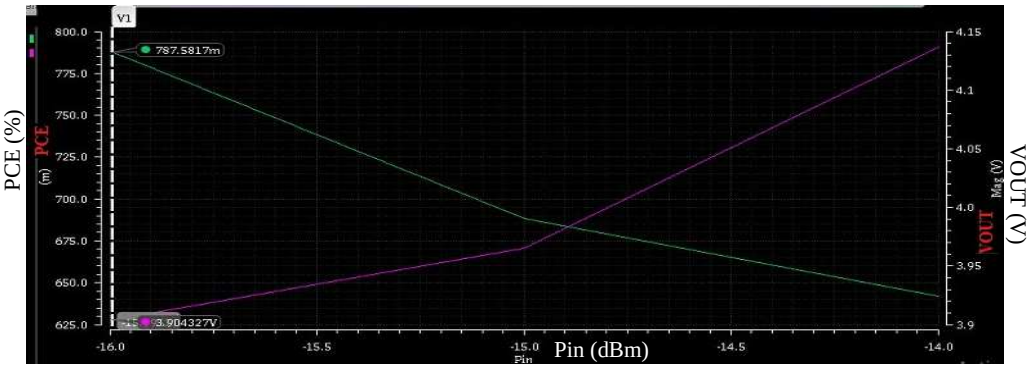


Figure 13. PCE (%) and VOUT(V) vs. Pin (dBm) – pre-layout

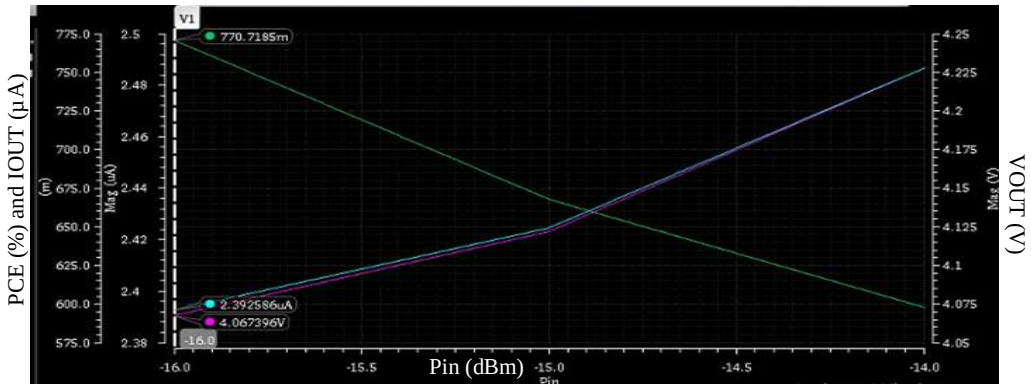


Figure 14. PCE (%), IOUT (µA) and VOUT(V) vs. Pin (dBm) – post-layout

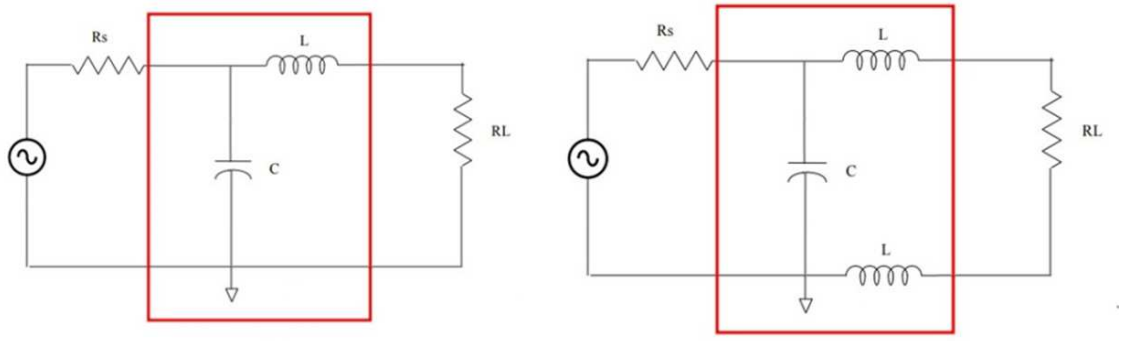
4.2. Impedance Matching

In impedance matching network, reflection coefficient (Γ) or also known as S11 determines how much power is reflected from the antenna or the source. Reflection coefficient is the ratio of the signal reflected from the load to the incident signal and can be calculated as in Eq. (9) where Z_L and Z_S are the load and source impedances respectively. The higher the reflection coefficient, the better the match between the source to the termination circuit. The voltage standing wave ratio (VSWR) is a measure of how well a transmission line is matched to the load. VSWR can be calculated as in Eq. (10) [26]. As discussed in Section 3.2, low-pass upward impedance matching network as shown in Figure 15(a) is applied at the input of rectifier to transfer maximum input power from the source to the rectifier. From Figure 15(a), the total input impedance (Z_{in}) is defined as $Z_{in} = X_L + X_C$ and $X_L = \omega L$ and $X_C = 1/\omega C$. L and C are the inductor and capacitor values and ω is the angular frequency. Rewriting the equation, Z_{in} can be defined as in Eq. (11) and the matching network can be reconfigured as shown in Figure 15(b). It should be noted that Eq. (11) is the general equation to represent the input impedance. The real reactance depends on the transistors models and sizing and is calculated through S-parameter (SP) analysis in Cadence.

$$\Gamma = \frac{Z_L - Z_S}{Z_L + Z_S} \tag{9}$$

$$\text{VSWR} = \frac{1 + |\Gamma|}{1 - |\Gamma|} \tag{10}$$

$$Z_{in} = \frac{1}{2}\omega L + \frac{1}{2}\omega L + \omega C \tag{11}$$



(a) (b)

Figure 15. (a) Single and (b) differential end low-pass upward matching network

From the schematic simulation, the total input impedance of the rectifier without the matching network is equals to 27.99 – j1624. By applying the equation from (5) until (8) and (11), the total ideal inductor and capacitor values would be around 145.8nH and 3.15pF respectively. With the matching circuit, the rectifier achieves the 50Ω source resistance with very small reactance and obtained high reflection coefficient value as shown in Figure 16. Ideal inductor and capacitor are electronic components where no parasitic elements are considered. In practice, parasitic elements exist in these components and the total inductor and capacitor values might be different from the ideal components. In IC design industry, inductor contained very high parasitic capacitance due to its physical structure that usually is formed from the top metal elements. Thus, a fine tune of inductor and capacitor should be done to match the rectifier impedance with the source resistance. In this proposed circuit, the matching network is realized on-chip and the capacitor and inductor are built from MIM capacitor and asymmetrical square inductor (with optimized Q-factor). The post-layout proposed rectifier achieved the highest S11 when the on-chip inductor and capacitor values are at 40.827nH and 1.0555pF respectively and the impedance, Z11 and S11 are shown in Figure 17. The layout of the proposed rectifier and on-chip matching network has a total core area of 1486.1µm x 1178.1µm as shown in Figure 18. Table 1 compares the performance of the proposed rectifier with the previous research works.

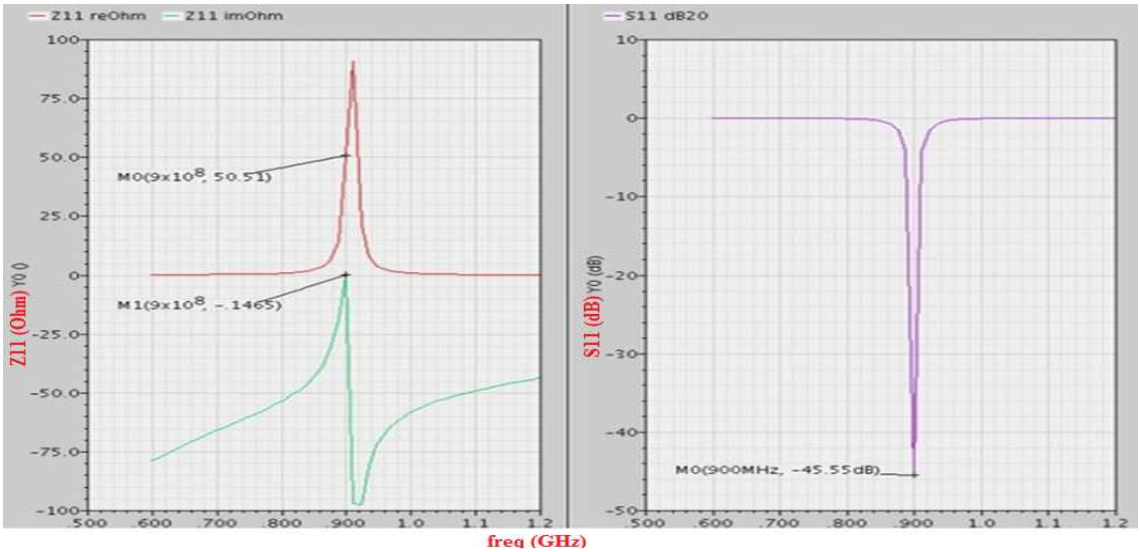


Figure 16. Z11 and S11 Pre-layout DDR with impedance matching

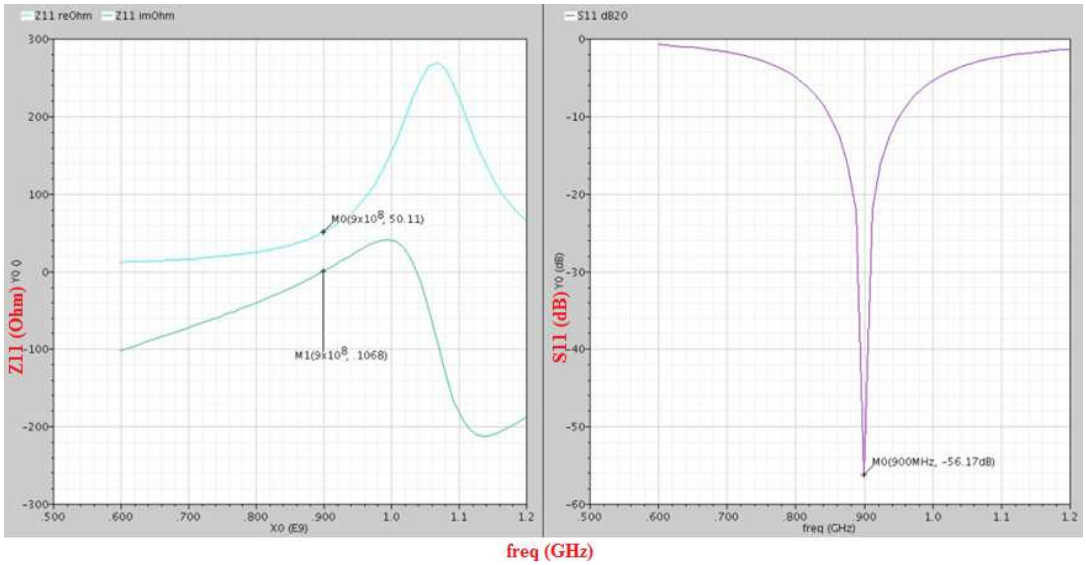


Figure 17. Z11 and S11 Post-layout DDR with on-chip impedance matching

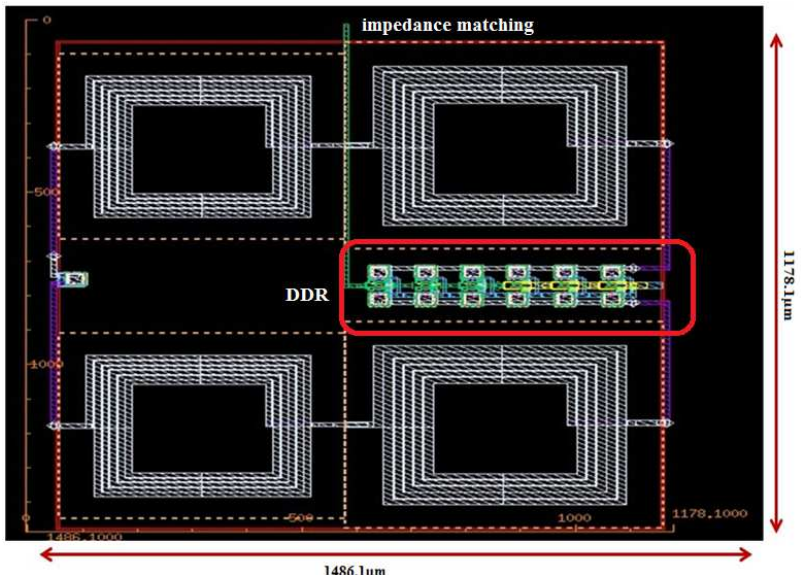


Figure 18. Proposed DDR and impedance matching core layout

Table 1. RF Energy Harvesting performance benchmarking

Topology	[16]	[17]	[20]	[22]	[23]	This Work pre-simulation	This Work post-simulation
Technology (µm)	0.13	0.13	0.18	0.35	0.13	0.18	
Freq. (MHz)	915	900	900	915	953	900	
Pin (dBm)	-32.1	-21.3	-10	-3	5.2	-16	-16
N-stage(s)	50	3	3	5	3, double rail	6	6
PCE (%)	-	48	17.74	66	69.5	78.76	77.71
Vout (V)	1	1.2	0.214	4	3.5	3.9	4.07

5. CONCLUSION

An energy harvesting system that is capable to generate at least 3.3V output voltage at very high sensitivity has been proposed. The system consists of 6-stage BTMOS DDR and low-pass upward impedance matching circuit to obtain high sensitivity and output voltage rectifier. In order to obtain high efficiency rectifier, dual-oxide-thickness transistors are applied to the rectifier. The rectifier is divided into 2 parts where the first three stages of the rectifier are designed by using thin-oxide transistors for stage's output voltage lower than or equals to 1.8V and the next three stages are designed by using thick-oxide transistors for stage's output voltage higher than 1.8V. This is to avoid the rectifier in thin-oxide from performing

poorly after it reaches the maximum 1.8V operating voltage and if using thick-oxide transistor for the whole 6-stage rectifier, it will reduce the PCE as smaller channel length is needed to increase the PCE of rectifier. The proposed rectifier produces 4.067V output at -16dBm sensitivity with 2.39µA load current. Due to the high voltage produced by the rectifier, the need of DC-DC charge pump to boosts the output voltage of rectifier that is typically used in conventional RF energy harvesting system is eliminated which saves the size of core area and the cost of fabrication. The system is targeted for urban environment where the RF sources are easily accessible.

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