International Journal of Power Electronics and Drive System (IJPEDS)
Vol. 10, No. 2, June 2019, pp. 625~635
ISSN: 2088-8694, DOI: 10.11591/ijpeds.v10.i2.625-635

Hardware implementation of single phase three-level cascaded H-bridge multilevel inverter using sinusoidal pulse width modulation

A. Shamsul Rahimi A. Subki[1], Mohd Zaidi Mohd Tumari[2], Wan Norhisyam Abd Rashid[3], Aiman Zakwan Jidin[4], Ahmad Nizammuddin Muhammad Mustafa[5]
[1,2,3,4,5] Departement of Electrionic and Computer Engineering, UTeM, Malaysia
[1,2] Center for Robotics and Industrial Automation, Universiti Teknikal Malaysia Melaka, Malaysia

Article Info

Article history:

Received Nov 27, 2018
Revised Jan 12, 2019
Accepted Feb 3, 2019

Keywords:

Mutilevel Inverter
PSIM Implementatio

ABSTRACT

In this paper a hardware implementation of single-phase cascaded H-bridge three level multilevel inverter (MLI) using sinusoidal pulse width modulation (SPWM) is presented. There are a few interesting features of using this configuration, where less component count, less switching losses, and improved output voltage/current waveform. The output of power inverter consists of three form, that is, square wave, modified square wave and pure sine wave. The pure sine wave and modified square wave are more expensive than square wave. The focus paper is to generate a PWM signal which control the switching of MOSFET power semiconductor. The sine wave can be created by using the concept of Schmitt-Trigger oscillator and low-pass filter topology followed by half of the waveform will be eliminated by using the circuit of precision half-wave rectifier. Waveform was inverted with 180º by circuit of inverting op-amp amplifier in order to compare saw-tooth waveform. Two of PWM signal were produced by circuit of PWM and used digital inverter to invert the two PWM signal before this PWM signal will be passed to 2 MOSFET driver and a 3-level output waveform with 45 Hz was produced. As a conclusion, a 3-level output waveform is produced with output voltage and current recorded at 22.5 Vrms and 4.5 Arms. The value of measured resistance is 0.015 Ω that cause voltage drop around 0.043 V. Based on the result obtained, the power for designed inverter is around 100W and efficiency recorded at 75%.

Corresponding Author:

A Shamsul Rahimi Bin A Subki,
Faculty of Electrical and Electronic Engineering Technology FTKEE,
Universiti Teknikal Malaysia Melaka (UTeM),
76100 Durian Tunggal, Malacca, Malaysia
Email: shamsulrahimi@utem.edu.my

1. INTRODUCTION

Power semiconductor devices is very important in the power electronics field. It will form of a matrix of on or off switches and help to convert the power from one to another one such as AC to DC, DC to AC, DC to DC and AC to AC. Recent technologies require a high demand in practice and fast developing of high power devices [1]. Thus, researchers and industrial companies interested in multilevel inverter due to its relation with control technique. Multilevel inverter (MLI) can improve the output voltage in term of reduce total harmonic distortion and decreases electromagnetic interference problems. Conventional two levels inverter only generates two stages of output voltage, while multilevel inverters can provide more, depends on their designed structure. Therefore, the MLI is used to produce multilevel-output voltages which are purely sinusoidal or synthesis a staircase voltage waveform and thus reduce harmonic content. Higher frequency

harmonics are easier to filter than harmonics near the fundamental frequency. MLI has the advantages of generating better output quality by using pulse width modulation (PWM) technique.

The most common MLI topologies are classified into three types which are neutral point clamped MLI (NPC-MLI), flying capacitor MLI (FC-MLI) and cascaded H-bridge MLI (CHB-MLI). Power rating of inverter is increased with increase in number of level in the inverter [2]. The inverter is the one type of the basic conversion which will transform a low DC power to a high voltage AC power. The inverters are always make use of renewable energy source such as wind, fuel cell and so on. These environmentally friendly energy source can be convert into AC source and used in many application. Besides, the inverters are widely used industrial applications such as variable speed AC motor, induction heating and so on. The output AC source is depends on the input DC source [3].

Pulse width modulation is the main control strategy implemented in the power electronics. This is the best way of driving modern power electronic devices. Most of the power electronic circuits are controlled by PWM signals of various forms such as multi carrier PWM [1-4]. The efficiency parameters of a multilevel inverter such as switching losses and harmonic reduction are principally depended on the modulation strategies used to control the inverter. In addition to these topologies, the modulation control schemes for the multilevel inverter can be divided into two categories which are fundamental switching frequency and high switching frequency PWM. Figure 1 shows the multilevel converter modulation methods. Among various control schemes, the sinusoidal PWM (SPWM) is the most commonly used control schemes for the control of multilevel inverters due to many advantages including easy implementation, lower harmonic output and low switching loss [5].

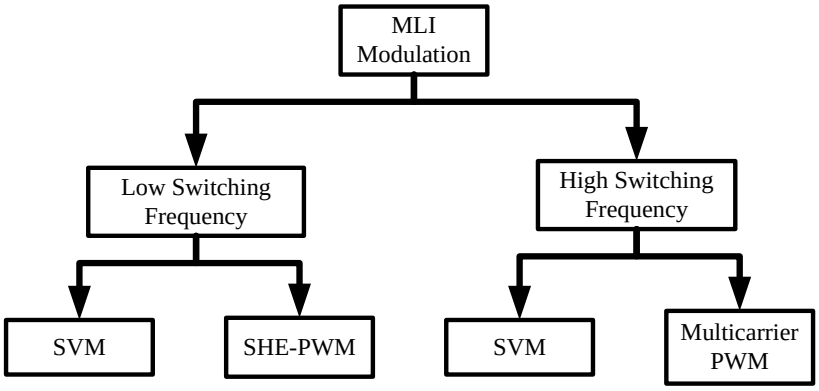

Figure 1. Multilevel converter modulation methods

The multilevel carrier based on PWM, Selective Harmonic Elimination and Space Vector Pulse Width Modulation (SVPWM) are the switching control methods and always used in industrial applications and power electronics [8-9]. The multilevel carrier based on PWM method is the most popular method due to easily implemented. This method can be categories into SPWM and SVPWM [8]. The SPWM is comparing the references wave and the carrier wave to produce the pulse. The carrier based on PWM scheme are classified into phase shifted multicarrier modulation and level shifted multicarrier modulation.

Multilevel inverter structures are becoming increasingly popular for high power applications, their switched output voltage harmonics can be reduced since semiconductors. The MLI is the improvement of the inverter which will transform a high AC source power. There are three type of the multilevel inverter, that is, diode clamped multilevel inverter, flying capacitor multilevel inverter and cascaded H-bridge MLI [6]. This project focuses on cascaded H-bridge MLI which connect all the H-bridge in the series form to obtain a high AC source power. The switching control method is very important to control the power semiconductor devices. The switching control method will reduce the harmonic contents in the output AC [7-10].

In this paper, a step by step design then implementation of the SPWM switching pulse circuit by using MultiSim software is presented. Later on, a complete prototype of cascaded H-bridge multilevel inverter by using a prototype of sine wave generator and triangular wave generator as gating pulse is developed and the finally the result is compared and analyzed for both simulated results and prototype results.

2. RESEARCH METHOD

2.1. Sine wave generator

The Figure 2 shows the circuit that generates the sine wave is composed of a Schmitt-Trigger oscillator and a fourth-order Butterworth low-pass active filter with a Sallen - Key topology. The Schmitt trigger oscillator can produce a square wave by having a symmetric stimulus and the low-pass filter will filter all the harmonics except the fundamental frequency which is sine wave. The frequency of the fundamental wave is equal to frequency of square wave and all-numbered harmonics multiplied by 1/k.

The low-pass filter will mitigate the harmonics, leaving the fundamental wave which is sine wave with about 2% of THD. The frequency of the square wave can be controlled by resistor (R3) and capacitor (C1) on the inverting terminal. The capacitor will charge through the resistor (R3) if the output is in high state. This condition will continue until the voltage at negative terminal is higher than the non-inverting terminal. The cycle continues and result is a square wave. The square wave consists of fundamental frequency sine wave and odd number of harmonic, so, the low-pass filter was design to filter out all the harmonics except fundamental sine wave.

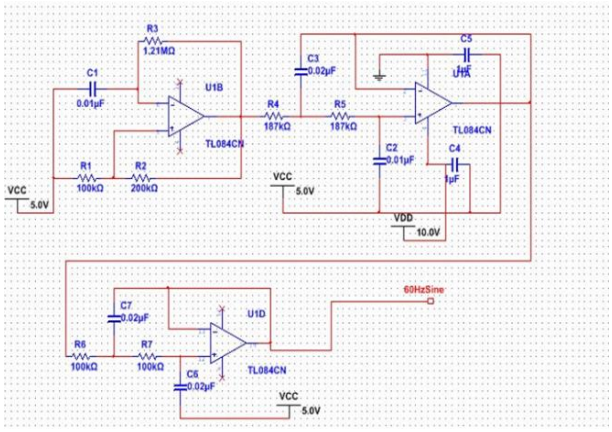

Figure 2. Circuit of sine wave generator

2.2. Precision rectifier

There is no level-shifting of the saw-tooth wave in the IC TL494, so, the circuit of precision rectifier is needed to eliminate the need to level-shifting the saw-tooth wave. Before the sine wave pass to the precision rectifier, one of the sine wave will be flow to the inverting amplifier. Therefore, the inverting amplifier will invert the sine wave and amplifier the amplitude of the sine wave with Rf/R1. The invert sine wave means the phase of the sine wave is 180°out of phase of the original sine wave. Then, both of the sine wave will be passed into the circuit of precision rectifier in order to obtain half-wave.

Figure 3 shows the circuit of precision rectifier including of inverting amplifier. In this case, the amplitude of the sine wave wasn't enlarged because two of those amplitude of sine wave must be in same reading, so, the Rf and R1 are in same value which is 10 kΩ. Then, the sine wave including of original sine wave and 180°out of phase of sine wave will be flowed through the precision rectifier circuit in order to obtain the half-wave of the sine wave. When the positive cycle of the sine wave, the diode D3 and D4 are forward biased, so, the forward biased of diode D3 makes short output of the IC TL084 to the inverting terminal and bypass the R12. When the negative cycle of the sine wave, the diode D3 and D4 are negative biased and this make an open circuit. So, the negative sine wave will be flow to the inverting amplifier with gain – R12/R13. Therefore, the output of the IC TL084 will be positive as the input of the sine wave is negative and the output of the IC TL084 will be zero as the input of the sine wave is positive.

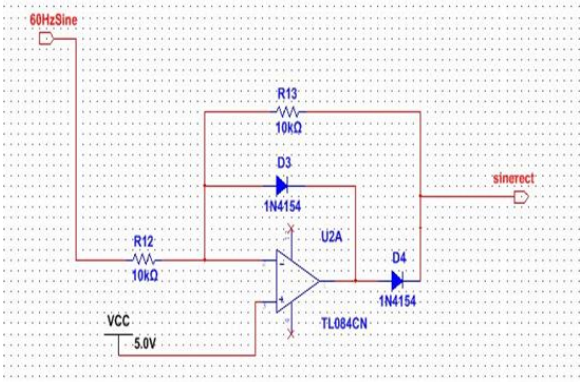

Figure 3. Circuit of precision rectifier

2.3. Inverting gain amplifier

Figure 4 below shows the circuit of inverting gain amplifier. This type of circuit function as to produce a maximum of the PWM duty cycle. The half-wave of the sine wave was inverted in this circuit and the amplitude of half-wave including of 180° out of phase half-wave was enlarged by –R15/R14. In this circuit, the frequency of the both inverting half-wave remain unchanged as previous half-wave frequency. Besides, the voltage divider was construct behind the output of IC LM358. The voltage divider will reduce the DC level of the inverting half-wave in order to maximize the PWM duty cycle.

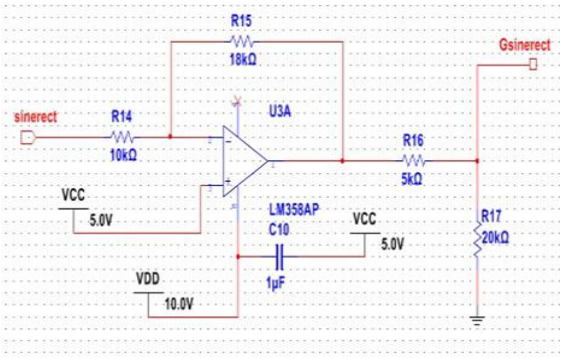

Figure 4. Circuit of inverting gain amplifier.

2.4. PWM circuit

The next step is pass the inverting half-sine wave to the PWM circuit. The construction of PWM as Figure 5. The single-ended application was applied in this circuit, so, the pin output control must connect to ground. The frequency of saw-tooth waveform can be calculated by using Equation 1.

$$f = \frac{1}{R_{24} \times C_{13}} \quad (1)$$

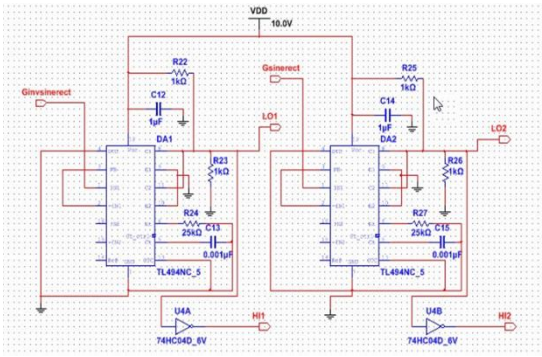

Figure 5. Pulse width modulation circuit

2.5. Cascaded H-bridge multilevel inverter

The simple circuit of cascaded H-bridge multilevel inverter with MOSFET and driver are shown in Figure 6. Due to high switching speeds, the N-channel MOSFET was chosen as the switches in the H-bridge. Besides, the N-channel MOSFET will also minimize the power loss and prevent the damage.

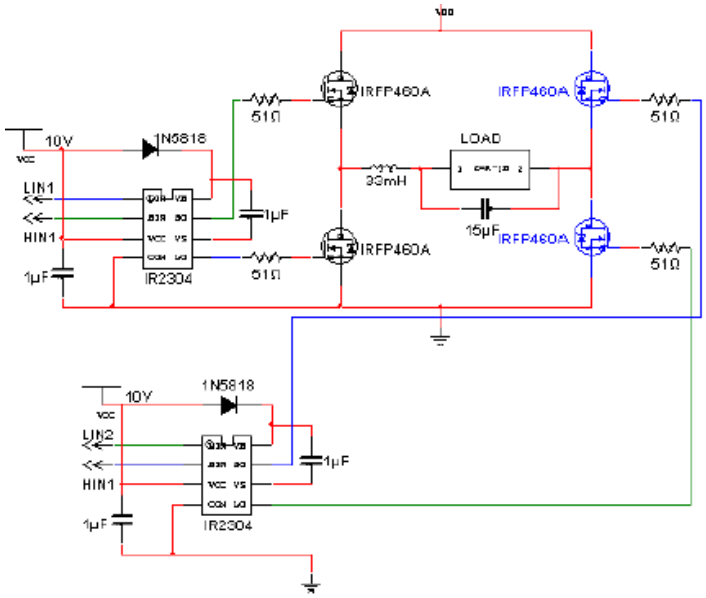

Figure 6. Three level H-bridge MLI

3. RESULTS AND ANALYSIS

The sine wave is successfully created using circuit composed of a Schmitt Trigger oscillator and a fourth-order Butterworth low-pass active filter with a Sallen - Key topology as shown in Figure 7. The whole circuit is made with a single and passive component. The Schmitt Trigger is basically a comparator with hysteresis

Using this topology, the output sine waveform amplitude and frequency created is recorded at 5.36 V at 41 Hz as indicates in Figure 8 below. The signal generation circuit for 3-Level PWM circle around the TL494, device incorporates all the functions required in the construction of a pulse-width-modulation (PWM) control circuit on a single chip. TL494 generates a PWM signal by comparing an internally generated saw-tooth wave with an error signal. In make out DC/AC converter, the error amplifiers with no feedback from the output is used so that the error signal is the signal required is encoded in the PWM output.

TL494 works in the same fashion as the PWM generation of the 2-Level PWM circuit, a few modifications and tweak is required. The modification is divided in to three parts which is (1) externally level shifting the sine wave reference by creating reference half-waves to eliminate the need to level-shift the carrier wave, (2) inverting them to produce the maximum PWM duty cycle, and (3) using pairs of TL494 to

produce each half of the sine wave output. The typical level shifting carrier wave in 3-level PWM systems required using op-amp rectifiers on the reference sine wave. Based on Figure 3, the op-amp precision rectifier works by turning on diode D_3 whenever the input is greater than signal ground. This has the effect of bypassing any current that would go through R_{13}, preventing it from developing a voltage. Since the output is connected to the virtual ground, it is equal to it. When the input is less than signal, the circuit acts like a fixed inverting amplifier with the gain equal to ratio of - R_{13}/R_{12}. Since this circuit rectifies only the half of the sine wave that is less than signal ground, an inverted sine wave is used with another precision rectifier to create the second half-wave for PWM signal comparison. Figure 9 shows the output sine waveform the precision half-wave rectifier.

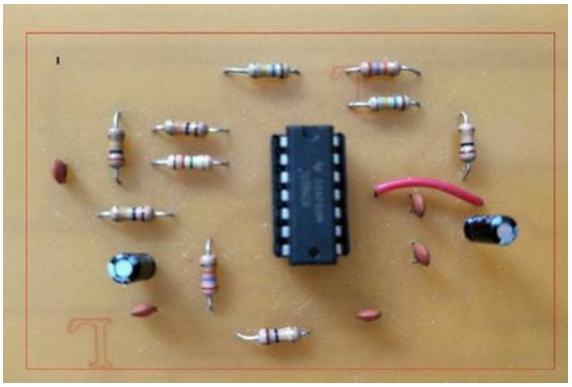

Figure 7. Sine wave generation circuit

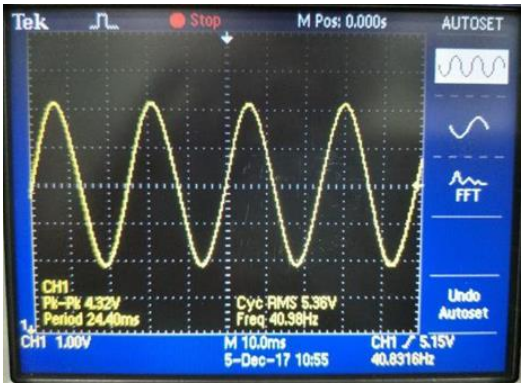

Figure 8. Output sine waveform

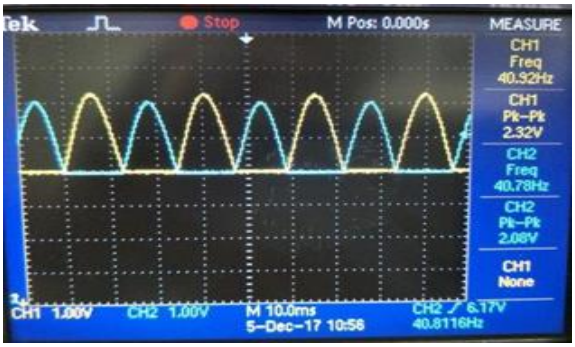

Figure 9. Half-sine wave output sine waveform

Based on our output waveform, the voltage suffering mild distortion. This distortion is created by the negative feedback compensating for the forward drop across the output diode, however, the signals are still operational. These signals should produce the produce the necessary PWM signals when sampled with a carrier wave, but the TL494 produces a smaller duty cycle as the error signal gets larger. This can be thought of as an increasing DC level at the output, and the TL494 compensates by providing shorter pulses. Subsequently, as each of the half-waves reaches its peak amplitude, minimum duty cycle happens. This is the conflicting of the desired effect. Therefore, to overcome this, the half waves created previously will be inverted. Based on Figure 3, LM358 is chosen for the inverting gain stage of the half waves due to this device ability to draw an output voltage very close to negative rails voltage, and will have freedom for adjusting maximum duty cycle, as the TL494 reaches maximum PWM duty cycle as the input reaches 0V, while minimum duty cycle occurs when the input is at about 3V. It should be noted that R_{16} and R_{17} adjust the DC Level of the half-wave and R_{14} and R_{15} adjust the amplitude of the half wave. The values above were experimentally determined to produce the least crossover distortion of the output sine wave while sustaining a realistic amplitude. Figure 10 shows the inverting half-sine output waveform of inverting gain amplifier.

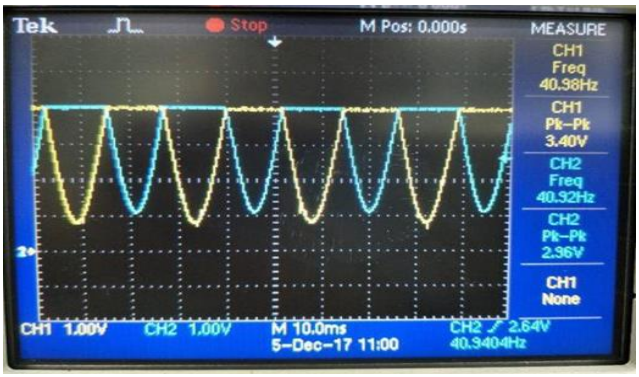

Figure 10. Inverting half-sine wave output

At this instant, the signals are ready to use in the TL494. Using Equation 1, the switching frequency is programmed to be at 40 kHz with selection of R_{24} equal to 25k Ω and C_{13} equal to 1000p F. Figure 11 shows the frequency and amplitude of the saw-tooth waveform generate. The output at the pull-down transistor were the inverse as expected. The duty cycles were precise, but where we expected a logic 1, there was a logic 0. Therefore. To overcome this issue, the voltage in half at the TL494 collectors is divided to make the output compatible with 74-series logic gate inverters. The signal at the TL494 collector would be suitable to drive the low-side gates on our MOSFET H-bridge, with the inverted signal driving the high-side gates.

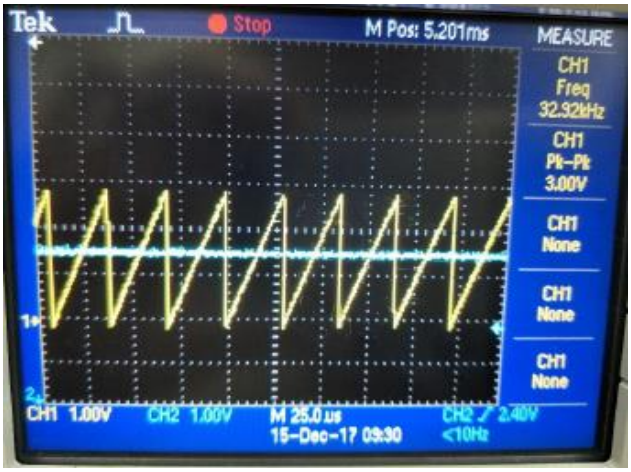

Figure 11. Frequency and Amplitude of Saw-Tooth Waveform

As shown in Figure 12, by comparing the input (inverse sine waveform) with the saw-tooth waveform, PWM signal is produced. Figure 13 shows the PWM signal produced after comparing step as mention in Figure 12. This PWM signal will be fed into both low side gate of cascade H-bridge MOSFET configuration.

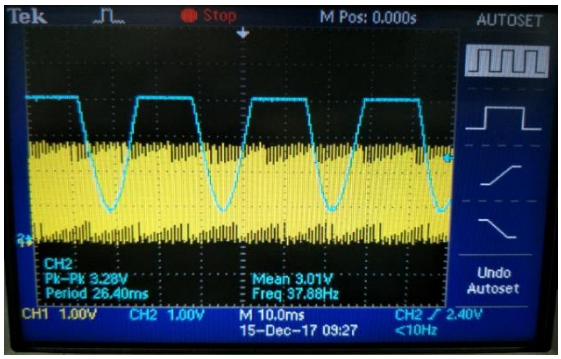

Figure 12. Comparison between saw-tooth waveform and inverting half-sine wave

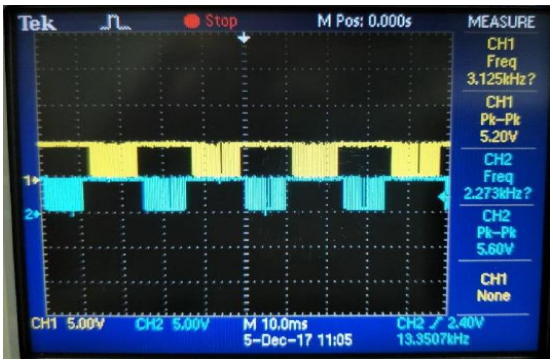

Figure 13. PWM Signal from TL494 for both low-side gate

For both high side gate half-cycles, an alternating PWM signal as shown in Figure 14 is applied. After then PWM was successfully generated, now these PWM signal in fetch into the three-level cascaded H-bridge MLI topology to test whether this PWM signal suitable in term of switching the IR 2304 MOSFET half bridge driver. For this prototype, two half bridge drivers is used as shown in Figure 6.

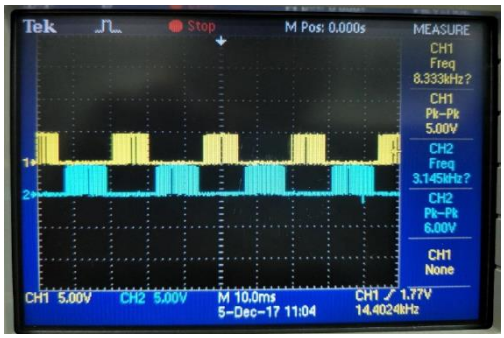

Figure 14. PWM signal from TL494 for both high-side gate

The bootstrap capacitor was added and connected between the pin 6 and pin 8 of the MOSFET driver. The function of bootstrap capacitor is to activate the high-side of the H-bridge inverter. Normally, the gate voltage of the MOSFET required a high voltage and more than input voltage supply. For the condition of high-side of H-bridge inverter, the voltage supply should connect with MOSFET power semiconductor before connecting with load. Due to very low resistance of MOSFET driver, the load voltage is very high and almost equal to voltage supply. So, the gate-source voltage is larger than the threshold voltage of the MOSFET and the source voltage. The source voltage is equal to load voltage and the gate-source voltage is gate voltage minus the source voltage. From these statements, the gate voltage is equal to source voltage plus the threshold voltage, so, the bootstrap capacitor is used in order to solve this problem. Firstly, the bootstrap capacitor charges from V_{cc} through diode when the lower MOSFET power semiconductor is turn on and the upper MOSFET power semiconductor is turn off. The function of diode is to prevent the capacitor from discharging into V_{cc}. When upper MOSFET power semiconductor is turn on, the bootstrap capacitor will undergo discharging process and this process will cause gate voltage goes up to overcome the effect of high-side of the H-bridge inverter.

The fabricated prototype has been testing for low-voltage testing mechanism. The low-voltage testing was conducted using the 12 V_{DC} lead acid battery both as the V_{CC} regulator source and as the H-bridge DC rail. As such, the output was a 12 V PWM signal, which was filtered and used to power up a 12V halogen bulb. Testing at low-voltage allowed us to safely test our setup and perform basic troubleshooting before moving on to high voltage. Figure 15 shows the output of H-bridge inverter. Channel 1 shows output voltage for the high gate of the half-bridge. Some distortion can be seen, but the waveforms otherwise look as they should. This distortion was complemented by severe overheating of MOSFETs and caused quite a bit of trouble until it was figured out.

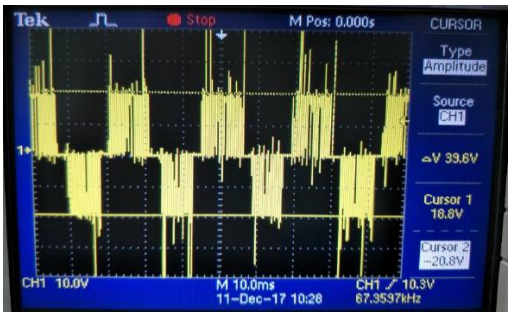

Figure 15. Output of three level H-bridge inverter

During low-voltage testing mechanism, the voltage and current are recorded as shown in Table 1. Figure 16 shows the output voltage waveform across the 12 V halogen bulb without capacitor filter. With the capacitor removed, the previous distortion also gone, though the voltage still slopes to some degree at both positive and negative cycle. The sine output was enough with the filter and that the output without the filter was essentially the same as before, but with the distortion gone, can be taken to mean that output would be ideal if we had the filter.

Table 1. Recorded data during low voltage testing mechanism

Measured Voltage	Measured Current	Output Power
18.8 V	3.69 A	70 W

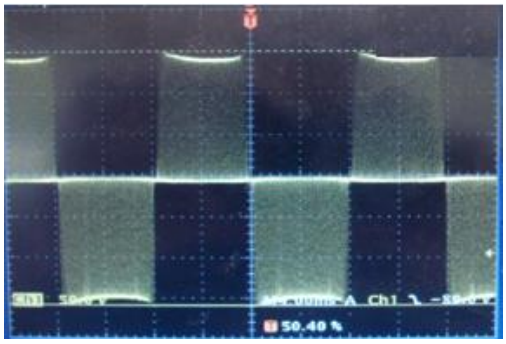

Figure 16. Output voltage waveform across halogen bulb

Table 2 shows the outcome of the three level H-bridge inverter when the system is fed from 20 V power supply. The value of measured resistance is 0.015 Ω that cause voltage drop around 0.043 V. Based on the result obtained, the power for designed inverter is around 100W and efficiency recorded at 75%. Figure 17 below shows the FFT for the output voltage waveform, performed actively by the oscilloscope. The large peak, which is all the way to the left in this image, is the 45Hz sine wave fundamental frequency. This primary frequency which will be retained by filter and go through to the load.

Table 2. Three level H-bridge inverter at 20V DC power supply

Measured Voltage	Measured Current	Output Power
22.5 V	4.5 A	100 W

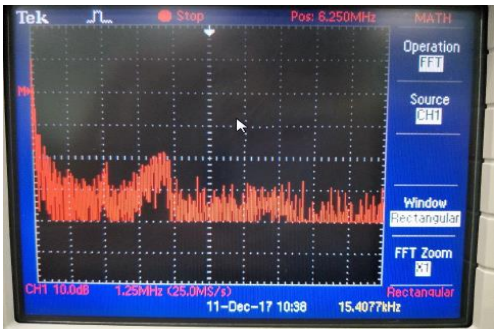

Figure 17. Output voltage FFT

4. CONCLUSION

For further improvements, to improve total harmonic distortion and improve output power efficiency, at least three improvements can be done. Firstly, the filter circuit such as RC filter, RL filter or LC filter should be constructed in the load because the harmonic contents will be filtered out or attenuated. Secondly, the switching frequency can be increased over than 40 kHz because the switching frequency can minimize the harmonic contents. So, the higher the switching frequency, the lower the harmonic contents of the 3-level output waveform. This increasing switching frequency will also decrease the filter component size. Finally, a high-level of the H-bridge multilevel inverter will reduce more the THD of the output waveform compare to the low-level of the H-bridge multilevel inverter. For example, 5-level H-bridge multilevel inverter will bring with high efficiency, low distortion and easier filter. So, a 5-level H-bridge multilevel inverter is very interested to be pursued in the future.

ACKNOWLEDGEMENTS

The authors would like to thank Fakulti Teknologi Kejuruteraan UTeM and Universiti Teknikal Malaysia Melaka for sponsoring this work under the short-term grant, UTeM, P PJP/2018/FTK (11A)/S01612.

REFERENCES

[1] P. V. Kumar, *et al.*,"Single Phase Cascaded Multilevel Inverter Using Multicarrier PWM Technique." *ARPN Journal of Engineering and Applied Sciences*, vol. 8, no. 10, pp. 796-799, 2013.
[2] P. P. Rajeevan, *et al.*, "A Seven-Level Inverter Topology for Induction Motor Drive Using Two-Level Inverters and Floating Capacitor Fed H-bridges," *IEEE Transactions on Power Electronics*, vol. 26, no. 6, pp. 1733–1740, 2011.
[3] W. A. Halim, et al., "Review of Multilevel Inverter Topologies and Its Applications." *Journal of Telecommunication, Electronic and Computer Engineering (JTEC)*, vol. 8, no. 7, pp. 51-56, 2017.
[4] A. Namboodiri and H. S. Wani, "Unipolar and Bipolar PWM Inverter." *International Journal for Innovative Research in Science & Technology (IJIRST)*, vol. 1, no. 7, pp. 237-243, 2014.
[5] L. M. Tolbert, *et al.* "Multilevel Converters for Large Electric Drives", *IEEE Trans. Ind. Electron*, vol.35, pp.36-44, 1999.
[6] M.K. Kumar, *et al.*, "Cascaded Multilevel Inverter with PWM Control Method." *International Journal of Engineering Trends and Technology (IJETT)*, vol. 4, no. 5, pp.1491-1496. 2013.
[7] V. M. Reddy, *et al.*, "Comprehensive Review on Single-Phase Five-level Inverter Topologies" *International Journal of Engineering Research & Technology (IJERT)*, vol. 4, no. 6, pp. 211-216, 2015.
[8] D. Subramanian and R. Rasheed, 2013. "Five Level Cascaded H-bridge Multilevel Inverter Using Multicarrier Pulse Width Modulation Technique." *International Journal of Engineering and Innovative Technology (IJEIT)*, vol. 3, no. 1, pp. 438-441.
[9] P. Iraianbu and M. Sivajumar, "A Single DC Source Based Cascaded H-bridge 5 Level Inverter." *International Journal of Innovative Research in Science, Engineering and Technology*, vol. 3, no. 1, pp. 995-1000, 2014.
[10] T. Singaravelu, *et al.*, "Design and Implementation of Seven Level Cascaded H-bridge Inverter Using Low frequency transformer with Single DC Source," *International Journal of Engineering and Technology (IJET)*. vol. 5, no. 3, pp. 3068-3076. 2013

BIOGRAPHIES OF AUTHORS

ASR ASubki obtained his MSc in Microelectronics from Universiti Kebangsaan Malaysia in 2011. He has 2 years of working experience as Photolithography and Wet Etcing Process Engineer at ON Semicondcutor Malaysia and as Process Integration Engineer at SilTerra Malaysia focusing on maintaining process parameters for CMOS 0.16 nm technology, before joining Universiti Teknikal Malaysia Melaka (UTeM) as lecturer and researcher, in Electronics and Computer Engineering. His research interests include CMOS process flow optimization and characterization and power electronic.

Mohd Zaidi Mohd Tumari is received his first degree in B.Eng. Electrical Mechatronics in 2008 from University of Technology Malaysia (UTM) in Johor, Malaysia and in 2010, he received a Master's degree in M.Eng. Mechatronics and Automatic Control from University of Technology Malaysia (UTM). He has an experience as a research assistant at Robotic Laboratory in University of Technology Malaysia (UTM) in 2008, Tutor in Universiti Pendidikan Sultan Idris (2008-2011) and Lecturer in Universiti Malaysia Pahang (2011-2014). As an academician and researcher, he has involved in many research and development in field of mechatronics, control and robotics. Currently, he is a Lecturer in Faculty of Engineering Technology, Universiti Teknikal Malaysia Melaka (UTeM). His current research interests are vibration and sway control, input shaping, crane system, liquid slosh system and flexible robot manipulator.

Wan Norhisyam Abd Rashid obtained his MEng in Uthm in 2014. He has 3 years of working experience in Infineon Technologies Sdn Bhd, before joining Universiti Teknikal Malaysia Melaka (UTeM) as lecturer and researcher, in Electronics and Computer Engineering. His research interests include tomography and embedded system design.