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Comparative High-K material gate spacer impact in DG-FinFET parameter variations between two structures

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ABSTRACT

This paper investigates the impact of the high-K material gate spacer on short channel effects (SCEs) for the 16 nm double-gate FinFET (DG-FinFET), where depletion-layer widths of the source-drain corresponds to the channel length. Virtual fabrication process along with design modification throughout the study and its electrical characterization is implemented and significant improvement is shown towards the altered structure design whereby in terms of the ratio of drive current against the leakage current (ION/IOFF ratio), all three materials tested being S3N4, HfO2 and TiO2 increases from the respective 60.90, 80.70 and 84.77 to 84.77, 91.54 and 92.69. That being said, the incremental in ratio has satisfied the incremental on the drive current as well as decreases the leakage current. Threshold voltage (VTH) for all dielectric materials have also satisfy the minimum requirement predicted by the International Technology Roadmap Semiconductor (ITRS) 2013 for which is at 0.461±12.7% V. Based on the results obtained, the high-K materials have shown a significant improvement, specifically after the modifications towards the Source/Drain. Compared to the initial design made, TiO2 has improved by 12.94% after the alteration made in terms of the overall ION and IOFF performances through the ION/IOFF ratio value obtained, as well as meeting the required value for VTH obtained at 0.464V. The ION from high-K materials has proved to meet the minimum requirement by ITRS 2013 for low performance Multi-Gate technology.

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1. INTRODUCTION

The size of integrated devices reduces day by day with higher demand in multiple operations and therefore, causing size of MOSFETs which is the main component in memory and processors to be scaled down [1]. On top of that, Moore's Law scaling prediction suppression can be done through the proposed new semiconductor devices and applications [2]. The reduction to nanometer regime has triggered the short channel effects to arise which degrades the system performance and reliability. Therefore, a fin-shaped field effect transistor (FinFET) of 16nm technology is designed along with the performance of the transistor that is improved in relation to the Moore's Law [3]. The devices performance may have been degraded via scaling process for the transistor miniaturization. Meaning that, the key device parameters of a transistor can be affected due to the channel length reduction in nanometer regime for instance the carrier mobility and transconductance. Besides that, by comparison, Multi-gate FET (MGFET) shows better drain potential

screening as opposed to the conventional planar MOSFET and therefore, improving in short channel performance in drain-induced barrier lowering (DIBL), V_{TH} roll-off, and also sub-threshold swing (SS) and therefore consequently reducing the V_{TH} degradation with continuous scaling and in turn effecting the I_{OFF} degradation to be minimized [4]. The SCEs has affected the device and the performance of the circuit in electron drift characteristics limitation within the channel, besides the reconstruction of the threshold voltage. Therefore, the gate oxide thickness and the gate-controlled junction or depletion depth in the silicon have to be reduce in proportion to L (Gate Length) [5]. Accordingly, alternative structure such as Double Gate FinFET (DG-FinFET) is believed to have solved the scaling problems especially on the device short channel performance and scalability of nanoscale. Several experiments of designing FinFET Double-Gate MOSFET device is carried out after the initial fabrication simulation by altering several input process parameters.

In this research, the traditional polysilicon/SiO_2 material will be replaced by the metal gate/high-k dielectrics in order to increase the I_{ON} for which a recent work done by Rahul et. al. 2012 has shown that the I_{ON} of vertical double-gate MOSFET can be further improved by replacing poly-Si/SiO_2 with the metal-gate/high-k stack technology [6]. The results from Rahul et. al. showed that the I_{ON} was successfully improved from 720 μA/μm up to 1772 μA/μm. Besides, in other research the hafnium dioxide (HfO_2) and nickel have been utilized as a high-k dielectric and metal-gate correspondingly [7]. Mostly, a significant amount of work has been published on the prediction of leakage current and leakage power by various researchers [8-12].

Appropriate statistical analysis techniques have been implemented to apply the input process parameter optimization from data collected. In fabricating a proper Double-Gate FinFET device, each steps of fabrication and its order have been prioritized. Other than that, in obtaining the desired V_{TH} level, I_{ON}, I_{OFF}, and SS, several FinFET characteristics is studied. The data from the simulation will be used to determine the dominance of the process parameter effects on the device's characteristics. Parameters considered are improving the values of respective V_{TH}, I_{ON}, I_{OFF} that are based on the minimum requirement standardized by International Technology Roadmap Semiconductor (ITRS) 2013 prediction for low power (LP) multi-gate technology for the year 2020.

2. MATERIALS AND METHOD

2.1. Virtual Fabrication Process

In this study, ATHENA and ATLAS modules from Silvaco International is used to simulate the fabrication process of DG-FinFET device. Each ATHENA and ATLAS is implemented for process simulation and device simulation specifically in electrical characterization respectively, of intended FinFET device. That being said, five geometrical parameters have been identified and are observed to cause variation impact on FinFET. Output responses variation are due to the process parameter fluctuations through local parameters variations that are 30% from the overall variation based on the research conducted by Kaharudin et. al (2014) [13]. The value of parameters identified are changed and varied in order to fulfil the minimum values required as shown in Table 1.

Table 1. Value of the Geometrical Parameters Set

No	Parameters	ITRS Value	Set Value
1	Gate Length, L_g	20 nm	16 nm
2	Oxide Thickness, T_{OX}	2.42 n	2.4 nm
3	Fin width, T_{fin}	6.4 nm	28 nm
4	S/D length	N/A	8.45 nm
5	S/D underlap	N/A	6.25 nm

The physical structure of the nano-scaled device is gained through simulation utilized with Silvaco TCAD. The <100> of orientation is utilized as a part of this current outline's main substrate which is a P-type silicon along with an oxide layer developed on the silicon bulk's top acting as a mask in P-well implantation process. This is trailed by an infusion of $1x10^{17}$ atom/cm^3 of Boron into the silicon substrate. Since the gate terminal can be isolated from source and drain terminal away from its conductive channel through a dielectric layer, gate oxide is developed at 875^{o}C in dry oxygen condition in 3% HCL at 1 atmospheric pressure. The threshold voltage alteration implantation is actualized in channel region through an approximate $1.95x10^{13}$ atom/cm^3 of Boron at 5 keV of energy. Huge changes can be analysed as slight changes being made towards the gate concentration and hence making it appropriate to be contemplated as one of the parameter variations before the ones with hugest changes are selected. Polycrystalline silicon is then deposited on the semiconductor wafer as multi-layered structure is shaped through conformal polysilicon deposition.

Meanwhile, as p-type impurities particle is implanted in the substrate that permits the development of the n-type Source/Drain areas, indium is then doped with $1.17x10^{13}$ atom/cm^3 of measurements with 1 keV of energy implanted in the halo implantation for which can lessen the SCE. The layer of nitride Si_3N_4 is produced on the surface of the silicon and polysilicon in sidewall spacer production. $1.22x10^{18}$ atom/cm^3 of arsenic dose with implant energy of 3 keV is implanted to perform Source/Drain implantation before the side capacitance is minimized through compensate implantation. The first formation of the contact window in the Source/Drain region alongside aluminium deposition and patterning has permitted the metallization procedure to be performed before structure mirroring procedure and electrode definition is made as in Figure 1.

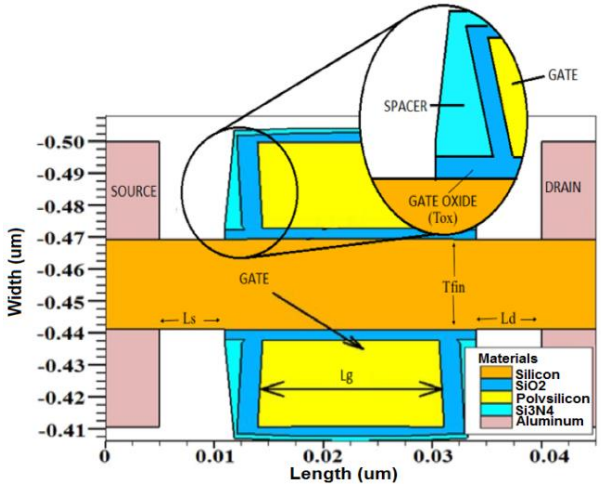

Figure 1. FinFET structure S_3N_4 gate spacer

By using device simulation, electrical characteristics of parameters, namely V_{TH}, I_{OFF}, I_{ON} and SS can be extracted. Based on the parameters identified, in addition to the application of geometrical parameters, for which is by adjusting the parameters to change the structure of the device, the optimization process has been done by changing the values of the parameter that is identified, throughout the experiment to fulfil the experiment criteria.

The values set for the electrical characteristics are also followed based on the ITRS values set whereby the V_{TH} are predicted to be within 12.7% from the ideal 0.461V, with I_{OFF} less than 10pA/µm. The respective I_{ON} and SS meanwhile are supposed to meet at higher than 574µA/µm and in between 70 - 90 mV/decade. The device performance has been analyzed in term of V_{TH}, I_{OFF}, I_{ON} and SS and ratio of I_{ON}/I_{OFF} by performing variation on gate length, channel doping and S/D doping concentration where a curve of Drain Current (µA/µm), I_D against Gate Voltage (V), V_{GS} is generated by ATLAS module as in Figure 2.

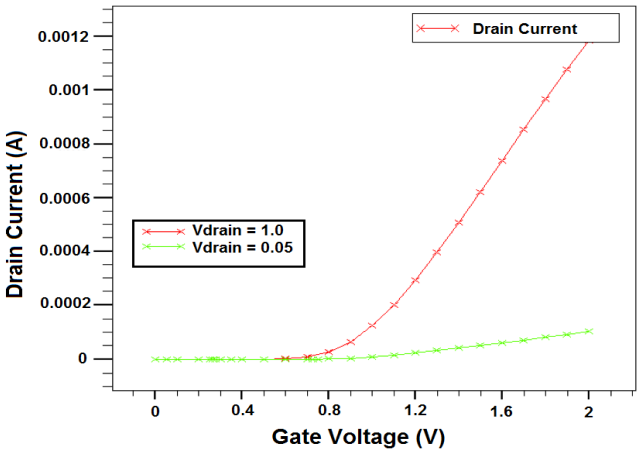

Figure 2. Drain current (A), I_D against gate voltage (V), V_{GS} curve for S_3N_4 spacer gate DG-FinFET from ATLAS module

The I_D-V_G curves obtained in Figure 2 are then extracted by the ATLAS to acquire the respective V_{TH}, I_{ON}, I_{OFF} and SS and thus the values obtained from the simulations are as in Table 2.

Table 2. Value of Electrical Characteristics using S_3N_4

No	Parameters	ITRS Value	Set Value
1	Threshold Voltage (V), V_{TH}	0.461±12.7%	0.461
2	Leakage Current (pA/µm), I_{OFF}	<20	19.09
3	Drive Current (µA/µm), I_{ON}	>574	1162.60
4	Subthreshold Voltage (mV/dec), SS	70-90	88.70

Hafnium Dioxide (HfO_2) and Titanium Dioxide (TiO_2) has been used as dielectric materials in addition to the Si_3N_4 in the construction of 16 nm DG-FinFET. The related dielectric constant values including the high-k materials for the corresponding various dielectric materials are as in Table 3.

Table 3. Dielectric Constant Values for S_3N_4, HfO_2 and TiO_2

No	Dielectric Materials	Dielectric Constant (KeV)
1	S_3N_4	9.5
2	TiO_2	85
3	HfO_2	25

Based on the results obtained from the Si_3N_4 as in Table 2, the following materials in HfO_2 and TiO_2 are then used to compare its electrical characteristics consisting the V_{TH}, I_{OFF}, I_{ON} and SS as shown in Table 4 [14].

Table 4. Value of Electrical Characteristics for S_3N_4, HfO_2 and TiO_2 Gate Spacer

No	Parameters	S_3N_4	TiO_2	HfO_2
1	Threshold Voltage (V), V_{TH}	0.46	0.461	0.461
2	Leakage Current (pA/µm), I_{OFF}	19.09	5.34	5.18
3	Drive Current (µA/µm), I_{ON}	1162.61	431.46	415.89
4	Subthreshold Voltage (mV/dec), SS	88.74	107.89	109.78

The I-V characteristics is known as the relationship between the electric current through a device and the corresponding voltage across it. The threshold voltage (V_{TH}), leakage current (I_{OFF}), drive current (I_{ON}) and the subthreshold voltage (SS) can be extracted from the curve of Drain Current (A) against Gate Voltage (V) as in Figure 2. Transistors should have a high drive current (I_{ON}) and a low threshold voltage (V_{TH}) to increase the switching speed of this transistor.

2.2. Structure Design Alteration

Based on a research conducted by Kumar et. al., the placement of the Source/Drain location to the sides which is in between the silicon substrate has been done for which has reduced the fin width (T_{fin}) closer to the ITRS prediction on the geometrical parameter value from 28 nm to 18 nm while being able to improve or at least retaining its value compared to the design fabricated in Figure 1 [15].

Initially, the dimension of the main substrate has been retained in its size with <100> orientation when the boron dose is implanted at $5.65x10^{13}$ atom/cm^3 before the polysilicon is etched 0.5 nm less than the dimension from the initial polysilicon structure. The fin width is then reduced to 18 nm through the etching process. Aluminium deposition process is then achieved by etching process applied to the silicon before the material is deposited. Structure mirroring and the electrode defining procedures follows as changes occurred in the Source and Drain positioning within the structure. The parameters used in the restructuring process are selected as in Table 5. The parameter values chosen has allowed an improvement in terms of meeting the required minimum values predicted by the ITRS compared to the initial structure as in Figure 1. The altered FinFET structure with S3N4 gate spacer shows in Figure 3.

Table 5. Value of the Geometrical Parameters Set

No	Parameters	ITRS Value	Set Value
1	Gate Length, L_g	16 nm	16 nm
2	Oxide Thickness, T_{OX}	2.4 nm	2.4 nm
3	Fin width, T_{fin}	28 nm	18 nm
4	Extension length to source/drain (L_s & L_d)	45 nm	35 nm

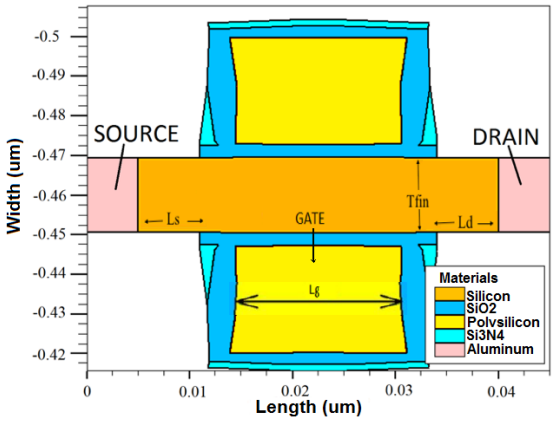

Figure 3. The altered FinFET structure with S_3N_4 gate spacer

Through the design modification, the V_{TH} values for the altered structure in comparisons with the initial design structure are shown to have obtained within ±12.7% from the targeted 0.461 V. Based on Table 6, comparatively the newly altered structure both have acquired the respective 0.464 V and 0.465 V which has met the prediction set by the ITRS 2013.

Table 6. Value of Electrical Characteristics for S_3N_4, HfO_2 and TiO_2 Gate Spacer based on Altered Structure

No	Parameters	S_3N_4	TiO_2	HfO_2
1	Threshold Voltage (V), V_{TH}	0.464	0.464	0.465
2	Leakage Current (pA/µm), I_{OFF}	18.99	17.89	17.8625
3	Drive Current (µA/µm), I_{ON}	1189.4	1658.03	1635.07
4	Subthreshold Voltage (mV/dec), SS	118.9	117.69	118.17

Based on the results obtained, it is observed that HfO_2 has its drawback in its crystallization temperature; for which is low despite its low leakage current property.

3. RESULTS AND DISCUSSION

This paper uses the High-K dielectric material from Hafnium Oxide (HfO_2) and Titanium Oxide (TiO_2) as the gate oxide in 16nm Double Gate FinFET structure. All the devices are set to the same level of VTH during the simulation which was 0.461±12.7% V as predicted by ITRS 2013 for low power (LP) multi-gate technology in the year 2017. This is done to precisely evaluate the performance in terms of the corresponding I_{ON}, I_{OFF}, I_{ON}/I_{OFF} ratio, and SS of the aforementioned devices. The FinFET structures spacers is studied by implementing different materials such as Silicon Nitride (Si_3N_4), HfO_2 and TiO_2 having dielectric constants 7 keV, 25 keV and 85 keV respectively due to its high K dielectric properties. The analysis of the results revealed that the TiO_2 device has superior electrical characteristics compared to others as listed in Table 7.

Table 7. Comparisons in Value of Electrical Characteristics for S_3N_4, HfO_2 and TiO_2 of Gate Spacer based on the Initial and Altered Device Structure

Device		V_{TH} (V)	I_{ON} (µA/µm)	I_{OFF} (pA/µm)	I_{ON}/I_{OFF} Ratio	SS (mV/ dec)
S_3N_4	Initial	0.461	1162.6	19.09	60.9	88.7
	Altered	0.464	1609.7	18.99	84.8	118.9
TiO_2	Initial	0.461	431.5	5.35	80.7	107.9
	Altered	0.464	1658.0	17.89	92.7	117.7
HfO_2	Initial	0.461	415.9	5.18	80.3	109.8
	Altered	0.465	1635.1	17.86	91.5	118.2
ITRS 2013		0.461 ±12.7%	>574	<10	57.4	70-90

At the end, based on the results in Table 7, the alteration made towards the structure has allowed the FinFET's threshold voltage (V_{TH}) to have vastly improved in terms of meeting the minimum requirement predicted. Subsequently, while the drive current, I_{ON} for the S_3N_4 is has met the target of the ITRS 2013, which is larger than 574 µA, it increases from 1162.6 µA/µm to 1609.7 µA/µm after the alteration is made. Meanwhile, the I_{ON} for the TiO_2 and HfO_2 for which previously have not met the prediction values, have significantly improved after the modification is made towards the structure from 431.5µA/µm and 415.9 µA/µm into 1658.0 µA/µm and 1635.1 µA/µm respectively. However, the I_{OFF} value does not meet the minimum value predicted which is lower than 10 pA after the structure alteration, for which does bring the value closer to the predicted values. Despite that, ideally the device with a higher I_{ON}/I_{OFF} ratio after the alteration is made towards the structure for which means that the device has met a superlative value due to incremental of I_{ON} against the decreasing of I_{OFF}, that is corresponding to the prediction made by the ITRS 2013 and therefore, through Table 7 it is analysed that the alteration towards the structure has bring the ratio much greater in comparison to the ideal ratio of 57.4 targeted throughout various dielectric material gate spacer.

4. CONCLUSION

In conclusion, based on simulation done, the double gate FinFET have established good electrical properties such as high drive current and low leakage current based on the electrical characteristic analysed. Comparatively, improvement has been resulted by the alterations towards the device structure. The application of the high-k materials has also enhanced the increment in its drive current (I_{ON}) despite a slight increment in its leakage current (I_{OFF}). That being said, the TiO_2 meanwhile has resulting in improvement of the device due to high in current drive which is used to decide on the drive capability of FinFET device as well as the material's low leakage current properties. Besides that, the device characteristics have met the requirement of low performance (LP) multi-gate (MG) technology predicted by ITRS 2013 for the year 2017 requirements.

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