Bulletin of Electrical Engineering and Informatics
Vol. 8, No. 4, December 2019, pp. 1268~1278
ISSN: 2302-9285, DOI: 10.11591/eei.v8i4.1615

Performance analysis of ultrathin junctionless double gate vertical MOSFETs

K. E. Kaharudin, Z. A. F. M. Napiah, F. Salehuddin, A. S. M. Zain, Ameer F. Roslan
MiNE, Centre for Telecommunication Research and Innovation, Faculty of Electronics and Computer Engineering, Universiti Teknikal Malaysia Melaka (UTeM), Hang Tuah Jaya, Durian Tunggal, 76100 Melaka, Malaysia

Article Info

Article history:

Received Mar 29, 2019
Revised May 24, 2019
Accepted May 30, 2019

Keywords:

Channel length
I_{ON}/I_{OFF} ratio
Off-state current
On-state current
Subthreshold slope

ABSTRACT

The main challenge in MOSFET minituarization is to form an ultra-shallow source/drain (S/D) junction with high doping concentration gradient, which requires an intricate S/D and channel engineering. Junctionless MOSFET configuration is an alternative solution for this issue as the junction and doping gradients is totally eliminated. A process simulation has been developed to investigate the impact of junctionless configuration on the double-gate vertical MOSFET. The result proves that the performance of junctionless double-gate vertical MOSFETs (JLDGVM) are superior to the conventional junctioned double-gate vertical MOSFETs (JDGVM). The results reveal that the drain current (I_D) of the n-JLVDGM and p-JLVDGM could be tremendously enhanced by 57% and 60% respectively as the junctionless configuration was applied to the double-gate vertical MOSFET. In addition, junctionless devices also exhibit larger I_{ON}/I_{OFF} ratio and smaller subthreshold slope compared to the junction devices, implying that the junctionless devices have better power consumption and faster switching capability.

Corresponding Author:

F. Salehuddin,
Centre for Telecommunication Research and Innovation,
Faculty of Electronics and Computer Engineering,
Universiti Teknikal Malaysia Melaka (UTeM),
Hang Tuah Jaya, Durian Tunggal, 76100 Melaka, Malaysia.
Email: fauziyah@utem.edu.my

1. INTRODUCTION

Aggressive scaling of conventional MOSFET leads to several short channel effect (SCE) as the channel length (L_{ch}) is reduced. Multiple MOSFETs architectures have been introduced [1-5] to realize the Moore's law prediction in producing ultra-small transistors while maintaining excellent electrical performance. As the transistor size is continuously scaled down, the formation of extremely intricate junctions between source/drain and channel regions offers a real challenge to chip designers. But still, an ultrathin and narrow body configuration is believed to be a significant alternative for extreme MOSFET scaling. The double-gate vertical MOSFET is one the MOSFET configurations that offers the maximum control of the electrostatic field in the channel region by the two side gates. The reduction of L_{ch} and pillar (body) thickness could further improve the controllability of both gates upon the electrostatic potential in the ultrathin channel [6]. As a result, the channel experiences lesser electrical interference between the source and drain region that subsequently leads to the improvement of on-state current (I_{ON}), leakage current (I_{OFF}) and subthreshold slope (SS). The double-gate vertical MOSFET, though having better immunity to SCE, are yet far from perfect and encounter similar challenges like conventional bulk MOSFET. For instance, the requirement of new doping approaches, advanced source/drain and channel engineering are required to form ultrashallow source/drain (S/D) junctions with high doping gradient [7].

Recently, a lot of junctionless [8-13] MOSFET configurations have been proposed to eliminate the adversity arisen from ultrashallow junction formation. The key feature of junctionless MOSFET configuration is to eliminate the presence of junction between the source/drain and channel region where both regions are doped with the same polarity dopant, either n-type or p-type material. The junctionless configuration absolutely neglects the adversity of having high doping gradient, hence considerably diminishing the complicated fabrication process. Therefore, the working principle of junctionless transistors is based on depletion-mode and it heavily relies on the geometrical design, process parameters and work function (WF) engineering.

Numerous research groups are working on studying, analyzing and optimizing multiple types of junctionless transistor in order to improve the electrical performances as well as the fabrication cost. Colinge *et al.* (2009) [14] are the first researcher groups that discovered and studied the fundamental and physical properties in junctionless transistor. They found that the N+ and P+ silicon-on-insulator (SOI) based nanoribbon are less sensitive to thermal budget issue than conventional MOSFET since they contained no junction and no doping gradients [15]. The simple process fabrication with excellent subthreshold slope and drain induced barrier lowering (DIBL) are the main advantages of the junctionless device. Akram *et al.* (2014) [16] have investigated the impact of multiple parameter variations on the device characteristics in 20 nm p-type double-gate junctionless tunnel field transistor (p-DGJLTFET). It is observed that the optimized parameters along with the utilization of high-*k* dielectric material (TiO_2) of 20 nm gate length yields excellent device characteristics with I_{ON}~0.3 mA/µm, a low I_{OFF} of ~30 fA/µm, a high I_{ON}/I_{OFF} ratio of ~$1x10^{10}$, a subthreshold slope (SS) point of ~49 mV/decade at a supply voltage of –1 V and at room temperature. Lakshmi and Srinivasan (2015) [6] have studied the influence of process variations on unity cut-off frequency (f_t) in both conventional and junctionless gate-all-around (GAA) transistors via TCAD simulation. The results show that the f_t was more sensitive to gate length and S/D doping, less sensitive to gate oxide thickness, ovality and channel doping and least sensitive to gate work function (WF) variations. Riyadi et al. (2016) [17] have investigated the impact of gate material and process on subthreshold performance of junctionless FET (JLFET), by comparing four sets of gate material and process techniques. Based on the results, it was observed that the V_{TH} value for all JLFET types heavily depended on the channel doping concentration as well as the WF. The SS value for JLFETs was generally lower than SOI based device, with the slope which was closed to ideal value of 60mV/decade. This is mainly due to the bulk transport mechanism in which the conducting channel is fully accupied by the majority carriers, in contrast to the surface conduction experienced in conventional MOSFET and SOI FET.

Archana *et al.* (2017) [18] have derived the analytical modeling of junctionless surrounding gate MOSFET based on existing model. Based on the derived model, multiple characteristics and behavior of the device such as surface potential, V_{TH}, SS were plotted against channel length, radius and doping concentration. The result revealed that the V_{TH} rolls off as the channel doping concentration was increased. In addition, the variation of V_{TH} and SS were explicitly noticed when the channel length was scaled down below 20 nm. This clearly indicates that the junctionless device is significantly related to process and geometrical parameters as it shrinks into nano scale regime. The study of structural and geometrical variability on the performance jumctionless transistors have also been conducted recently by khorramrouz *et al.* (2018) and Ambika and Srinivasan *et al.* (2018) [19, 20]. Based on their observation, the structural and geometrical parameters such as thickness of silicon, thickness of insulator, channel length and etc. did contribute significant changes in the electrostatic and analog performance of the devices. Carrillo-Nunez *et al.* (2018) in their report [21] have investigated the effect of channel length variation on the junctionless silicon nanowire transistor. Based on the results, the reduction of the channel length slightly deteriorated the device performance in term of on-state and off-state current due to weakened electrostatic control. The variation of structural and geometrical parameters does not only affect the DC performance but also defining the RF characteristics of the junctionless device [22-25]. Based on the aforementioned literatures, junctionless configuration is definitely one of the alternative device configurations that allow the continuity of transistor scaling with minimal degradation of electrical performances. Several focal research areas can be drawn from the previous literatures such as the impact of geometrical design, process variations and high-k/metal-gate application on the transistor performance [26-30]. This paper will focus on the performance analysis of ultrathin Junctionless Double Gate Vertical MOSFETs (JLDGVM) by comparing their electrical characteristics with the Junctioned Double Gate Vertical MOSFETs (JDGVM).

2. METHODOLOGY

This section will describe about numerical models used to attain simulation solutions via Silvaco TCAD tools. Then, the 2D process simulation for ultra-thin JLDGVMs is conducted via Athena module as the process flow of the device is presented in Figure 1. The process simulation consists of the ultrathin

pillar formation, the high-*k* metal-gate (HKMG) deposition, source/drain implantation and metallization. The device simulation is finally employed via Atlas module in order to extract the I_D-V_G characteristics.

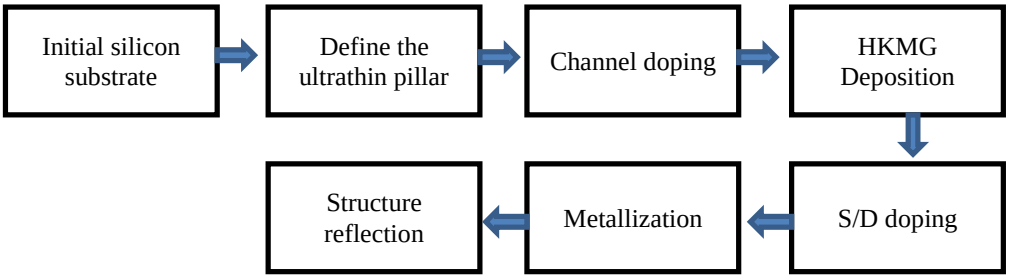

Figure 1. Simulated process flow for ultrathin JLDGVM design

2.1. Numerical models

The transport model is based on drift-disfussion model since it is suitable for designing the device with low power density specification. The drift-diffusion model is basically employed for carrier transport in semiconductors and is defined by the basic semiconductor equations. Current density for electrons and hole is given by (1) and (2):

$$J_n = -qn\mu_n \nabla \psi_n + qD_n \nabla_n \quad (1)$$

$$J_p = -qp\mu_p \nabla \psi_p + qD_p \nabla_p \quad (2)$$

The μ_n and μ_p stand for the electron and hole mobilities, where as φ_n and φ_p stand for the electron and hole quasi-Fermi potentials respectively. The q and D are used to indicate the absolute value of the electronic charge and diffusion coefficient correspondingly. The three main equations for carrier transport in the semiconductor devices are known as Poisson equation, the electron and hole continuity equations. The poisson equation is denoted as:

$$-\nabla^2 \psi = \frac{q}{\varepsilon}\left(N_D - n + p - N_A\right) + \rho_{trap} \quad (3)$$

where ε is the electrical permittivity, n and p are the electron and hole densities, N_D is the donor ion concentration, N_A is the acceptor ion concentration, and ρ_{trap} the charge density contributed by traps and fixed charges. Continuity equations for electron and hole are denoted as:

$$\nabla . J_n = qR + q\frac{\partial_n}{\partial_t} \quad (4)$$

$$\nabla . J_p = qR + q\frac{\partial_p}{\partial_t} \quad (5)$$

where R represents the net recombination rate for electrons and holes. Modeling the carrier mobilities of the JLDGVM are subjected to surface scaterring extreme carrier-carrier scattering, and quantum mechanical size quantization effects. These effects need to be taken into account in order to execute the device simulation. Lombardi CVT model is opted to be employed in ATLAS module for accurate simulation of non-planar MOSFET like JLDGVM. In this model, the mobility parts consist of the transverse field, doping dependent and temperature dependent which are given by three combined components as follows:

$$\mu_T^{-1} = \mu_{AC}^{-1} + \mu_b^{-1} + \mu_{sr}^{-1} \quad (6)$$

where $\mu_{AC,}$ μ_b and μ_{sr} are the surface mobility limited by scattering with acoustic phonons, mobility limited by scattering the optical intervalley phonons and mobility limited by surface roughness respectively. The surface mobility of electron and hole are formulated by:

$$\mu_{AC,n} = \frac{BN.CVT}{E_{\perp}^{EN.CVT}} + \frac{CN.CVT.N^{TAUN.CVT}}{T_L E_{\perp}^{DN.CVT}} \quad (7)$$

$$\mu_{AC,p} = \frac{BP.CVT}{E_{\perp}^{EP.CVT}} + \frac{CN.CVT.N^{TAUN.CVT}}{T_L E_{\perp}^{DP.CVT}} \quad (8)$$

where BN.CVT, CN.CVT, DN.CVT, EN.CVT, TAUN are the default electron mobility parameters and BP.CVT, CP.CVT, DP.CVT, EP.CVT, TAUP are the default hole mobility parameters, which are preset by the Silvaco Atlas. The symbol $T_{L,}$ $E_{\perp}$ and N stand for the temperature, perpendicular component of electric field and total doping concentration, respectively.

The mobility model is combined with SRH (Shockley-Read-Hall Recombination) with fixed carrier lifetimes models. This recombination model is opted in order to take the phonon transitions effect into account due to the presence of a trap (or defect) within the forbidden gap of the devices. The numerical model of SRH recombination is shown as follows:

$$R_{SRH} = \frac{pn - n_{ie}^2}{TAUP0\left[n + n_{ie}\exp\left(\frac{ETRAP}{KT_L}\right)\right] + TAUN0\left[p + n_{ie}\exp\left(\frac{ETRAP}{KT_L}\right)\right]} \quad (9)$$

where ETRAP, T_L, n_{ie}, are the difference between trap energy level and the intrinsic Fermi level, intrinsic carrier concentration and lattice temperature in Kelvin, respectively. Meanwhile, TAUN0 and TAUP0 are the electron and hole lifetimes which are user definable in the material statement in Atlas module. This model will be activated as the SRH parameter of the model statements are defined in Atlas module.

2.2. Device simulation

The schematic structure of JLDGVM and JDGVM are illustrated in Figure 2. The structures of these devices are based on the ultrathin silicon pillar/body in order to operate in fully depleted mode. Both devices are designed based on the similar geometrical parameters in which the channel length (L_{ch}), pillar thickness (L_p) and hafnium dioxide (HfO_2) thickness are set to 11 nm, 9 nm and 3 nm respectively. All the detailed geometrical and process parameters ulitized for both devices are summarized in Table 1. In term of process parameters, the silicon substrate of n-channel JLDGVM is heavily doped with concentration of $1x10^{18}$ cm^{-3} of n-type dopant (Arsenic). On the other hand, the silicon substrate is heavily doped with the concentration of $1x10^{18}$ cm^{-3} of p-type dopant (boron) for p-channel JLVDGM. In constrast, JDGVM design utilizes the opposite dopant type where the silicon substrate is doped with the concentration of 1 x 10^{14} cm^{-3} of p-type dopant (boron) for n-channel device and with the concentration of 1 x 10^{14} cm^{-3} of n-type dopant (arsenic) for p-channel device. This is because the working principle of n-channel JDGVM and p-channel JDGVM are based on N-P-N (Inversion-mode) and P-N-P (Accumulation-mode) respectively.

Table 1. Parameters used in the simulated devices

Parameter	Units	JLDGVM		JDGVM	
		n-type	p-type	n-type	p-type
Channel Length, L_{ch}	nm	11	11	11	11
Pillar Thickness, L_p	nm	9	9	9	9
High-*k* material thickness, $T_{high\text{-}k}$	nm	3	3	3	3
Channel doping, N_{ch}	cm^{-3}	1.0E18	1.0E18	1.0E14	1.0E14
S/D doping, N_{sd}	cm^{-3}	1.0E18	1.0E20	1.0E18	1.0E14
Metal work-function, WF	eV	4.5	4.7	4.5	4.7

The source and drain regions of the JLDGVM are heavily doped with the same type of dopant used in the channel region where $1x10^{18}$ cm^{-3} concentration of n-type dopant (Arsenic) and $1x10^{20}$ cm^{-3}

concentration of p-type dopant (boron) are implanted for n-channel JLDGVM and p-channel JLDGVM, respectively. This is important in order to form the junctionless configurations that require an N+–N+–N+ (n-channel) and a P+–P+–P+ (p-channel) doped structure for the source, channel and drain region. The S/D doping for JDGVM is in contrast with the JLVDGM where 1 x 10^{18} cm^{-3} concentration of n-type dopant (Arsenic) and 1 x 10^{14} cm^{-3} concentration of p-type dopant (boron) are employed for n channel JDGVM and p channel JDGVM, accordingly. The physical high-*k* dielectric thickness ($T_{high\text{-}k}$) of 3 nm is considered for both JLDGVM and JDGVM devices in order to keep the equivalent oxide thickness (EOT) intact. The HfO_2 is a dielectric material applied for both devices as it has permitivity 4–6 times higher than that of silicon dioxide.

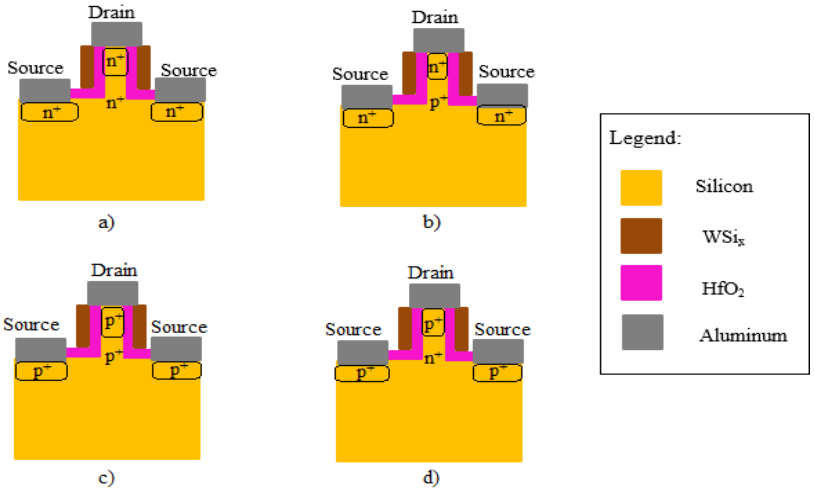

Figure 2. 2D structure of double-gate vertical MOSFETs, (a) n-JLDGVM (Junctionless), (b) n-JDGVM (Inversion-mode), (c) p-JLDGVM (Junctionless), (d) p-JDGVM (Accumulation mode)

Having a larger dielectric constant would enable thicker insulator to be used for leakage reduction while retaining fast reaction of the device. The presence of two metal gates (tungsten silicide) that wrap the ultrathin pillar would help in producing an accelerating force to drive the charge carrier into the channel, thus improving the on-current (I_{ON}) as well as suppressing the SCE. For both type of devices, the metal work functions of n-type and p-type device are taken as WF=4.5 eV and WF=4.7 eV, respectively. The doping profile across the JLDGVM device is shown in Figure 3 where the net doping for silicon, hafnium dioxide, tungsten silicide and aluminum has been clearly displayed.

The ATLAS module provides specific characteristics such as the I_D-V_G curve that enable the extraction of critical device characteristics such as threshold voltage (V_{TH}), drive current (I_{ON}), off-leakage current (I_{OFF}), I_{ON}/I_{OFF} ratio and subthreshold slope (SS). The device simulation condition [31] as shown in Table 2 is used to generate I_D-V_G transfer characteristics for DC characteristics extraction. All the investigated characteristics are extracted and computed from the generated I_D-V_G transfer characteristics. In the next section, the simulation results for JLDGVM and JDGVM devices were then analyzed, compared and further discussed.

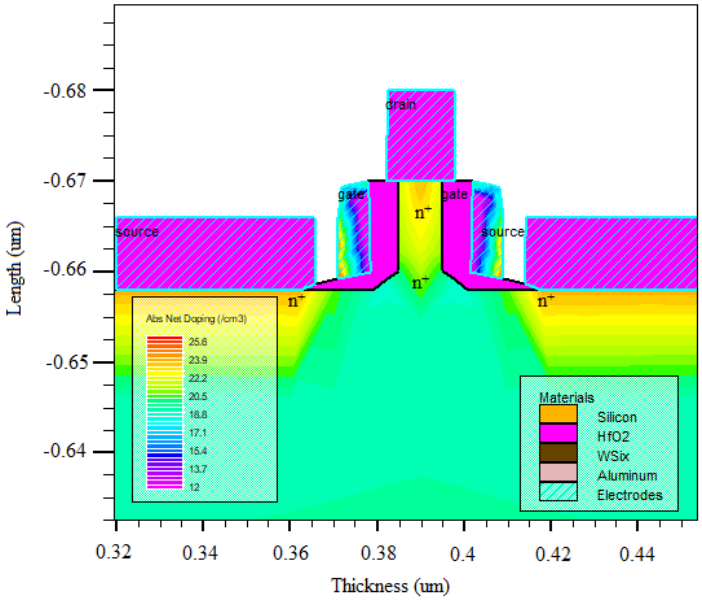

Figure 3. Contour Mode of n-JLDGVM layout

Table 2. Device simulation condition

Electrical Characteristics	Drain Voltage, V_D (V)	Gate Voltage, V_G (V)		
		$V_{Initial}$	V_{Step}	V_{Final}
Threshold Voltage (V_{TH})	1.0	0	0.1	2.0
On-state Current (I_{ON})	1.0	0	0.1	2.0
Off-state Current (I_{OFF})	1.0	0	0.1	2.0
Subthreshold Slope (SS)	1.0	0	0.1	2.0

3. RESULTS AND ANALYSIS

In this section, all the simulation results and its discussion are briefly described for both JLDGVM and JDGVM devices. In order to study and analyze the performance of JLDGVM and JDGVM devices, the V_{TH} values of both devices were tuned at 0.25 V. In other words, all the investigated characteristics were normalized to the fixed V_{TH} value for unbiased performance evaluation. The variation of I_D-V_G transfer characteristics of both JLDGVM and JDGVM devices, shifting the curves to the positive x-axis for n-channel and to the negative x-axis for p-channel is depicted in Figure 4.

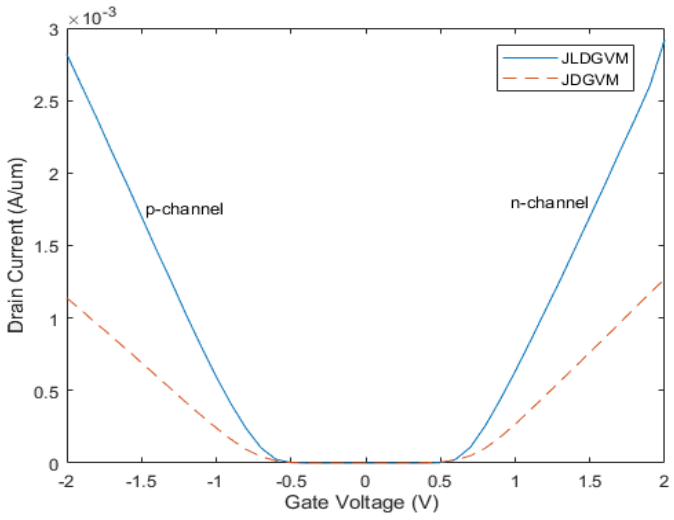

Figure 4. I_D-V_G transfer characteristics of both JLDGVM and JDGVM

Based on the graph, it is clearly shown that the I_D of both n- and p-channel JLDGVM were significantly larger than JDGVM. The I_D of the n-JLDGVM and p-JLDGVM could be tremendously enhanced by 57% and 60% respectively as the junctionless configuration was applied to the double-gate vertical MOSFET. Such occurrence is majorly due to the electric field perpendicular to the flow of current in the junctionless configuration is significantly less than in the junctioned configuration. In junctioned configuration, the carriers propagating from source to drain experience much higher phonon scattering due to high electric field which subsequently lead to mobility degradation. Since the electrons/holes mobility in the channel region is significantly associated with this electric field, a much lower electric field featured in the JLDGVM could contribute a significant rise in drain current which is desirable for nanometer-scale complementary metal-oxide semiconductor applications.

Figure 5 depicts the semilog I_D-V_G transfer characteristics for both JLDGVM and JDGVM. The value of I_{ON}, I_{OFF} and SS of both devices can be extracted from the graph. It is shown that the I_{ON} magnitudes for the n- and p-channel JLDGVMs are approximately 50% higher than the JDGVMs. The majority carriers in the JDGVM's channel are heavily scattered due high electric field, whereas, the JLDGVMs experience much lower electric field that significantly increases the electrons/holes volume in the channel, subsequently leading to higher I_{ON}. In term of off-current (I_{OFF}), the n- and p-channel JLDGVMs exhibit approximately 20% and 75% smaller I_{OFF} than the JDGVMs. This implies the presence of junction in JDGVMs did cause larger effect of band-to-band-tunneling, leading to a significant leakage in the OFF state condition.

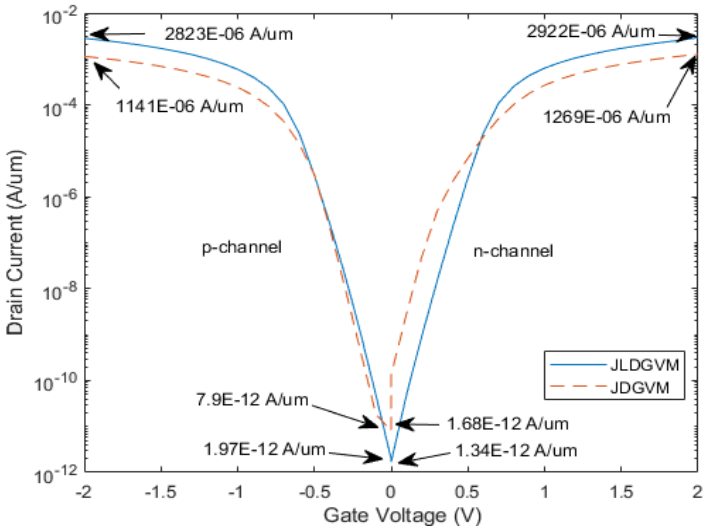

Figure 5. Semilog I_D-V_G transfer characteristics of both JLDGVM and JDGVM

The I_{ON}/I_{OFF} ratio is an important figure of merit for having high performance (more I_{ON}) and low leakage (less I_{OFF}) for the CMOS transistors. Figure 6 depicts the bar graph, indicating the level of I_{ON}/I_{OFF} ratio between JLDGVM and JDGVM for both types of channel.

Based on the bar graph, the n-channel and p-channel JLDGVM devices exhibit approximately 44% and 90% higher I_{ON}/I_{OFF} ratio over the n-channel and p-channel JDGVM devices respectively. This implies that the JLDGVM devices feature a better power consumption than the JDGVM devices as the devices could switch instantly from 'OFF' to 'ON' or vice versa at a minimum rate of required gate voltage. The increasing rate of drain current below the threshold limit is defined by a characteristic called the subthreshold slope (SS), which is mathematically derived from the semilog I_D-V_G transfer characteristics as:

$$SS = -\frac{dV_G}{d(\log(I_D))} \tag{10}$$

where the logarithm is in base 10, V_G is the gate voltage and I_D is the drain current. Figure 7 shows the bar graph, indicating the SS values between JLDGVM and JDGVM for both types of channel.

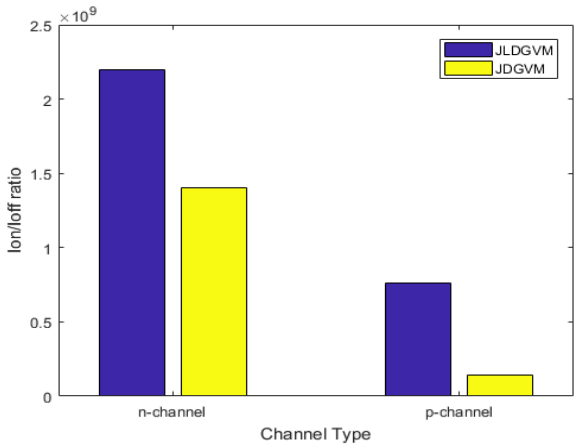

Figure 6. Bar Graph of the I_{ON}/I_{OFF} ratio for JLDGVM and JDGVM devices

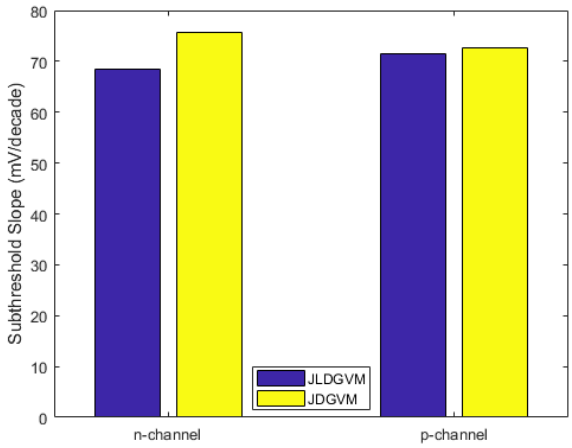

Figure 7. Bar Graph of the I_{ON}/I_{OFF} ratio for JLDGVM and JDGVM devices

The SS magnitude is commonly monitored to determine the scalablity limit of the device in which the changing rate of required gate voltage to increase the drain current by one decade is measured. Based on Figure 7, the n-channel and p-channel JLDGVM devices exhibit approximately 9.8% and 1.5% lower SS value than the n-channel and p-channel JDGVM devices respectively. The smaller SS indicates that the device has lower power consumption as it only requires minimum changes in V_G to increase one decade of I_D. Hence, the device with smaller SS (JLDGVM) would reach saturation mode much faster than the device with larger SS (JDGVM). For instance, the SS value for n-channel JLDGVM is 68.4 mV/decade, implying that a 68.4 mV increase of V_G would contributes approximately a tenfold increase in the I_D as shown in Figure 5. Therefore, in order to switch the current from its off-state (1.34E-12 A/µm) to the on state (I_D=7.9E-9 A/µm at threshold), a swing in V_G of

$$68.4mV \times \log \frac{7.9E-9A}{1.34E-12A} = 0.258V$$

is required. Similar to n-channel JDGVM, the SS value is measured at 75.8 mV/decade, thereby switching the current from from its off-state (1.68E-12 A/µm) to the on state (I_D=2.7 E-7 A/µm at threshold) requires a swing in V_G of

$$75.8mV \times \log \frac{2.7E-7A}{1.68E-12A} = 0.395V$$

is required. This implies that the n-channel JLDGVM can be turned on from its off-state much faster than the n-channel JDGVM.

In practice, the gate control over the channel region might not perfect due to electrostatic coupling between the gate and the ultrathin channel. This issue is mainly aroused due to the geometry-related process parameters such as channel length (L_{ch}) and pillar thickness (T_p), which, on the other hand, significantly deteriorate the performance of JLDGVMs. Since controlling process variations become the crucial factor in deciding the JLDGVM's performances, several optimization approaches [32-34] can be conveniently employed for further improvement.

4. CONCLUSION

In summary, the DC behaviours and performances of junctionless double-gate vertical MOSFETs (JLDGVMs) are compared with the junction double-gate vertical MOSFETs (JDGVMs). The performance evaluation of JLDGVMs and JDGVMs are made in term of on-state current, off-state current, I_{ON}/I_{OFF} ratio and subthreshold slope. Junctionless devices are observed to experience less short-channel effects than the junction devices. Comparison of I_D-V_G transfer characteristics are made between junctionless devices and junction devices, and the benefits of bulk transport in junctionless devices are clearly portrayed via the tremendous improvement of the drain current as the gate voltage is increased. Junctionless devices also have larger I_{ON}/I_{OFF} ratio and smaller subthreshold slope compared to the junction devices, implying that

the junctionless devices have better power consumption and faster switching capability. For future work, the impact of process parameters towards AC behavior of the JLDGVMs will be futher investigated. In addition, optimization approaches could be deployed for further enhancing the device performances.

ACKNOWLEDGEMENTS

The authors would like to thank to the Ministry of Higher Education (MOHE) for sponsoring this work under project (FRGS/1/2017/TK04/FKEKK-CeTRI/F00335) and MiNE, CeTRI, Faculty of Electronics and Computer Engineering (FKEKK), Universiti Teknikal Malaysia Melaka (UTeM) for the moral support throughout the project.

REFERENCES

[1] F. A. Rezali, M. Mazhar, N. Aida, F. Othman, and S. W. Muhamad, "Performance and device design based on geometry and process considerations for 14/16-nm FinFETs stress engineering," *IEEE Transactions on Electron Devices*, vol. 63, no. 3, pp. 974–981, 2016.

[2] K. E. Kaharudin, F. Salehuddin, N. Soin, A. S. M. Zain, M. N. I. A. Aziz, and I. Ahmad, "Electrical Characterization of Different High-k Dielectrics with Tungsten Silicide in Vertical Double Gate NMOS Structure," *ARPN Journal of Engineering and Applied Sciences*, vol. 11, no. 21, pp. 12328–12335, 2016.

[3] S. R. Mulmane, S. C. Wagaj, and N. U. Chaudhari, "Simulation of Nanoscale Fully Depleted EJ-SOI Junctionless MOSFET for High Performance," *International Journal of Industrial Electronics and Electrical Engineering*, vol. 4, no. 6, pp. 34–37, 2016.

[4] M. N. I. A. Aziz, F. Salehuddin, A. S. M. Zain, and K. E. Kaharudin, "Electrical Characteristics of PMOS Bulk MOSFET and PMOS Silicon-on-insulator (SOI) MOSFET Device," *ARPN Journal of Engineering and Applied Sciences*, vol. 11, no. 10, pp. 6315–6318, 2016.

[5] S. Dubey, P. K. Tiwari, and S. Jit, "On-current modeling of short-channel double-gate (DG) MOSFETs with a vertical Gaussian-like doping profile," *Journal of Semiconductors*, vol. 34, no. 5, p. 054001, May 2013.

[6] B. Lakshmi and R. Srinivasan, "Effect of Process Parameter Variation on ft in Coventional and Junctionless Gate-All-Around Devices," *Journal of Engineering Science and Technology*, vol. 10, no. 8, pp. 994–1008, 2015.

[7] Y. Chen, M. Mohamed, M. Jo, U. Ravaioli, and R. Xu, "Junctionless MOSFETs with laterally graded-doping channel for analog/RF applications," *Journal of Computational Electronics*, vol. 12, no. 4, pp. 757–764, 2013.

[8] K. P. Londhe and Y. V. Chavan, "A Novel Double Gate Junction-less MOSFET Using Germanium," in *International Conference on Innovative Trends in Engineering Research*, 2016, pp. 115–118.

[9] S. Das and S. Kundu, "A Review on Junctionless Transistor - A Prospective sub-10nm Logic Device," *Advanced Research in Electrical and Electronic Engineering*, vol. 1, no. 3, pp. 98–102, 2014.

[10] C. Y. Chen, J. T. Lin, and M. H. Chiang, "Comparative study of process variations in junctionless and conventional double-gate MOSFETs," in *IEEE Nanotechnology Materials and Devices Conference, IEEE NMDC 2013*, 2013, pp. 1–2.

[11] R. Norani, "A Dynamic Simulation on Single Gate Junctionless Field Effect Transistor Based on Genetic Algorithm," *Advances in Computer Science: an International Journal*, vol. 3, no. 5, pp. 140–145, 2014.

[12] A. K. Mandia and A. K. Rana, "Performance Enhancement of Double Gate Junctionless Transistor Using High-K Spacer and Models," in *Proceedings of 11th IRF International Conference*, 2014, no. 8, pp. 8–11.

[13] A. Kamath, X. Chen, N. Shen, X. Li, N. Singh, G. Q. Lo, and D.-L. Kwong, "Junctionless CMOS Transistors with Independent DoubleGates," *International Journal of Information and Electronics Engineering*, vol. 3, no. 1, pp. 13–15, 2013.

[14] J. P. Colinge, C. W. Lee, A. Afzalian, N. Dehdashti, R. Yan, I. Ferain, P. Razavi, B. O'Neill, A. Blake, M. White, A. M. Kelleher, B. McCarthy, and R. Murphy, "SOI gated resistor: CMOS without junctions," in *2009 IEEE International SOI Conference*, 2009, pp. 1–2.

[15] C. W. Lee, A. Borne, I. Ferain, A. Afzalian, R. Yan, N. Dehdashti Akhavan, P. Razavi, and J. P. Colinge, "High-temperature performance of silicon junctionless MOSFETs," *IEEE Transactions on Electron Devices*, vol. 57, no. 3, pp. 620–625, 2010.

[16] M. W. Akram, B. Ghosh, P. Bal, and P. Mondal, "P-type double gate junctionless tunnel field effect transistor," *Journal of Semiconductors*, vol. 35, no. 1, p. 014002, 2014.

[17] M. A. Riyadi, I. D. Sukawati, T. Prakoso, and Darjat, "Influence of gate material and process on junctionless FET subthreshold performance," *International Journal of Electrical and Computer Engineering*, vol. 6, no. 2, pp. 895–900, 2016.

[18] S. Archana, G. Vallathan, and M. A. Kumar, "Analytical Modeling of Dual Material Junctionless Surrounding Gate MOSFET," *SSRG International Journal of Electronics and Communication Engineering*, vol. 4, no. 3, pp. 40–43, 2017.

[19] F. Khorramrouz, S. A. S. Ziabari, and A. Heydari, "Analysis and study of geometrical variability on the performance of junctionless tunneling field effect transistors: Advantage or deficiency?," *Analysis and study of geometrical variability on the performance of junctionless tunneling field effect transistors: Advantage or deficiency?*, vol. 9, no. 3, pp. 260–272, 2018.

[20] R. Ambika and R. Srinivasan, "Impact of structural process variation on junctionless silicon nanotube FET,"

Advances in Natural Sciences: Nanoscience and Nanotechnology, vol. 9, pp. 1–7, 2018.
[21] H. Carrillo-Nunez, M. M. Mirza, D. J. Paul, D. A. MacLaren, A. Asenov, and V. P. Georgiev, "Impact of Randomly Distributed Dopants on __-Gate Junctionless Silicon Nanowire Transistors," *IEEE Transactions on Electron Devices*, vol. 65, no. 5, pp. 1692–1698, 2018.
[22] K. Biswas, A. Sarkar, and C. K. Sarkar, "Fin shape influence on analog and RF performance of junctionless accumulation-mode bulk FinFETs," *Microsystem Technologies*, vol. 24, no. 5, pp. 2317–2324, 2018.
[23] V. Pathak and G. Saini, "A Graded Channel Dual-Material Gate Junctionless MOSFET for Analog Applications," *Procedia Computer Science*, vol. 125, pp. 825–831, 2018.
[24] A. Kumar, M. M. Tripathi, and R. Chaujar, "Comprehensive analysis of sub-20 nm black phosphorus based junctionless-recessed channel MOSFET for analog/RF applications," *Superlattices and Microstructures*, vol. 116, no. February, pp. 171–180, 2018.
[25] E. Simoen, A. Veloso, P. Matagne, N. Collaert, and C. Claeys, "Junctionless Versus Inversion-Mode Gate-All-Around Nanowire Transistors from a Low-Frequency Noise Perspective," *IEEE Transactions on Electron Devices*, vol. 65, no. 4, pp. 1487–1492, 2018.
[26] D. A. J. Millar, X. Li, U. Peralagu, M. J. Steer, I. M. Pavey, G. Gaspar, M. Schmidt, P. K. Hurley, and I. G. Thayne, "High Aspect Ratio Junctionless InGaAs FinFETs Fabricated Using a Top-Down Approach," *2018 76th Device Research Conference (DRC)*, no. September, pp. 1–2, 2018.
[27] S. Nilamani, P. Chitra, and V. N. Ramakrishnan, "Topological variation on sub-20 nm double-gate inversion and Junctionless-FinFET based 6T-SRAM circuits and its SEU radiation performance," *Microelectronics Reliability*, vol. 82, no. July 2017, pp. 11–19, 2018.
[28] M. Puttaveerappa, V. Kumar, J. Lin, and S. Member, "Junctionless FETs With a Fin Body for Multi-V TH and Dynamic Threshold Operation," *IEEE Transactions on Electron Devices*, vol. 65, no. 8, pp. 3535–3542, 2018.
[29] S. C. Wagaj, S. Patil, and Y. V. Chavan, "Performance analysis of shielded channel double-gate junctionless and junction MOS transistor," *International Journal of Electronics Letters*, vol. 6, no. 2, pp. 192–203, 2018.
[30] M. Vadizadeh, "Characteristics of GaAs/GaSb tunnel field-effect transistors without doping junctions: numerical studies," *Journal of Computational Electronics*, vol. 17, no. 2, pp. 745–755, 2018.
[31] Silvaco, "Silvaco ATLAS manual Device Simulation Software," 2006.
[32] K. E. Kaharudin, F. Salehuddin, and A. S. M. Zain, "Optimization of Electrical Properties in TiO2/WSix-based Vertical DG-MOSFET using Taguchi-based GRA with ANN," *Journal of Telecommunication, Electronic and Computer Engineering the*, vol. 10, no. 1, pp. 69–76, 2018.
[33] K. E. Kaharudin, F. Salehuddin, A. S. M. Zain, and M. N. I. A. Aziz, "Comparison of Taguchi Method and Central Composite Design for Optimizing Process Parameters in Vertical Double Gate MOSFET," *ARPN Journal of Engineering and Applied Sciences*, vol. 12, no. 19, pp. 5578–5590, 2017.
[34] K. E. Kaharudin, F. Salehuddin, A. S. . Zain, and M. N. I. . Aziz, "Application of Taguchi-based Grey Fuzzy Logic for Simultaneous Optimization in TiO2/WSix-based Vertical double-gate MOSFET," *Journal of Telecommunication, Electronic and Computer Engineering*, vol. 9, no. 2–13, pp. 23–28, 2017.

BIOGRAPHIES OF AUTHORS

K. E. Kaharudin received Ph.D in Electronic Engineering and M. Eng degree in Computer Engineering from Technical University of Malaysia Melaka (UTeM), in 2017 and 2013 respectively. His Ph.D project focused on the process optimization of vertical double gate MOSFET. His research's interests include CMOS design, microelectronics, semiconductors, engineering optimization and artificial intelligence. Recently, his efforts emphasize on the simulation design of Junctionless MOSFET, silicon-on-insulator (SOI) MOSFET, high-*k*/metal-gate stack technology and design of experiment (DoE).

Z.A.F.M.Napiah received the B.Eng. degree in electrical engineering and the M.Eng. degree in Microelectronic from Universiti Teknologi Malaysia (UTM). He received the Ph.D. degree in Microelectronics from Kanawa University, Japan. He is currently a senior lecturer at Faculty of Electronic and Computer Engineering (FKEKK), UTeM. His research interest includes process and device simulation of MOSFET device, advanced CMOS design and CMOS based Photodetector and Photoreceiver.

F. Salehuddin received the B.Eng. degree in electrical engineering (Communication) from Universiti Teknologi Mara (UiTM), Malaysia in 2001 and the M.Sc. degree in Electrical, Electronic and System Engineering from Universiti Kebangsaan Malaysia, in 2003. She received the Ph.D. degree in Microelectronics Engineering from Universiti Tenaga Nasional (UNITEN), Malaysia in 2012. She joined Universiti Teknikal Malaysia Melaka (UTeM) in December 2001 as a tutor and is currently a senior lecturer at Faculty of Electronic and Computer Engineering (FKEKK), UTeM. Her research interest includes process and device simulation of nanoscale MOSFETs device, advanced CMOS design, optimization approach (DOE) and process parameter variability.

A. S. M. Zain received the B.Eng degree in electrical, Electronic and System engineering and M. Sc in Microelectronics from National University of Malaysia (UKM), Malaysia She received the Ph.D. degree in Nanoelectronics Engineering from University of Glasgow, UK in 2013. She is currently working as a senior lecturer at Faculty of Electronic and Computer Engineering (FKEKK), Universiti Teknikal Malaysia Melaka (UTeM). Her research interest includes Nanoscale Device Design and Simulation,Variability and Reliability of Emerging Technology Devices, IC Design for Biomedical Applications.

Ameer F. Roslan received by. Sc. Degree in Telecommunication Engineering from Technical University of Malaysia Melaka (UTeM), in 2017. He is currently pursuing his M.Sc degree in electronics and doing research on the DG-FinFET device at Centre for Telecommunication Research and Innovation, Faculty of Electronics and Computer Engineering, Technical University of Malaysia Melaka (UTeM). His research interest includes the DG-FinFET architecture and statistical.