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Integrated cmos rectifier for rf-powered wireless sensor network nodes

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Article Info	ABSTRACT
	This article presents a review of the CMOS rectifier for radio frequency energy harvesting application. The on-chip rectifier converts the ambient low-power radio frequency signal coming to antenna to useable DC voltage that recharges energy to wireless sensor network (WSN) nodes and radiofrequency identification (RFID) tags, therefore the rectifier is the most important part of the radio frequency energy harvesting system. The impedance matching network maximizes power transfer from antenna to rectifier. The design and comparison between the simulation results of one- and multi-stage differential drive cross connected rectifier (DDCCR) at the operating frequencies of 2.44GHz, and 28GHz show the output voltage of the multi-stage rectifier doubles at each added stage and power conversion efficiency (PCE) of rectifier at 2.44GHz was higher than 28GHz. The (DDCCR) rectifier is the most efficient rectifier topology to date and is used widely for passive WSN nodes and RFID tags.

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1. INTRODUCTION

An on-chip rectifier is semiconductors bsed device of a size of a few square microns. It is a component built into the radio frequency energy harvester converts AC from RF signal coming to antenna to useful DC voltage. Rectifier is the most important component of the RF energy harvesting system block diagram because the rectifier converts AC power to the DC voltage required to recharge energy to applications such as the WSN nodes. CMOS stands for Complementary Metal Oxide Semiconductor, and it's a technology builds integrated circuits. CMOS is a preferable technology for integrating the rectifier circuit on chip. CMOS technology is the most efficient to date and has superior benefits. The CMOS circuit has less power consumption, a wider operating temperature range and is better protected against noise. Battery replacement and maintenance are difficult if not impossible in the WSN nodes and the output power of the on-chip rectifier is less than the operating energy of the WSN node in the wireless power transfer domain. The output power of rectifier should be equal or more than the energy consumption of sensor node for the sensor to be capable to operate perpetually. Wireless power transfer is a new technology and an independent scientific field consist mainly of transmitter and receiver subfields, and the receiver is such that the radio frequency energy harvesting system discussed in this article focuses on WSN networks. The simulation of

DDCC rectifier circuit was performed using SilterraC18G PDK (Process Design Kit) in a standard 0.18 μm CMOS technology. RF Energy harvesting (RFEH) is a green technology helps preserve the environment by eleminating the use of batteries and recycling the ambient RF waves using RF energy harvesting system.

An on-chip CMOS rectifier is a miniaturized device based on semiconductors. The CMOS rectifier converts the small amount of power dedicated or small amount of-voltage ambient signal into a useful DC voltage for replenishing energy to microsystem applications. The CMOS differential cross connected rectifier is the most efficient so far and is used widely for radio frequency energy harvesting applications such as WSN nodes and RFID tags. The various technologies of modern RF tramsmitters send lots of power into the air, and in free space the RF wave carries both energy and information. Wireless energy reception is fundamentally different from wireless information reception. The RF signal uses energy to propagate information in free space between antennas. The reception unit can be active or semi passive with power source such as battery, or passive tage which is smaller in size because it contains no battery. RF signal come from analog RF dedicated source such as any RF power transmitter and RFID reader and from ambient RF sources such as radio mast, TV tower, wireless router, and GSM cell tower.

The on-chip CMOS rectifier of dedicated radio frequency energy harvesting system applies to RFID tags and implementable medical devices. The ambient energy harvesting system applies to recharge energy to active, and WSN nodes that spread immensely in the environment, as well as IoT devices in urban and semi urban areas and these kind of applications require little amount of energy to operate and the required energy can be harvested as these kind of applications increase enormously nowadays. Since the RF signal carries energy and information, the RF energy harvester and the sensor receiver share the same antenna as in Figure 1.
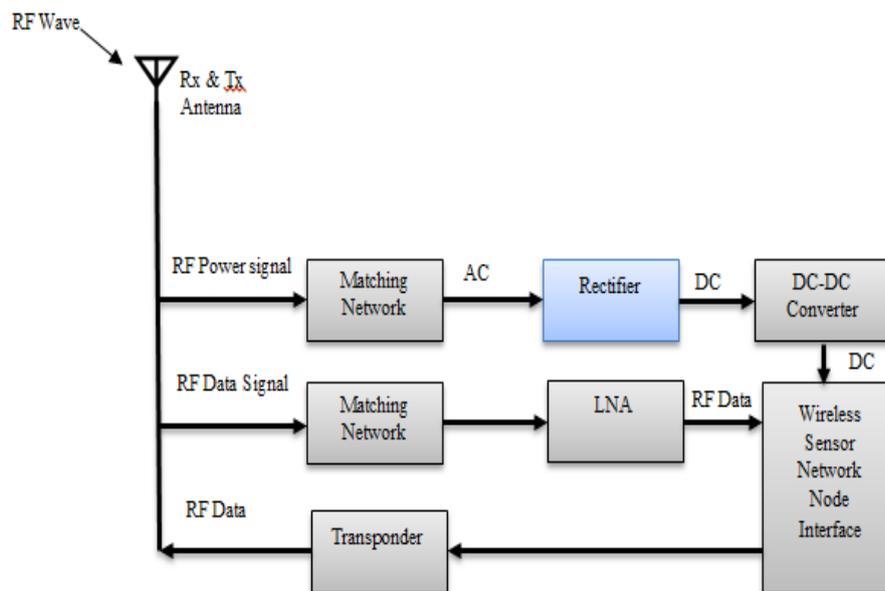

Figure 1. WSN system with RF energy harvester block diagram

On Chip Rectifier Power Conversion Efficiency η is defined as the ratio of DC output power to the AC input power from the antenna. $\eta = \frac{P_{out(DC)}}{P_{in(AC)}} \times 100\%$, $P_{out} = \frac{V_{out}^2}{R}$, and the main challenge in designing a CMOS radio frequency energy harvesting system is the design of a rectifier circuit operating at small amount of input power, due to the bounded power of RF wave signal as the signal power must be a function of the power levels of the RF transmitter, and for safety and health reasons, FCC rules restrict RF high level power radiations. Figure 2 (a) shows conventional diode connected transistor, and Figure 2 (b) shows Complementary diode connected transistor. Rectifier types are full wave and half wave, and structures are differential rectifier and a single ended rectifier.
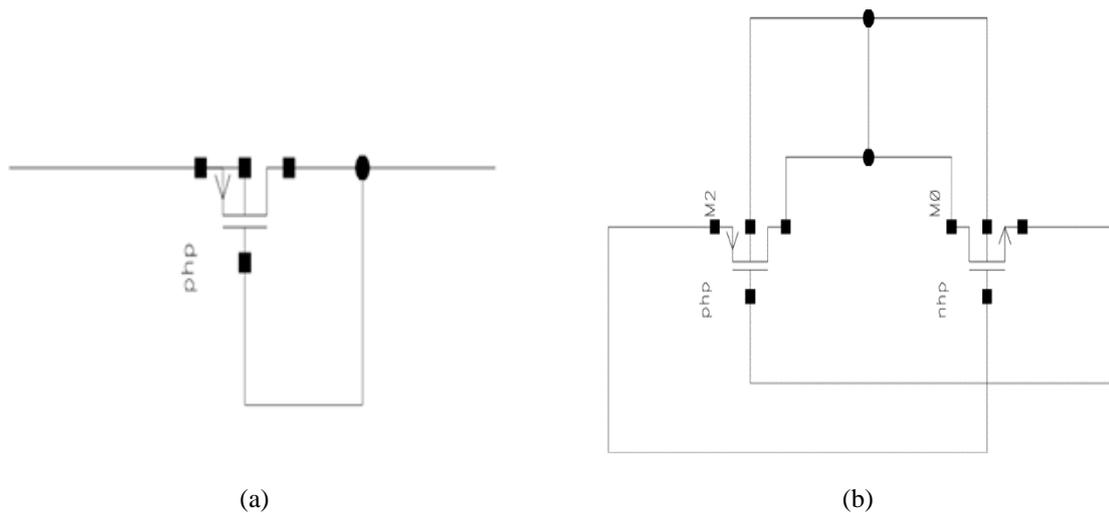
Figure 2. Diode connected transistor, (a) Conventional, (b) Complementary

The CMOS cross-connected rectifier outperforms the diode rectifier, and in our design we use the differential drive topology in which the voltage threshold cancellation scheme is implemented, and as the ambient RF power is only a few microwatts, conventional rectifier circuit reconfiguration with improvement techniques are used to increase the output voltage and efficiency of the rectifier circuit such as voltage cancellation technique in [1] the control loop circuit in [2], adaptive self biasing as in [3], improvement of the Dynamic Threshold Reduction (DTR) technique using clamper circuit that biases the gates of the pMOS diode switches through a capacitor and a diode-connected pMOS transistor[4], and implementation of impedance matching network to convert most of the available energy from the antenna to the input of threshold voltage compensation rectifier circuit [5]. In previous study [6] was found that at low input power level, the cross connected rectifier is most efficient compared to other topologies and adjusting transistors sizes (PMOS/NMOS) increases PCE. The diode-connected transistor is the fundamental unit of the on-chip CMOS rectifier and radio frequency energy harvesting solves the constraint of high-power consumption and small battery size of body area network [7]. Improving the bandwidth for the covering of wide range of telecommunication operating frequencies using an integrated transformer with ultra wideband antenna for next generation radio frequency front end [8].

The Pi impedance matching coverage can be increased at multi operating frequencies through configuring the electrical distance [9]. The PCE of rectifier is controlled by topology of rectifier circuit, input RF power, operating frequency, MOS transistor size, circuit component values such as coupling capacitors, output capacitor and load resistors. Simulation of power conversion efficiency (PCE) of conventional cross–connected rectifier topology found that PCE is 75.4% at input power of -12.5dBm [10], for achieving high PCE, a low voltage threshold transistor with less leakage current is preferred [11] The transistor internal resistance is one of the causes of low PCE and it should be reduced by adjusting transistor size. The transistor's threshold voltage is subtracted from the low input voltage and reduces the PCE, therefore the implementation of voltage threshold cancellation (VTC) technique is used to provide the threshold voltage internally from the output of the rectifier for passive RFID tag [12].

The cons of VTC that as the PMOS and NMOS voltage from DC output exceeds the threshold voltage it causes high leakage current. For semi-passive and active WSN node and RFID tag, external voltage threshold cancellation is possible with battery. Reducing the threshold effect and increasing efficiency can be achieved from rectifier itself by storing energy from output of rectifier in capacitor and provide stored energy to base transistor and provide the minimum threshold voltage [13]. The new ambient energy harvesting opportunities and capabilities were studied, investigated, revealed the ambient radio frequency available at 1 μW/cm2, and predicted that harvesting and recycling efficiently of ambient electromagnetic energies in the air are potential resources to recharge energy to RFID tags [14], WSN nodes [15]. A wireless communication network based on a potentially hybrid access point for far-field transfer shall add deploy a power beacon, to the current communication systems for enabling simultaneous power and data transfer. it is very intersting for evolving advanced communication and signal processing techniques for the design of efficient WPT systems [16]. The ambient RF energy sources available at 1 μW/ cm^2 have been revealed [17]. Recent studies have shown the ability to harvest ambient RF engergy and predicts that the efficient harvesting and recycling of ambient RF energy from the air is a potential power source helps conserving energy and is for recharging

energy for applications requires such amount of energy, as for example ubiquotesly deployed WSN nodes [18, 19]. More recently, the radiative WPT has sparked a keen interest in a relatively small energy distribution over a few meters to possibly several hundred meters, due to the growing need to build reliable and practical WPT systems for remote recharging energy to devices, such as RFID tags [20-22], and wireless sensors [23-28]. Table 1 Summarizes the recently released papers on CMOS rectifiers and comparison with this work, the voltage threshold cancellation (VTC) technique enables the rectifier to perform at low input power. Increasing number of stages increases output voltage but reduces efficiency.

Table 1. State of the art CMOS differential drive cross-connected rectifiers performance correlations at standard process for radio frequency energy harvesting applications

Year/Source	Frequency (Hz)	Technique	Number of Stages	Input Power	Output Voltage	Load RL(Ω)	Output power	Efficiency
Kotani, 2009 [1]	953MHz	VTC	1	-12.5 dBm	0.616V	10K	37.95µW	67.50%
Stoopman, 2014 [2]	868MHz	VTC, control loop	5	-17 dBm	1.4V	0.33M	7.98µW	40%
Ouda, 2017 [3]	433MHz	VTC, self biased	1	-15.2 dBm	0.99V	50K	19.72µW	65.30%
Manal M. Mohamed, 2018 [4]	953MHz	DTR	1	-16.8 dBm	0.38	10K	14.4µW*	70%
	402MHz			-16.5 dBm	0.52V		27µW*	86%
This work 2018	2.44GHz	VTC	7	-16 dBm	1V at -8.6dBm	60K	2.3µW	58%
	28GHz		1		1V at 2dBm		0.014µW	3.6%

*Estimatated value

2. RESEARCH METHOD
2.1. The method of using Wireless Power Transfer (WPT)

The method of using wireless power transfer (WPT) has the advantage of providing enough and durable power to the sensor nodes potentially for a lifetime or for a very long time. One of the approaches to increase the efficiency of WPT is to use an appropriate impedance matching network that also develops the efficiency at the front end of the dedicated WPT receiver, as well as the ambient radio frequency energy harvester, and cascading rectifier's stages increases the output DC voltage which provides a sustainable source of adequate power to the nodes of the wireless sensor network. The Cadence Virtuoso platform with the Silterra Process Design Kit (PDK) assists in the development of the schematic design of the rectifier's circuit. The load of the rectifier was reduced from 1MΩ during my first simulations to 60KΩ, and however this reduction decreases the output DC voltage value, but the efficiency of the rectifier increased. A 5pF capacitor is used to filter out the DC voltage, to reduce the voltage ripple and smoothen the DC voltage wave. Figure 3 shows schematic of conventional cross-connected rectifier. Figure 4 shows a representation of the use of WPTto recharge energy to WSN node.
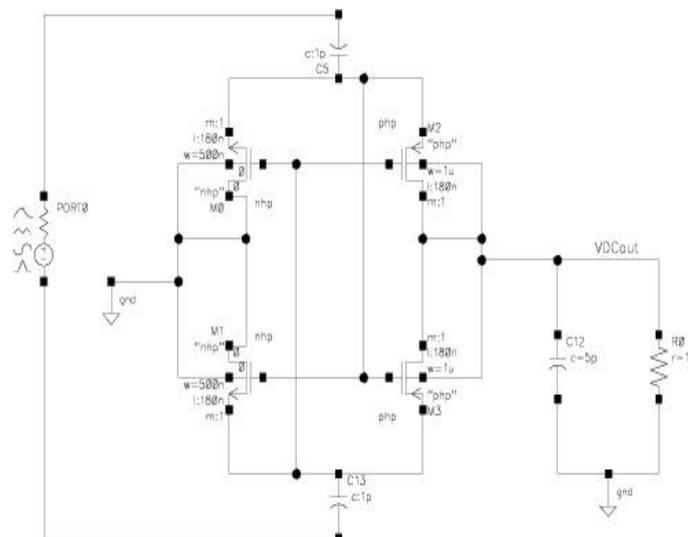

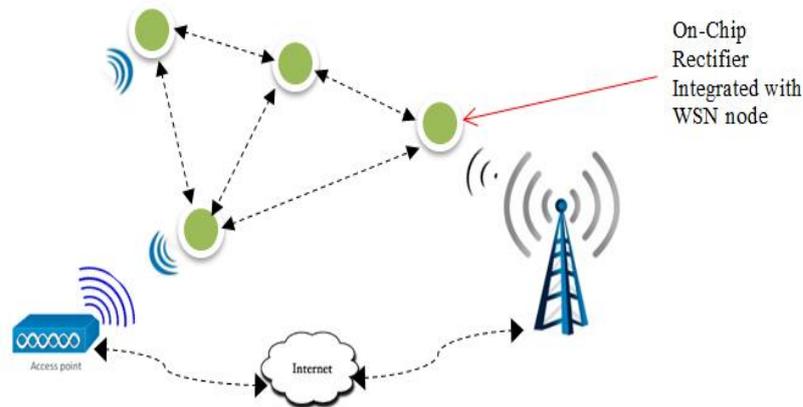Figure 3. Schematic of conventional cross-connected rectifier

Figure 4. Symbolic representation of RF Energy transmitters Re-charging wirelessly WSN nodes

2.2. Cadence parametric analysis tool used to optimize the input impedance of the rectifier

Use WPT technology to provide wireless Sustainable power to recharge WSN node through RF energy harvester.

2.3. Optimize the Harvester System and replace sensor battery

Following the design flowchart of the CMOS circuit, we first draw the on-chip rectifier circuit in the schematic capture diagram, specifying input power, operating frequency, and load. The input power of the signal which depends on the available power in the ambient environment, ambient signal strength in urban area between -20dBm to -40dBm with peak -33dBm at distance between 25 to 100 meters, and in our design, we define the input power as -16dBm, assuming the RF energy harvester near enough to an ambient RF source, and simulate for input power range from -40dBm to 10dBm, at operating frequencies of 2.44 GHz and 28GHz. Once the results of the schematic capture simulation have been verified, we begin the physical design of the circuit and execute the simulation and compare it with the previous simulation. Finally, the measurement of the RF and DC function of the manufactured chips and the comparison with the results of the simulation. The rectifier's stage cascade to provide the sensor node required DC voltage.

a. Design and development of the rectifier circuit: the conventional cross connected rectifier circuit is simulated with rectifier's designed input impedance and the matching network as well, and at output stage a filter capacitor of 5pF and a load of 60KΩ.
- Single Stage rectifier: Figure 3 shows CMOS conventional differential cross connected rectifier cell made up of two pMOS transistors and two nMOS transistors connected in cross topology similarly to the counterpart of diode bridge rectifier
- Multi stage rectifier: the purpose of cascading the single stage rectifier to multistage is to double the output voltage to be as required for the application load
- Rectifier Input Impedance: is modeled as a resistor and a capacitor in parallel as shown in the 2.44GHz schematic in Figure 5 (a), rectifier equivalent circuit with Pi- impedance matching network at 28GHz in Figure 5 (b), and equivalent circuit of rectifier with cascaded L-impedance matching network in Figure 6. The rectifier input impedance is expressed as a complex number, $Z\_rect=R – jX\_c.$, where R and Xc are measured in Ω. For multistage rectifier with 2.44GHz operating frequency, the input impedance matching network $Z\_rect=13.84–j335$, and for rectifier circuit at 28GHz single stage rectifier, the input impedance matching network was $Z\_rect=49.98–j212$.
- Impedance Matching Network Design: is important because the proper impedance matching circuit transfers all power from radio frequency waves coming to antenna to input rectifier and hence increases output voltage and power conversion efficiency from end to end. In Figure 6 L-matching network was shown with rectifier equivalent ciurcuit at 2.44GHz, and in Figure 7 cascaded in series an L-matching network was shown with rectifier equivalent circuit at 28GHz. Cascadecd L-impedance matching networks in series increases the bandwidth of impedance matching. All the designed impedance matching networks with reflection coefficient S11 is -10dBm or less, as shown in Figure 7 (a) and (b).
- Load and capacitor filtering, the filter capacitor is designed as 5pF and Load as 60K
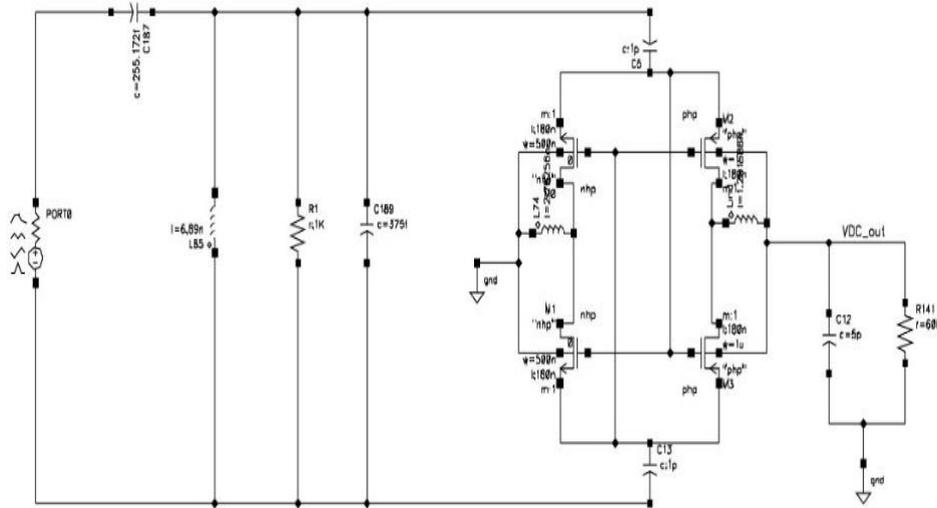
(a)
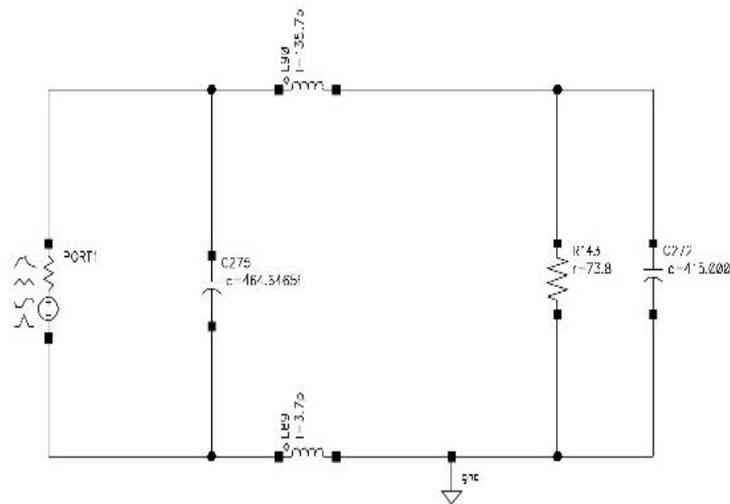
(b)

Figure 5. (a) Schematic rectifier with impedance matching network for 2.44GHz,
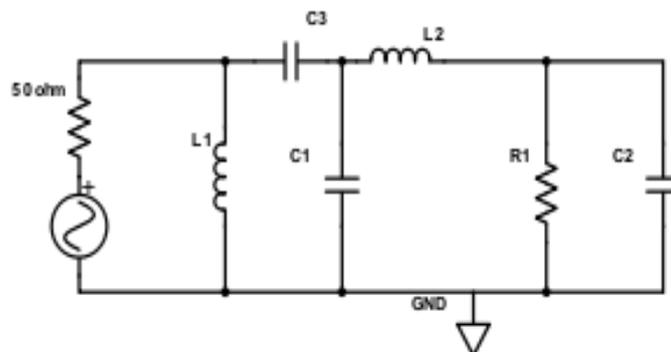(b) Pi-Matching network for 28GHz

Figure 6. L-cascaded matching network

3.   RESULTS AND ANALYSIS

The rectifier circuits are modelled using Silterra C18G PDK with a standard 0.18μm CMOS technology. The output voltage of the rectifier proportional to the input voltage or input power at fixed load. The small value load decreases the output voltage to possible less than the voltage required for activating the sensor; therefore, the one-stage rectifier circuit is cascaded to N-stage to produce the required output DC voltage.

3.1. Input impedance and matching network

The reflection coefficient S11 values at 2.44GHz is -46dB, and at 28 GHz is -67.74 dB are shown in Figure 7 (a) and Figure 7 (b) respectively.
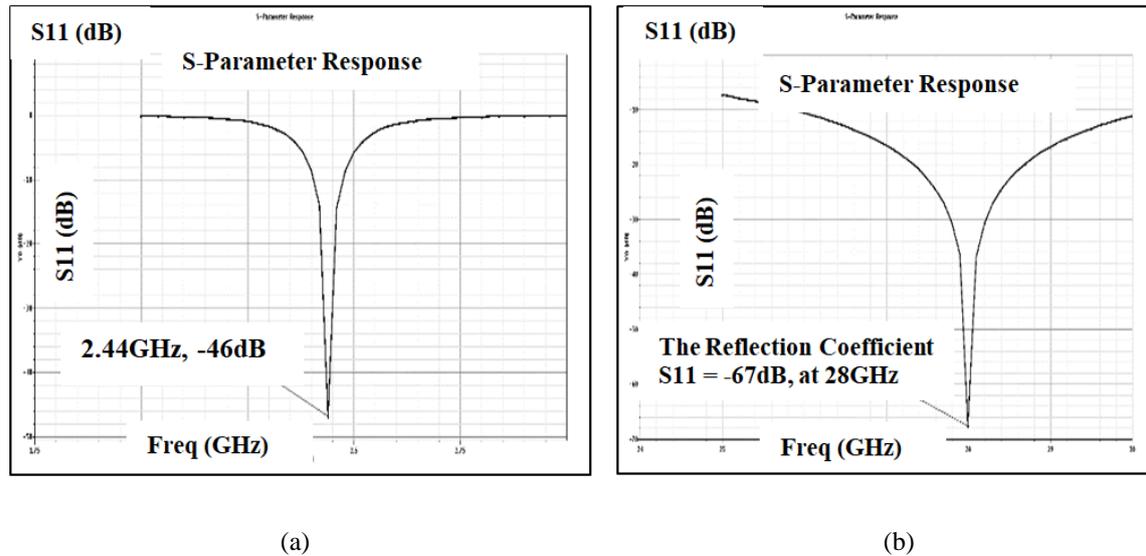

(a)   (b)

Figure 7. (a) Reflection coefficient S11 at 2.44 GHz, (b) Reflection coefficient S11 at 28GHz

3.2. Single-stage and multi-stage rectifier

Single stage differential cross connected rectifier is modeled with output load resistor equals to 60 KΩ, and filtering capacitor is 5pF. Input power of -16dBm and operating frequency at first stimulation 2.44GHz, and secondly 28GHz. Figure 8 shows a DC output voltage for different input power levels. With an input power of -16 dBm, and an output load of 60 K, the results of the simulation show that at 2.44GHz the PCE of one stage rectifier circuit is 79% and with 7 stages the PCE is 58%. The PCE decreases slightly with increasing number of stages due to increase of power dissipation at transistors. For a multi-stage DCCR rectifier with an operating frequency of 2.44 GHz, the reflection coefficient was -46 dB, and a simulation in the range of -40 dBm to 10 dBm resulted to a 1V at -8.6 dBm. For the single-stage DCCR rectifier at 28 GHz operating frequency, the reflection coefficient was -64 dB and a simulation in the power input range of -40 dBm to 10 dBm resulted to a 1V at 2 dBm and a maximum PCE of 3.6%. As frequency increases, PCE decreases and bandwidth increases, and the impedance matching network becomes easier to design with smaller values capacitor and inductor.

The output DC voltage varies with the change of load resistor value, and the filter capacitor smotthens the ripple voltage. Figure 9 shows output DC voltage with two different loads. First load value is 10K and second load value is 60K and with same input power the output DC voltage at 60K is higher than 10K.

Periodic Steady State Analyses

v /Output-DC-Voltage PORT0:dbm=-16; pss (V)   v /Output-DC-Voltage PORT0:dbm=0; pss (V)
v /Output-DC-Voltage PORT0:dbm=10; pss (V)   v /Output-DC-Voltage PORT0:dbm=-20; pss (V)

Output VDC = 7.4V, at Pin = 10dBm

Output VDC = 3.5V, at Pin = 0dBm

Output VDC = 174mV, at Pin = -16dBm

Output VDC = 20.58mV, at Pin = -20dBm
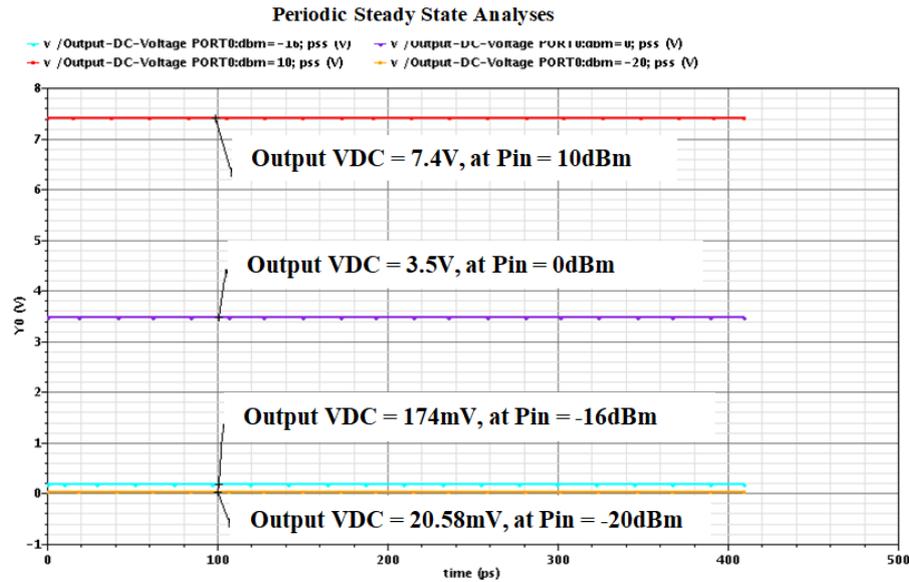
Figure 8. Output DC voltage for 2.44GHz at 60K Load and different input power values

Periodic Steady State Analyses

VDC at 10K ohm   Output DC voltage at 60K ohm

Output VDC = 174mV, at Pin = -16dBm, and RL = 60K
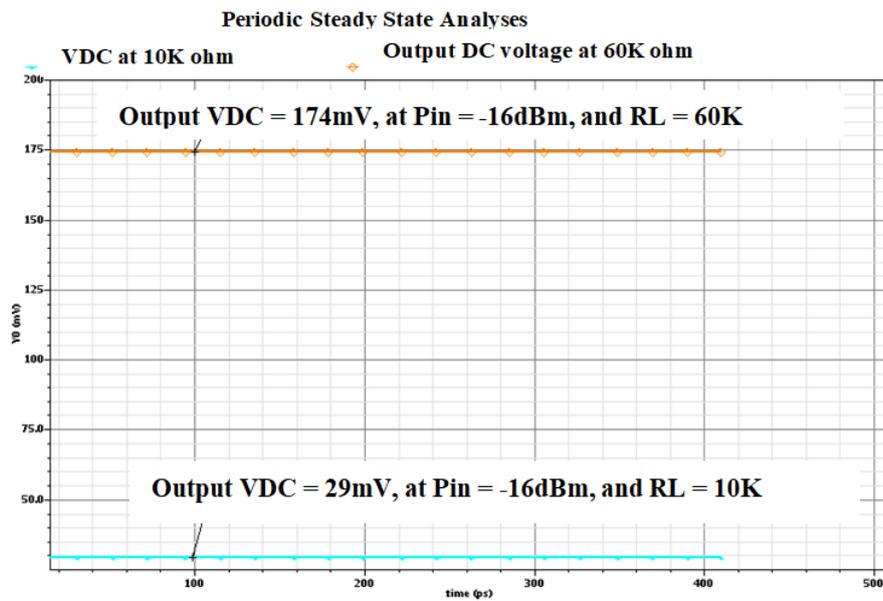
Output VDC = 29mV, at Pin = -16dBm, and RL = 10K

Figure 9. Output DC voltage at same Pin and different Load R, VDC=29mV at RL=10K
and 174mV at RL=60K

4.   CONCLUSION

The design of CMOS rectifier for energy harvesting from dedicated and ambient radiofrequency energy sources was reviewed. The use of the harvested energy to recharge a WSN node is a feasible technology and applies to radio frequency identification tags, internet of things and implementable medical devices. The power conversion efficiency of the on-chip differential drive cross connected rectifier is higher at 2.44GHz than 28GHz. Wideband impedance matching networks have been designed and optimized for a reflection coefficient of less than -10 dBm for a differential cross connected rectifier for operating frequencies of 2.44 GHz and 28 GHz. Simulation with an input power range of -40 to 10 dBm showed an increase in the rectifier output voltage after increasing the load from 10K to 60K. The output voltage is further enhanced by increasing the number of stages. When an RF signal carries energy and information, the RF receiver of the energy harvester and the sensor share the same antenna.

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