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Design consideration in low dropout voltage regulator for batteryless power management unit

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ABSTRACT

Harvesting energy from ambient Radio Frequency (RF) source is a great deal toward batteryless Internet of Thing (IoT) System on Chip (SoC) application as green technology has become a future interest. However, the harvested energy is unregulated thus it is highly susceptible to noise and cannot be used efficiently. Therefore, a dedicated low noise and high Power Supply Ripple Rejection (PSRR) of Low Dropout (LDO) voltage regulator are needed in the later stages of system development to supply the desired load voltage. Detailed analysis of the noise and PSRR of an LDO is not sufficient. This work presents a design of LDO to generate a regulated output voltage of 1.8V from 3.3V input supply targeted for 120mA load application. The performance of LDO is evaluated and analyzed. The PSRR and noise in LDO have been investigated by applying a low-pass filter. The proposed design achieves the design specification through the simulation results by obtaining 90.85dB of open-loop gain, 76.39º of phase margin and 63.46dB of PSRR respectively. The post-layout simulation shows degradation of gain and maximum load current due to parasitic issue. The measurement of maximum load regulation is dropped to 96mA compared 140mA from post-layout. The proposed LDO is designed using 180nm Silterra CMOS process technology.

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1. INTRODUCTION

As telecommunication systems getting evolve, the RF energy is widely spread to the surrounding from wireless broadcast system. This energy is available abundantly and some of it is being wasted [1]. Therefore, RF energy harvesting is proposed as an alternative to recycle and reuse it. However, the harvested energy is highly receptive to noise and volatile. An LDO is used to stabilize the harvested source so that the generated source is working efficiently for the next stages of the system. When considering the LDO, it is important for the device to suppress noise from upstream sources and downstream loads, while not adding further noise itself. Voltage regulator noise is measured in volts rms. The noise sources in an LDO can be separated by two categories, which are intrinsic and extrinsic [2-3]. Intrinsic noise refers to noise that is internally generated by any electronic device, whereas extrinsic noise is passed on from a source outside the circuit. The major sources of intrinsic noise in LDOs are the internal reference voltage and the error amplifier. Any device with current flowing through it is a potential noise source. In most cases, the Bandgap Voltage Reference (BGR) circuit consists of many resistors, transistors, and capacitors tend to dominate the noise source in an LDO [4, 5]. PSRR is another parameter used to evaluate the performance of an LDO. It is

a measure of how well a circuit suppresses or rejects extraneous signals which are basically noise and ripple appearing at the power supply input and keeps these unwanted signals from corrupting the output of the circuit [6-8]. PSRR and noise have different characteristics.

A design of an LDO voltage regulator with fast load regulation for a capacitor-less output is proposed by [9]. The regulator operates with supply voltages from 1.6V to 2V, providing 0.9V to 1.4V regulated voltages with a 99.2% current efficiency and fully integrated architecture with a 100pF load capacitor. Capacitor sizing plays a big role in reducing noise. However, it has a trade-off issue regarding the area consumption. External capacitor-less LDO architecture and Current Amplifier Hybrid Compensation (CAHC) scheme implements an active feedback-feedforward compensation system was introduced by [10] to overcome the typical load transient and AC stability issues in LDO. In other work, the LDO PSRR rating of -73dB @ 16.7MHz, and a relatively low power of 90mW was achieved by [11]. They improve the topology of the classical LDO structure by using double pole-zero cancellation scheme. The LDO design with enhanced PSRR and increased phase margin using the bulk driven transistor technique is presented by [12]. The proposed design achieved -90dB of PSRR. An isolated replica feedback ripple cancellation technique is applied to cancel the power supply noise at the output that is coupled through the main LDO parasitic [13]. The work achieved -42.1dB PSRR at 1MHz. Most of the previous works applied the PSRR improvement techniques without consideration of noise driving through to output of the LDO. A work proposed by [14, 15] claimed to have low output noise, but, the LDO have been utilized a noise free external reference voltage.

In this work, the LDO has been designed to regulate output voltage at 1.8V with the input supply of 3.3V. The operation of the LDO has loop gain higher than 80dB with the phase margin greater than 60º. The proposed LDO is capable to sustain a load current of 120mA targeted for RF energy harvesting system. The design of operational amplifier, BGR and pass element transistor have been included in this work. Besides, in BGR, the NMOS transistor has replaced the BJT to ensure the input differential of error amplifier is in saturated region, hence optimizing the performance of LDO. The analysis of noise is investigated by implementing low pass filter. The rest of the paper is organized as follows. Section 2 describes the LDO architecture. The design of error amplifier and bandgap voltage reference are presented in Section 3. The simulation performance of the design is justified in Section 4. The work is concluded in Section 5.

2. LDO TOPOLOGY

A simple linear voltage regulator consists of a basic control loop where a negative feedback is compared to an internal reference in order to provide a constant voltage regardless of changes or perturbations in the input voltage, temperature, or load current [16-19]. Some of voltage regulator are performed in switching configuration [20]. Figure 1(a) shows a basic block diagram of an LDO regulator. The output voltage, V_{reg} is divided by feedback resistors R1 and R2 to provide the feedback voltage, V_{fb}. V_{fb} is compared to the reference voltage, V_{ref} at the negative input of the error amplifier to supply the gate-drive voltage of the pass transistor. Finally, the error signal drives the output pass transistor to regulate the output voltage. A simplified analysis of noise begins with tracing a subset of the loop represented by a common amplifier variation known as a voltage follower or power buffer [21-25]. This voltage follower circuit forces output voltage to follow V_{ref}. V_{fb} is the error signal referring to V_{ref}. In steady state, V_{reg} is bigger than V_{ref}, which is described as:

$$V_{reg} = V_{ref}(1 + \frac{R_1}{R_2}) \quad (1)$$

where 1 +R1/R2 is the gain that the error amplifier must have to obtain the steady-state output voltage, V_{reg}

The voltage reference is not ideal and has an effective noise factor, $V_{(N)ref}$,on its DC output voltage V_{ref}. Assuming all circuit blocks in Figure 1(a) are ideal, the V_{reg} becomes a function of the noise source. As shown in (1) can be easily modified to account for the noise source, as described:

$$V_{reg} + V_{(N)reg} = V_{ref} + V_{(N)ref}(1 + \frac{R_1}{R_2}) \quad (2)$$

where $V_{(N)reg}$ is the independent noise contribution to the output, and is expressed by:

$$V_{(N)reg} = V_{(N)ref}(1 + \frac{R_1}{R_2}) \quad (3)$$

From (2) and (3), it is clear that a higher output voltage generates higher output noise. The feedback resistors, R1 and R2, set and adjust the output voltage, thereby setting the output noise voltage. For most typical LDO devices, a dominant source of output noise is the amplified reference noise in (3). Figure 1(b) shows a complete block diagram of each equivalent noise source corresponding to its respective circuit element. It illustrates that any device with current flowing through it is a potential noise source. The common technique used to compensate noise in LDO by applying low-pass filter.

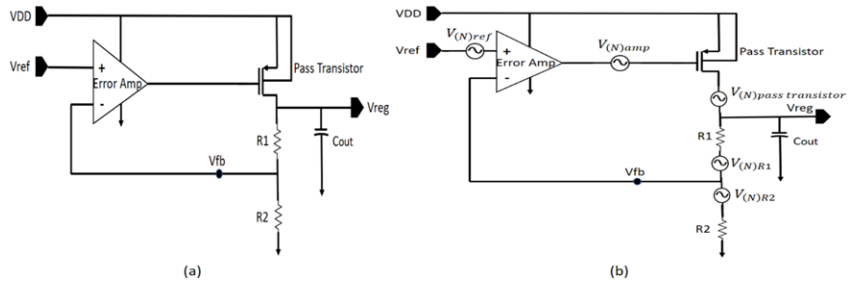


Figure 1. (a) Basic LDO circuit, (b) Noise corresponding in LDO circuit

3. DESIGN OF ERROR AMPLIFIER AND BANDGAP VOLTAGE REFERENCE

Figure 2 is the proposed schematic of the conventional error amplifier. This topology is considered due to its simplicity in terms of designing. The input differential NMOS pair is MN1 and MN2 with MP1 and MP2 as the active load. The second stage is implemented using a common source MP3 and MN5 as a bias current source. In the second stage, the output swing is much better in turning on and off the power transistor [11]. Thus, this design topology performs better and is suitable for low power, low voltage LDO. The current mirrors of MN3, MN4 and MN5 provide the current bias for both stages. I_{ref} is the current coming from a constant bias voltage through the drain of MN4.

The minimum value of the compensation capacitor, C_c is determined by setting the output pole at 2.2 times higher than the gain bandwidth and at 60 degrees phase margin. This condition is a requirement to define the minimum value for C_c where it is placed at or beyond ten times the gain bandwidth. The value of C_c in this design is defined as in [11];

$$C_c = 0.22\ C_L$$

Hence, $C_L = 5pF$;

$$C_c = 1.1pF$$

Assume $C_c = 1pF$

The value for the tail current I_{ref} which will be the output of our constant transconductance current reference is determined based on the slew-rate requirements as:

$$I_3 = SR(C_c)$$
$$I_3 = SR(C_c) > 10x10^6\ x\ (1pF) \quad (4)$$
$$I_3 = 10\mu A$$

Thus;

$$I_3 = I_{ref} = 10\mu A \quad (5)$$

Figure 3 shows the proposed structure of the bandgap voltage reference. The transistors MP4 and MP5 are connected to the differential inputs of the amplifier at node X and Y respectively. The feedback loop exists from the output to the inputs of the operational amplifier. The bandgap needs an operational amplifier of high gain [26]. Due to NMOS input differential has been applied in the proposed error amplifier, this work utilised NMOS transistor to replace the BJT at the node X and Y. This is to ensure the generated Proportional to Absolute Temperature (PTAT) voltage across R_a can provide voltage higher than NMOS threshold voltage. Otherwise, the NMOS input differential is not in saturated region, hence effecting the PSRR of the BGR. The transistor sizing need to be optimized to achive optimum performance [27]. The BGR needs a high gain of error amplifier to gurantee the node X and Y have the same potential across MP4 and MP5. Both of

MP4 and MP5 have the same current, $I_{P1} = I_{P2} = IR_a$. The complementary to absolute temperature (CTAT) current generator is formed by MP6, R_b and $Q1$.

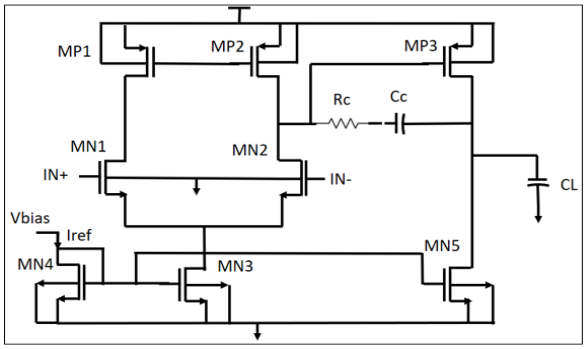


Figure 2. Schematic of the error amplifier

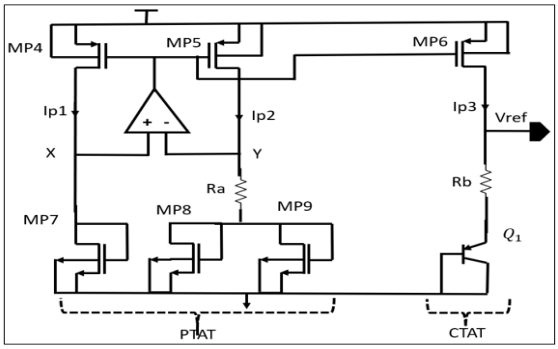


Figure 3. Schematic of proposed bandgap voltage reference

4. RESULTS AND ANALYSIS

Provide The LDO design should have good DC regulation characteristics but the main purpose for the LDO is the ability to supply power as required by system. Table 1 provides the design specification of the proposed LDO. The performance analysis of the amplifier circuit for the gain and phase margin are justified in Figure 4. The proposed design has achieved 92.85dB of gain and 87º of phase margin. The DC open loop gain should be higher under all load conditions to ensure accuracy of the output. The gain achieved is high because the length of common source transistors is optimized to a minimum value. However, higher quiescent current need to be compromised. The unity gain bandwidth of the error amplifier is 12.63MHz and it should be large enough to react fast upon changes of load conditions and input voltages. In this design, two-stage amplifier has been considered instead of the folded cascode amplifier. Two-stage amplifier has better output swing and phase margin, but low PSRR due to the compensation capacitor. For the folded cascode amplifier, it provides better PSSR and gain but difficult to deal with phase margin. Its load capacitor can provide the frequency compensation, but it does not compromise its phase margin.

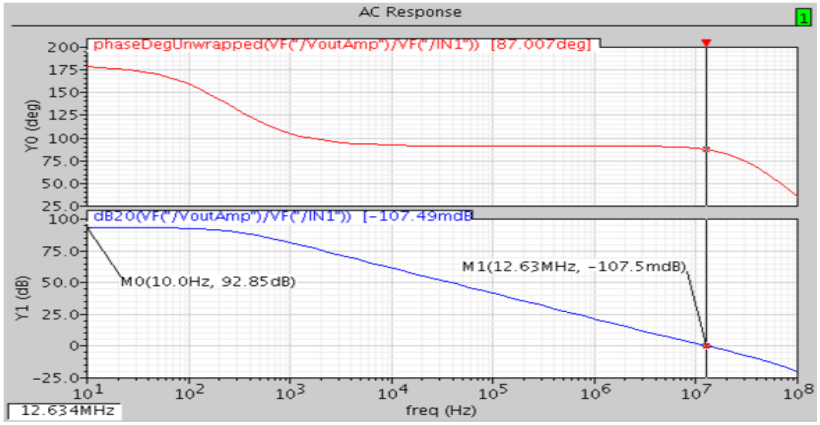


Figure 4. Gain and phase margin of error amplifier

The common mode rejection ratio (CMRR) has been investigated to measure how sensitive is the error amplifier to the changing of the common mode input level. Meanwhile, the PSRR is conducted to observe the performance of error amplifier's ability to eliminate output ripple caused by input variations. Ideally, both parameters should have no effect on the differential gain of the amplifier. However, in reality, these parameters performance could be affected by internal factors and technology as well. Therefore, higher CMRR and PSRR achieves better performance of the error amplifier. The CMRR and PSRR of the proposed design of error amplifier achieved 96.77dB and 76.42dB as shown in Figure 5 and Figure 6 respectively. The performance of error amplifier has been summarized in Table 2.

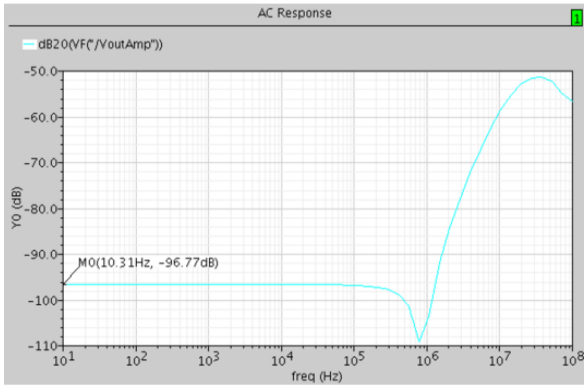


Figure 5. Common mode rejection ratio (CMRR) of error amplifier

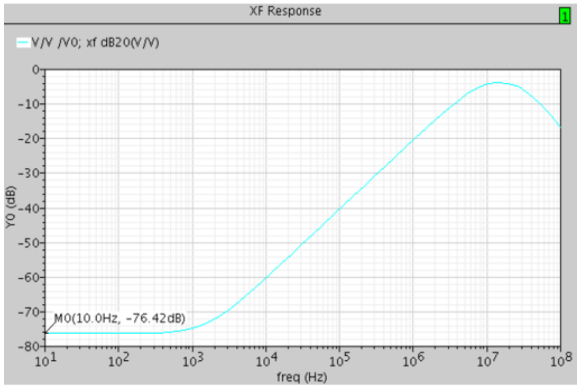


Figure 6. Power supply rejection ratio (PSRR) of error amplifier

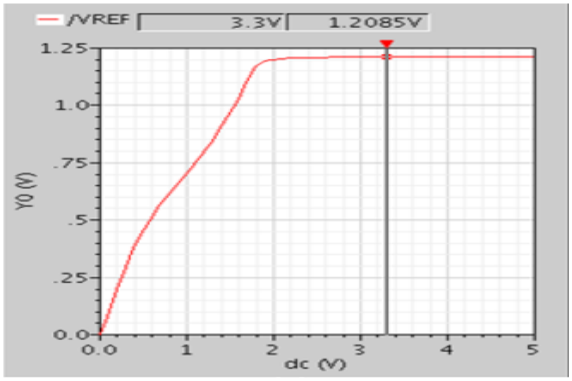
Table 1. The specification of the LDO

Parameter	Value
Input voltage	2.8V-5V
Output Voltage	1.8V
Reference Voltage	1.2V
Open loop gain	>80dB
Phase margin	>60º
Maximum Load Current	120mA
PSRR	>45dB

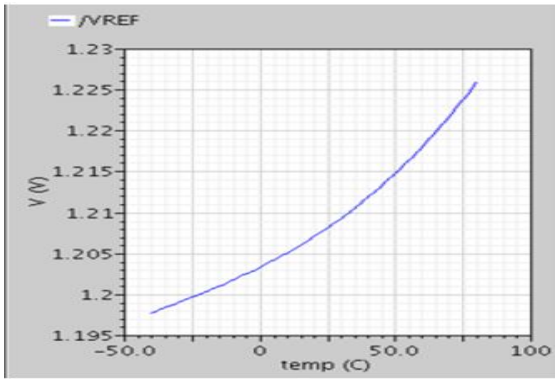
Table 2. Performance summary of error amplifier

Specification	Simulated Result
Open-loop gain	92.85dB
Gain bandwidth	12.25MHz
Phase margin	87.22º
Slew rate	20V/µs
CMRR	96.77dB
PSRR	-76.42dB @10Hz -40dB @100KHz

The analysis of BGR to the voltage variation and temperature coefficient are presented in Figure 7(a) and Figure 7(b) respetively. The sensitivity of the BGR to the temperature is slightly increased when the temperature is increased. The proposed BGR provides 1.2V of reference voltage at 2V–5V of input supply. The PSRR of the BGR is observed at 67.06dB as shown in Figure 8. At this 1Hz-1kHz frequency region, the PSRR depends on the PSRR of the reference amplifier and the open-loop gain.



(a)



(b)

Figure 7. Performance of BGR to, (a) the input voltage variation, (b) the temperature

The line regulation defines how the output behaves under slow change of the input supply. It is basically the steady DC power supply gain of the regulator. As the voltage was swept at the input, the changing value at the output can be observed. Based on the simulation, as the input voltage of LDO is 3.3V, the output voltage delivered is regulated at 1.812V over the 120mA load. Another steady state parameter is load regulation. Since the loop gain is finite, the regulator cannot completely cancel the effect of changing load current. The load regulation of the proposed design of LDO is extended up to 180mA load regulation capability. The purpose is to prepare the effect of parasitic when run post layout simulation.

Parasitic extraction is executed to analyses the effects in both the designed devices and the required wiring interconnects of circuit including parasitic devices. Parasitic capacitance and resistance (R and C) are

extracted from the layout design and then the post layout simulation is performed to compare the performance with pre-layout design. The result of line regulation, load regulation, open-loop gain, phase margin and PSRR are shown in Figure 9 to Figure 13 respectively. The dropout voltage measured in the post-layout simulation rose to 3.1V compare with pre-layout which is 2.79V. The maximum load current drop to 140mA instead of 180mA in pre-layout performance. The gain is dropped to 46.86dB and the phase margin is slightly increase to 79.67º with a slight drop of UGB. This is because of the large size of the pass device, so, the parasitic capacitances in the pass transistor are relatively large. However, the PSRR of post layout is higher than pre-layout performance.

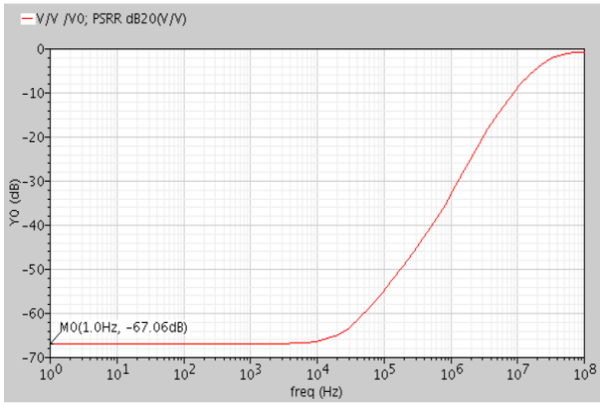


Figure 8. PSRR of bandgap voltage reference

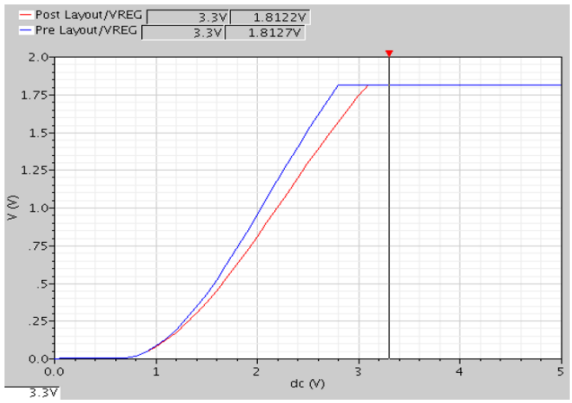


Figure 9. Post-layout of line regulation

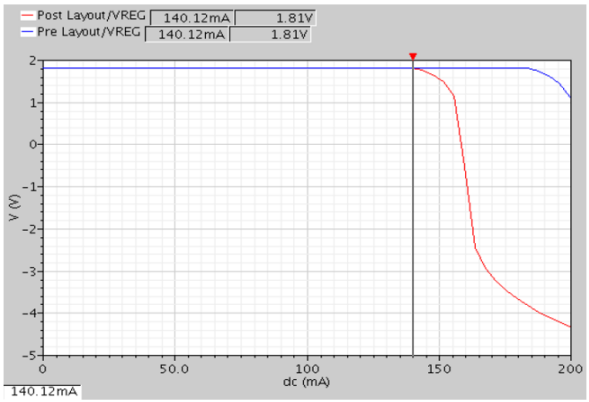


Figure 10. Post-layout of load regulation

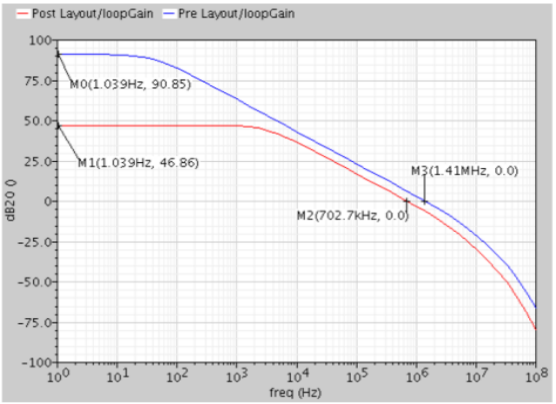


Figure 11. Post-layout of open loop gain

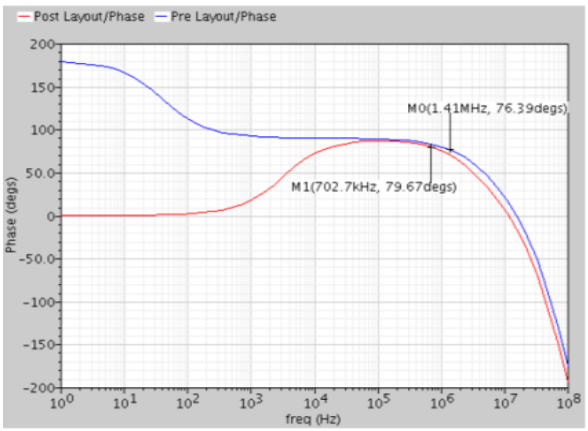


Figure 12. Post-layout of phase margin

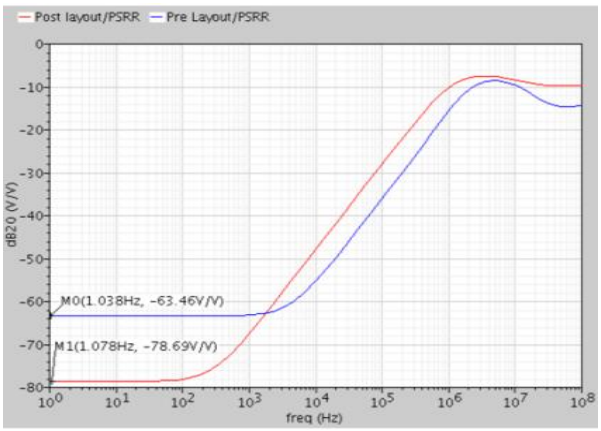


Figure 13. Post-layout of PSRR

The noise is presented in form of noise spectral density curve where the noise of LDO is plotted as $\mu V/sqrt(Hz)$ vs. frequency and the total integrated noise over some bandwidth is calculated in RMS. The PSRR and noise performance of the LDO have been investigated by varying the output capacitor. Beyond the 0dB crossover frequency, the parasitic parameters of the internal and external components along the input to output path has started to dominate. This is including the pass element and the output capacitor with the capacitance of the output capacitor being most significant. Improving the PSRR in this frequency range is typically accomplished by increasing the capacitance of the output capacitor. Figure 14 and Figure 15 show the PSRR and spectral noise density of the LDO when the output capacitor has been swept from 10pF to 10uF. The output noise does not show significant change over the output capacitor. Instead, the change of PSRR is observed at the higher frequency when output capacitor is increased.

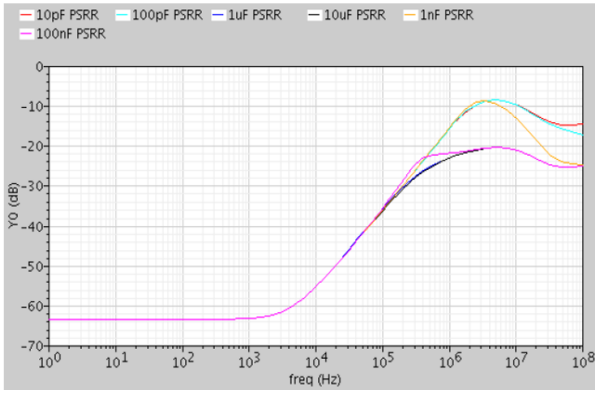


Figure 14. PSRR of LDO when sweep the output capacitor value

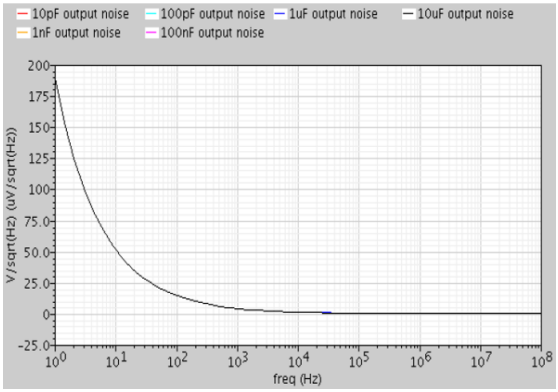


Figure 15. Noise of LDO when sweep the output capacitor value

The low-pass filter has been implemented as shown in Figure 16 to the input reference node of LDO. The purpose is to investigate the effect of PSSR and noise performance. The low pass filter bypasses both the output ripple and output noise to the ground. This prevent noises from propagating to the output of the LDO. The performance of the PSRR and the output noise over the low pass capacitor has been evaluated as shown in Figure 17 and Figure 18 respectively. The output capacitor has been set to 15pF. Based on the result, the higher value of the low-pass capacitor shows a reduction of the output noise and increasing of the PSRR. Figure 19 shows the noise performance calculated in RMS form, relative to the output capacitor and low-pass filter capacitor. It shows that the low-pass filter is a requirement to be applied in the LDO for noise reduction and it depicts that the noise has been dominated by bandgap voltage reference block. Eventually, a good performance could be achieved by using bigger capacitor, but it will not fit for on-chip design which lead to use of external capacitor. Additionally, applying large capacitor negatively impacts the start-up response of the LDO.

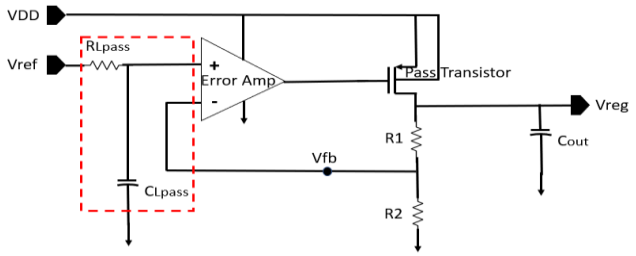


Figure 16. Schematic of low pass filter implementation

Figure 20 shows the layout of the proposed LDO design. The design has been fabricated as shown in Figure 21. The measurement of the fabricated chip is conducted to ensure the LDO is working to regulate the output voltage to 1.8V and able to deliver the desired load current. The line regulation is measured for output voltage and reference voltage by sweeping the input voltage from 0V to 5V. The result is recorded and is shown in Figure 22 and Figure 23. The results show that the regulated output voltage and reference voltage

are obtained approximately at 1.86V and 1.25V respectively. The resistance value is adjusted to verify the load regulation performance by using Ohm's law formula. Based on the result in Figure 24, the maximum measurement load that can be delivered by the LDO is 96mA compared to 140mA in post-layout simulation and 180mA in pre-layout simulation. The main reason dropping in load regulation is because of the high parasitic in the design and losses effected during the measurement is conducted.

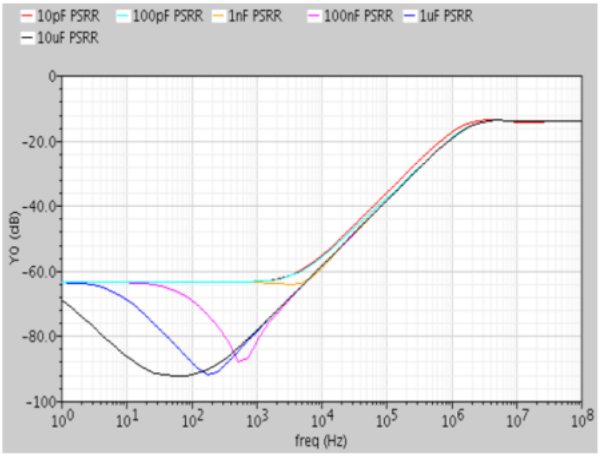


Figure 17. PSRR of LDO when sweep the low-pass capacitor value

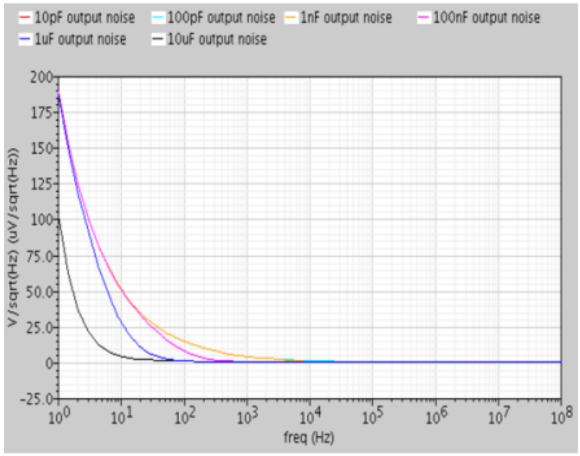


Figure 18. Noise of LDO when sweep the low-pass capacitor value

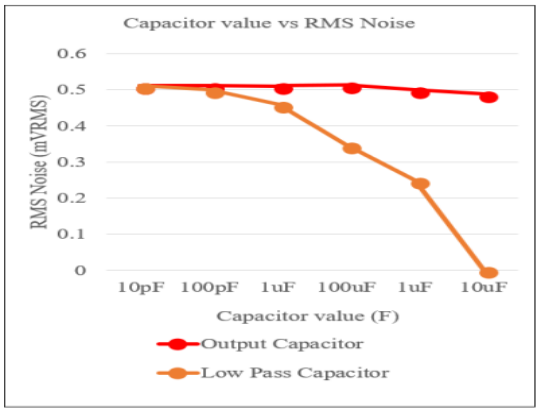


Figure 19. The RMS noise over capacitor size of output capacitor and low pass capacitor

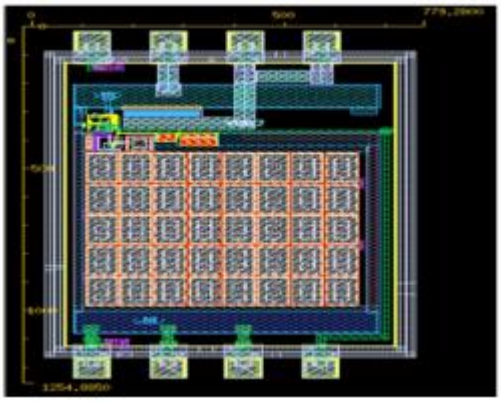


Figure 20. Layout design of proposed LDO

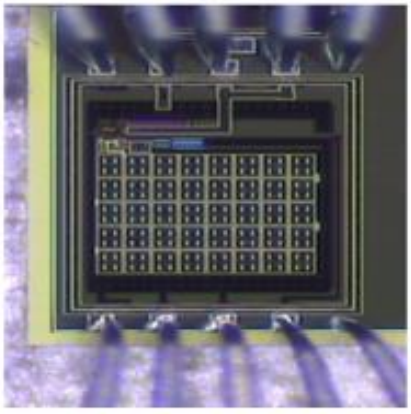


Figure 21. Fabricated chip of proposed LDO

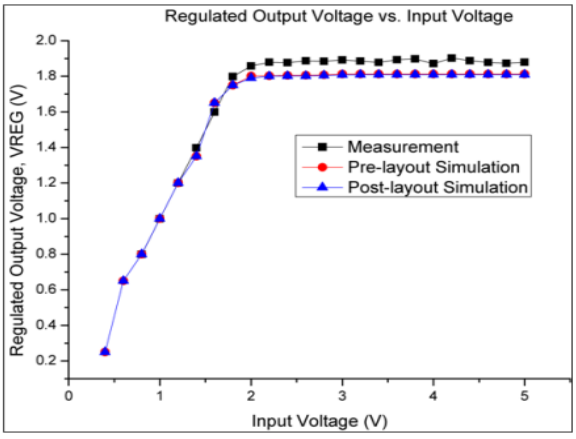


Figure 22. Measurement result of regulated output voltage versus input voltage

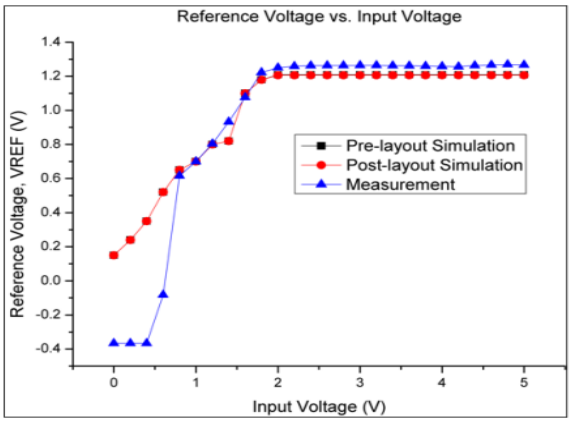


Figure 23. Measurement result of reference voltage versus input voltage

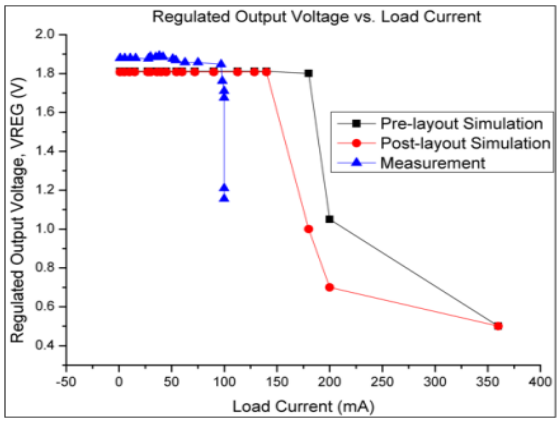


Figure 24. Measurement result of regulated output voltage versus load current

The performance of this work has been summarized and compared with previous work as shown in Table 3. The quiescent current is higher compared to previous work because this work is conducted in 3.3V of input supply voltage. The quiescent current is increased as the supply voltage is increased. For the noise and PSRR performance, some previous work used external reference voltage which leads them to have lower noise and higher PSRR. Instead, this work has proposed an internal reference voltage design. As a consequence, the noise performance is affected as the internal reference circuit is dominating the noise inside the LDO design. The proposed design is used for high load application hence, the power consumption is obtained at 225Mw.

Table 3. Comparison of previous work and performance benchmarking

Specifications	[15]	[14]	[10]	[11]	[28]	[29]	This work
Technology	180nm	500nm	350nm	180nm	180nm	130nm	180nm
Supply voltage	1.8V	2.3-5.5V	1.7V	1.8-3.3V	1.2-1.5V	1.02-2V	3.3V
Quiescent current	55µA	40µA	<61µA	4.41µA	6µA	14-120µA	310µA
Output current	50mA	150mA	50mA	50mA	50mA	300mA	120mA
Dropout voltage	200mV	100mA	<100mV	120mV	200mV	29.7mV	100mV
Output voltage	1.6V	1.2-5.4V	1.2V	1.68V	1V	1V	1.8V
Voltage reference	External	External	External	Internal	External	External	Internal
Line regulation	N/A	24mV	0.073mV	1.66mV/V	23mV	0.44mV/V	24mV/V
Load regulation	0.14mV/mA	0.417mA	0.0042mA	0.0022mA/mA	55mV/mA	1.8mV/mA	5.4mV/mA
Output capacitor	100pF	Capacitor-less	100pF	High	50pF	1uF	15pF
Gain	75dB	159dB	72-92dB	81.7 dB	52.2dB	N/A	90.85dB
Phase margin	50 º	N/A	N/A	63º	75º	N/A	76.39º
Output noise @ 100kHz(µV/√Hz)	0.27	12	N/A	N/A	N/A	N/A	4.224
PSSR	60dB @ 10kHz	-57.7dB @10kHz	-52@1kHz	-72.93 dB	N/A	-50 @10kHz	-63.46dB @ 1kHz/10kHz

5. CONCLUSION

The presented LDO design generates 1.8V of regulated output voltage when input voltage of 2.8V-5V is applied for 120mA load application. The operational amplifier is designed to achieve higher open-loop gain for better performance of BGR and its PSRR. Besides, in BGR, the NMOS transistor has replaced the BJT to ensure the input differential of error amplifier is in saturated region, hence optimizing the performance of LDO. The proposed design has successfully function to provide regulated voltage for 96mA maximum load current. Mismatch of measurement result such as gain and load regulation has been investigated and addressed. Consideration on layout development to address this issue has also been performed. Effect of low-pass filter to reduce the output ripple and grounding the noise from propagating to the input of LDO has been evaluated. The work demonstrates practical design consideration, covering from circuit to post layout and up to measurement results, for better performance of noise and PSRR in LDO design.

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