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IMPLEMENTATION OF SVM FOR CASCADED H-BRIDGE MULTILEVEL INVERTERS UTILIZING FPGA

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Implementation of SVM for Cascaded H-Bridge Multilevel Inverters Utilizing FPGA

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in fulfilment of the requirements for the degree of Master of Electrical Engineering
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DECLARATION

I declare that this project entitled "Implementation of SVM for Cascaded H-Bridge Multilevel Inverters Utilizing FPGA" is the result of my own research except as cited in the references. The project has not been accepted for any degree and is not concurrently submitted in candidature of any other degree.

Signature : .....

Name : Maher Abd Ibrahim Al-jewari

Date : 3/9/2019

APPROVAL

I hereby declare that I have read this project and in my opinion this project is sufficient in terms of scope and quality for the award of Master of Electrical Engineering (Power Electronics and Drives).

Signature : .....

Supervisor Name : Dr. Auzani bin Jidin

Date : 3 SEPTEMBER 2019.

DEDICATION

I would like to present my work to those who did not stop their daily support since I was born, my dear Father, and my kindness Mother, they never hesitate to provide me all the facilities to push me forward as much as they can. This work is a simple and humble reply to their much goodness I have taken over during that time. Thank you for giving me a chance and I love them.

I also dedicate this project to my nephew, sisters who have supported me throughout my life. I always miss and appreciate the memories we had. I love all of you.

ABSTRACT

In recent years the Space Vector Modulation (SVM) technique has gained wide acceptance for many AC drive applications. Further improvements of AC drives can be accomplished by applying SVM in multilevel inverters, since the more suitable voltage vectors can be chosen among larger number of voltage vectors available in the multilevel inverter. However, the use of multilevel inverters associated with SVM by using Digital Signal Processor (DSP) increases the complexity of control algorithm or computational burden and hence produces larger value of sampling time. This thesis reports the implementation of SVM in Cascaded H-Bridge Multilevel Inverter (CHMI) using Field Programmable Gate Arrays (FPGA) and analysis in-depth the performances of SVM computation on THD and fundamental component of output voltage. The SVM modulator is modelled using MATLAB/Simulink, which is sampled at the minimum sampling time, i.e. $DT = 5\ \mu s$. The data of switching signals for driving Insulated Gate Bipolar Transistors (IGBTs) which are stored in MATLAB workspaces, are then used to be programmed in FPGA using a Quartus II software. Note that the generation of switching signals performed by FPGA is at the same sampling time in MATLAB. Using this approach, the computational burden of SVM can be greatly minimized and the desired output voltage can be obtained at high degree of accuracy. The simulation and experiment results are carried out to highlight at the advantages of using SVM and to verify the improvements of this approach by using FPGA controller. Some simulations and experiments were carried out to highlight the improvements, which are as follows; 1) the lower THD of the simulation result is about 14.37% for five-level CHMI and experiment result is about 14.35% for five-level CHMI at modulation index $M_i = 0.9$, 2) the error percentage between the simulation and experimental results of the fundamental output voltage in SVM is small which is approximately less than 1 %, where the minimum error in two-level at $M_i = 0.9$ is around 0.06% and the maximum error in five-level at $M_i = 0.3$ is around 0.52%. The main benefit of this approach is to provide a high precision space vector modulator for cascaded H-bridge multilevel inverter for electric vehicle and Uninterruptible Power Supply (UPS) applications.

ABSTRAK

Dalam beberapa tahun kebelakangan ini, teknik Modulasi Vektor Ruang (SVM) telah mendapat banyak penerimaan untuk kebanyakan aplikasi pemacuan AU. Penambahbaikan lanjutan bagi pemacuan AU boleh dicapai dengan menggunakan SVM dalam penyongsang bertingkat, oleh kerana vektor voltan pensuisan yang lebih sesuai boleh dipilih diantara vektor voltan yang lebih banyak terdapat dalam penyongsang bertingkat. Walau bagaimanapun, penggunaan penyongsang bertingkat yang berkaitan dengan SVM menggunakan Pemproses Isyarat Digital (DSP) meningkatkan kerumitan algoritma kawalan atau beban pengiraan dan seterusnya menghasilkan masa persampelan dengan nilai lebih besar. Tesis ini melaporkan pelaksanaan bagi SVM di dalam Penyongsang Bertingkat Berlata Jejambat Penuh (CHMI) menggunakan FPGA dan analisa mendalam bagi prestasi pengiraan SVM terhadap THD dan komponen asas bagi keluaran voltan. Modulator SVM dimodelkan menggunakan MATLAB/Simulink, yang disampel pada masa pensampelan minimum, iaitu DT = 5 μs. Data bagi isyarat pensuisan untuk memandu IGBTs yang disimpan di dalam ruang kerja MATLAB, kemudiannya digunakan untuk diprogramkan di dalam FPGA menggunakan perisian Quartus II. Ambil perhatian bahawa penjanaan isyarat penukaran yang dilakukan oleh FPGA adalah pada masa persampelan yang sama dengan yang dilakukan di dalam MATLAB. Dengan menggunakan pendekatan ini, beban pengiraan SVM dapat dikurangkan dengan lebih besar dan voltan keluaran yang diinginkan dapat diperolehi dengan ketepatan tinggi. Hasil simulasi dan eksperimen dijalankan untuk menonjolkan kelebihan menggunakan SVM dan untuk mengesahkan penambahbaikan pendekatan ini dengan menggunakan pengawal FPGA. Beberapa simulasi dan eksperimen telah dijalankan untuk menunjukkan penambahbaikan, yang seperti berikut; 1) THD yang lebih rendah daripada keputusan simulasi adalah kira-kira 14.37% untuk lima peringkat CHMI dan keputusan eksperimen adalah kira-kira 14.35% untuk lima peringkat CHMI pada indeks modulasi $M_i = 0.9$, 2) kesilapan peratusan antara simulasi dan eksperimen keputusan bagi komponen asas keluaran voltan dalam SVM adalah kecil iaitu kira-kira kurang daripada 1%, di mana kesilapan yang minimum berlaku dalam dua peringkat pada $M_i = 0.9$ adalah sekitar 0.06% dan ralat maksimum dalam lima peringkat pada $M_i = 0.3$ adalah sekitar 0.52%. Manfaat utama pendekatan ini adalah untuk menyediakan pemodulat vektor ruang berketepatan tinggi bagi penyongsang bertingkat berlata jejambat penuh untuk aplikasi kenderaan elektrik dan Bekalan Kuasa Tidak Terganggu (UPS).

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TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF ABBREVIATIONS

VSI	Voltage source inverter
SPWM	Sinusoidal pulse width modulation
FOC	Field oriented control
DSC	Direct self-control
TD	Sampling time
AC	Alternating current
DC	Direct current
UPS	Uninterruptible power supply
CSI	Current source inverter
HVDC	High voltage direct current
DSP	Digital signal processor
ADC	Analog digital converter
DAC	Digital analog converter
FPGA	Field programmer gate array
SVM	Space vector modulated
UB	Upper band
LB	Lower band
IGBT	Insulated gate bipolar transistor
CHMI	Cascaded H-bridge multilevel inverter
NPCMI	Neutral point clamp multilevel inverter

FCI	Flying capacitor inverter
PWM	Pulse width modulator
THD	Total harmonic distortion
PI	Proportional integral
IPD	In-phase disposition
POD	Phase opposition disposition
APOD	Alternate phase opposition disposition

CHAPTER 1

INTRODUCTION

1.1 Research Background

Voltage Source Inverters (VSI) have evolved as the most popular power conversion for many AC drive applications. The involvement of VSI is in line with the development of various Pulse Width Modulation (PWM) algorithms supported by the advent of solid-state switching device technologies, fast digital signal processors, Field Programmable Gate Arrays (FPGA) and microcontrollers which are used to generate a PWM signals for real-time applications. Since a few decades ago, several PWM algorithms were developed to improve some performances of VSI such as high-power efficiency (Abu Bakar Siddique et al., 2015, Edpuganti and Rathore, 2015, Tong et al., 2015, Youssef et al., 2016), high-output voltage (Carrasco and Silva, 2013, Chai et al., 2016, Jana et al., 2013), and low-total harmonic distortion (THD) (Pramanick et al., 2015, Prieto et al., 2014). Apparently, the research about VSI has not reached to the state of saturation, as novel or simplified PWM methods is still continued to emerge for various topology inverter circuits and multilevel inverters (Gupta et al., 2016, Liu et al., 2016, Lopez et al., 2016, Narimani et al., 2016, Sakthisudhursun et al., 2016, Tan et al., 2016, Yi et al., 2016). Through various types of modulation strategies or PWM methods, a Space Vector Modulation (SVM) technique has received wide acceptance due to several advantages such as higher output voltages, lower THD, high-efficiency and flexible to be implemented in vector control

systems (Chai et al., 2016, Kai et al., 2016, Liu et al., 2016, Thomas et al., 2015, Zheng et al., 2016, Zhifeng et al., 2010).

1.2 Problem Statements

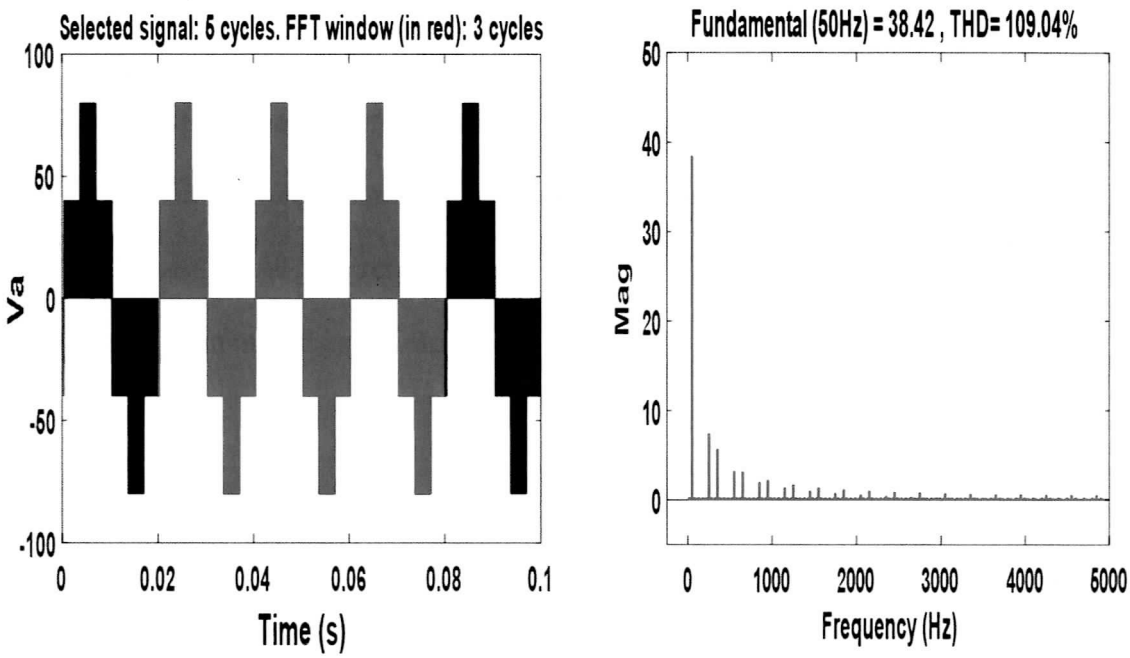
In general, the conventional two-level inverter using Sinusoidal PWM (SPWM) technique poses several problems, as reported in literature review, which can be listed as follows:

- low voltage capability, (Meng et al., 2004, Adeel et al., 2009)
- high rate of change of voltage, i.e. dv/dt , (Meng et al., 2004)
- high Total Harmonic Distortions (THD), (Darshan et al., 2008)
- large size of filter,(Adeel et al., 2009)
- low output voltage, i.e. SPWM technique cannot fully utilize the DC link voltage V_{dc}, (Meng et al., 2004)

The use of two-level inverter is somehow not suitable for high voltage applications because the switching devices may suffer from voltage stress and hard switching introduced (Das and Narayanan, 2012), particularly at high switching frequency operations. In two-level inverter, the number of voltage vectors is limited to eight, i.e. two zero vectors (with zero magnitude) and six active vectors (each vector has the same magnitude of $(2V_{dc}/3)$) , hence, the switching of the vectors might lead to larger dv/dt and higher harmonic distortions. Therefore, large size of filter is required to eliminate the harmonics in obtaining high-quality of AC voltage waves, i.e. close to sinusoidal wave. In addition, the output voltage obtained in SPWM technique cannot be extended until the six-step voltage achieves excellent dynamic control and improves power output of electrical drive systems. The implementation of SPWM is also not suitable for vector control of induction motor, as the technique needs to control three-phase quantities which are not flexible to improve dynamic performances.

Ultimately, all the above problems can be minimized by employing SVM technique in multilevel inverters.

However, to implement the SVM technique with multilevel inverter is not as easy as two - level inverters. The increment number of inverter levels will increase the complexity of SVM equation which contributes to computational processing burden. This thesis emphasized the potentials errors in computing the SVM algorithms because of larger sampling time and DSP controller using during the implementation of hardware. That will produce inappropriate output voltage which may lead to higher THD and lower fundamental. The higher THD and lower fundamental can be demonstrated by simulation results as shown in Figure 1.1. In this case, the sampling time of space vector modulator was set to a larger value, i.e. $DT = 50\mu s$ and DSP controller. The simulation results showed that a larger value of sampling time utilized a two-level inverter because the phase voltage had a 109.04% THD and 38.42V fundamental output voltage. Obviously, the higher THD and lower fundamental output voltage resulted because of larger sampling time and DSP controller. Moreover, it also caused the space vector modulator to produce inappropriate switching vectors; where the phase voltage was distorted.



(a) (b)

Figure 1.1: Simulation Results of FFT analysis for (a) Phase Voltage (b) THD% and Fundamental Phase Voltage

1.3 Objectives of Research

The main objectives of the thesis are as follows:

i. To develop the SVM technique for two-level, three-level and five-level inverter.

i. To implement the SVM technique for multilevel inverter by using FPGA controller with minimum sampling time.

ii. To investigate the performance of five-level inverter for the minimization of total harmonic distortion (THD) of the output voltage.

1.4 Scopes of Work

The scopes of work involve evaluating performances and verifying improvements of using multilevel inverters to investigate the performance effect of SVM with various levels of inverters and sampling times. In addition, the most practical and acceptable SVM technique for multilevel inverter is also implemented. Then, the improvements are validated through simulation or/and experimental results.

1.6 Thesis Contributions

This thesis evaluates the performances of the total harmonic distortion (THD), the fundamental output voltage for two-level inverter, three-level and five-level Cascaded H-Bridge Multilevel Inverters (CHMI). The Space Vector Modulation (SVM) is used through simulation and experimental results. This thesis will reveal that the computational burden of SVM algorithm can be minimized and it is possible to be implemented, minimum sampling time. The contributions of the thesis are as follows:

I. revealing the potential errors in executing SVM algorithms because of poor linearity and larger sampling time which can be restricted by employing a greater number of inverter levels. The results show that the error obtained in the five-level cascaded H-Bridge multilevel inverters (CHMI) is restricted to one-sixteen of that obtained in two-level inverter, in other words, the error reduction is 93.75% from that resulted in the two-level inverter,

II. highlighting the restriction of error in multilevel inverters (e.g. five-level CHMI), giving a minimum of THD voltage. If the larger sampling time should be used, due to limitation of processor and computation of complex control algorithm, it is suggested that greater number of inverter levels are employed to gain slightly small and acceptable error,