Faculty of Electrical Engineering

IMPLEMENTATION OF NEAREST LEVEL CONTROL METHOD FOR SINGLE-PHASE TRANSISTOR-CLAMPED H-BRIDGE MULTILEVEL INVERTER

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WAIL ALI ALI SALEH

A thesis submitted
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DECLARATION

I declare that this thesis entitled "Implementation of Nearest Level Control Method for Single-Phase Transistor-Clamped H-Bridge Multilevel Inverter**"** is the result of my own research except as cited in the references. The thesis has not been accepted for any degree and is not concurrently submitted in candidature of any other degree.

Signature : .....

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APPROVAL

I hereby declare that I have read this thesis and in my opinion this thesis is sufficient in terms of scope and quality for the award of Master of Science in Electrical Engineering.

Signature :……...

Supervisor Name : Dr. Nurul Ain Mohd Said

Date :……...

DEDICATION

I dedicate this work to my beloved parents and family for their endless love, support, encouragement and sacrifices.

I also dedicate this work to my best friend, Mr. Md Nazmul Islam Sarkar, for his support, encouragement and guidance.

ABSTRACT

Multilevel Inverters (MLIs) are gaining particular interest among researchers and in the industrial sector owing to their widespread applications and numerous features. Transistor-Clamped H-Bridge (TCHB) MLI has received increasing research attention due to its advantage in producing high-quality output using a reduced number of switches and DC voltage sources compared with other conventional MLI topologies. With regard to the modulation technique, High Switching Frequency (HSF) modulations suffer from high switching losses, making them unsuitable for high-power applications. For such applications, Low Switching Frequency (LSF) modulations, such as Nearest Level Control (NLC), are more efficient as they operate at low frequency and thus reduce switching losses significantly. NLC is a simple method in its concept and implementation. The main aim of this study is to implement the proposed NLC method to a single-phase TCHB MLI with symmetrical and asymmetrical DC voltage sources and to evaluate its Total Harmonic Distortion (THD) minimization. Two topologies of the TCHB MLI are investigated in this study, which are nine-level symmetrical and thirteen-level asymmetrical TCHB inverters. Adopting an asymmetry for the DC voltage sources of the MLI results in a higher number of output levels. The selected voltage ratio of the DC sources in the asymmetrical topology is 1: 2. The adopted topologies and the proposed control method are modeled through simulations in Matlab/Simulink. The simulation results are verified through experimental tests using an Altera Field-Programmable Gate Array (FPGA). The results show that the topologies and the proposed control method are efficient in achieving high-quality output with an improved THD. The minimum voltage THDs obtained from the experiments are below 8.1 % for the nine-level inverter and below 5.3% for the thirteen-level inverter for different types of load, which almost comply with IEEE Standard 519-2014. The simulation results are in close agreement with the experimental ones. It is concluded that the NLC performs more efficiently for inverters with a higher number of levels and produces better THD results compared with other LSF modulations.

PELAKSANAAN KAEDAH ARAS KAWALAN YANG TERDEKAT UNTUK PENYONGSANG BERTINGKAT TRANSISTOR-DIAPIT JEJAMBAT-H SATU FASA

ABSTRAK

Penyongsang-penyongsang bertingkat memperoleh minat khusus di kalangan penyelidik dan dalam sektor industri kerana penggunaannya yang meluas dan pelbagai ciri. Penyongsang bertingkat transistor-diapit jejambat-H telah mendapat perhatian penyelidikan kerana kelebihannya dalam menghasilkan keluaran yang berkualiti tinggi dengan menggunakan bilangan suis dan sumber voltan arus terus (AT) yang kurang berbanding dengan topologi penyongsang bertingkat lazim yang lain. Merujuk kepada modulasi, modulasi frekuensi pensuisan tinggi mengalami kehilangan pensuisan yang tinggi, membuatkan nya tidak sesuai untuk aplikasi-aplikasi berkuasa tinggi. Untuk aplikasi-aplikasi sedemikian, modulasi frekuensi pensuisan rendah, seperti kawalan aras terhampir adalah lebih cekap kerana ia beroperasi pada frekuensi rendah dan dengan itu dapat mengurangkan kehilangan pensuisan dengan ketara. Kawalan aras terhampir adalah satu kaedah yang mudah dalam konsep dan pelaksanaannya. Tujuan utama kajian ini adalah untuk melaksanakan kaedah kawalan aras terhampir yang dicadangkan kepada penyongsang bertingkat transistor-diapit jejambat-H satu fasa dengan sumber-sumber bekalan voltan AT simetri dan tidak simetri dan untuk menilai peminimuman jumlah herotan harmonik. Dua topologi daripada penyongsang bertingkat transistor-diapit jejambat-H diteliti dalam kajian ini, iaitu penyongsang-penyongsang transistor-diapit jejambat-H sembilan tingkat simetri dan tiga belas tingkat tidak simetri. Penggunaan sumber voltan AT tidak simetri menghasilkan bilangan tingkat keluaran yang lebih tinggi. Nisbah sumber voltan AT yang dipilih dalam topologi tidak simetri adalah 1: 2. Topologi-topologi yang digunakan dan kaedah kawalan yang dicadangkan dimodelkan melalui simulasi di dalam Matlab/Simulink, dan hasil simulasi disahkan melalui eksperimen menggunakan tatasusunan get boleh aturcara medan ALTERA. Keputusan menunjukkan bahawa topologi dan kaedah modulasi yang dicadangkan adalah cekap dalam mendapatkan satu keluaran berkualiti tinggi dengan jumlah herotan harmonik yang lebih baik. Jumlah herotan harmonik voltan terendah yang diperoleh daripada eksperimen adalah di bawah 8.1 % untuk penyongsang sembilan tingkat dan di bawah 5.3% untuk penyongsang tiga belas tingkat untuk pelbagai jenis beban, yang hampir mematuhi Piawai IEEE 519-2014. Hasil simulasi sangat hampir dengan hasil eksperimen. Disimpulkan bahawa kaedah kawalan aras terhampir berfungsi dengan lebih cekap untuk penyongsang dengan jumlah tingkat lebih tinggi dan menghasilkan keputusan-keputusan jumlah herotan harmonik yang lebih baik berbanding dengan modulasi frekuensi pensuisan rendah yang lain.

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LIST OF ABBREVIATIONS

APOD	-	Alternate Phase Opposition Disposition
A-TCHB	-	Asymmetrical Transistor-Clamped H-Bridge
CHB	-	Cascaded H-Bridge
CSI	-	Current Source Inverter
DRSC		Double Reference Single Carrier
FACTS	-	Flexible AC Transmissions
FC	-	Flying Capacitor
FPGA	-	Field Programmable Gate Array
GA	-	Genetic Algorithm
HDL	-	Hardware Description Language
HSF		High Switching Frequency
HVDC	-	High Voltage Direct Current
IGBT	-	Isolated Gate Bipolar Transistor
LSF		Low Switching Frequency
LSPWM	-	Level-Shifted Pulse Width Modulation
LUT	-	Look-up Table
MCPWM	-	Multicarrier Pulse Width Modulation
MLI	-	Multilevel Inverter
MMC	-	Modular Multilevel Converter
mNLM	-	Modified Nearest Level Modulation

MOSFET	-	Metal Oxide Silicon Field Effect Transistor
MRPWM	-	Multireference Pulse Width Modulation
NLC	-	Nearest Level Control
NPC	-	Neutral Point Clamped
NR	-	Newton Raphson
NVC	-	Nearest Vector Control
OHSW	-	Optimized Harmonic Stepped Waveform
OMTHD	-	Optimized Minimization of the Total Harmonic Elimination
PD	-	Phase Disposition
PI	-	Proportional Integral
POD	-	Phase Opposition Disposition
PSO	-	Particle Swarm Optimization
PSPWM	-	Phase-Shifted Pulse Width Modulation
PV	-	Photovoltaic
RMS	-	Root Mean Square
SHE	-	Selective Harmonic Elimination
SPWM	-	Sinusoidal Pulse Width Modulation
STATCOM	-	Static Synchronous Compensator
SVPWM	-	Space Vector Pulse Width Modulation
TCC	-	Transistor Clamped Converter
TCHB	-	Transistor-Clamped H-Bridge
THD	-	Total Harmonic Distortion
VHDL	-	Very High Speed Integrated Circuit Hardware Description Language
VSI	-	Voltage Source Inverter

LIST OF APPENDICES

LIST OF PUBLICATIONS

Saleh, W. A. A., Said, N. A. M. and Halim, W. A., 2020. Harmonic minimization of a single-phase asymmetrical TCHB multilevel inverter based on nearest level control method. *International Journal of Power Electronics and Drive System (IJPEDS)*, 11(3), pp. 1406–1414.

Said, N. A. M., Saleh, W. A. A. and Halim, W. A., 2020. Voltage harmonics reduction in single phase 9-level transistor clamped H-bridge inverter using nearest level control method. *Indonesian Journal of Electrical Engineering and Computer Science (IJEECS)*, 20(3), pp. 1725–1732.

CHAPTER 1

INTRODUCTION

1.1 Introduction

This chapter serves as an introduction to the research work. It outlines the background, motivation and contribution of the research work. The problem statement, research objectives and research methodology are explained. An outline of the thesis chapters is presented at the end of this chapter.

1.2 Research background

With the increase in renewable energy sources in recent years, such as solar cells, wind energy and fuel cells, there is a high demand for power electronics converters. Renewable energy is available in DC form and needs to be converted into AC in order to be fed into the grid or to power the AC based devices. The inverters are used for this type of conversion. Two-level inverters are commonly used in a wide range of industrial applications; however, they suffer from some disadvantages, which include high harmonic distortion and high switching losses (Rodriguez et al., 2009). Typically, in order to reduce the harmonic distortion, large-sized filters are used, making the system looks bulky. MLI has therefore been developed as a solution to this problem. They have more advantages as compared with two-level inverters such as higher voltage operating capability, less harmonic contents, smaller filter size, etc.(Rodriguez et al., 2009). MLI generates a staircase output voltage that becomes almost sinusoidal with the increase in the number of output levels.