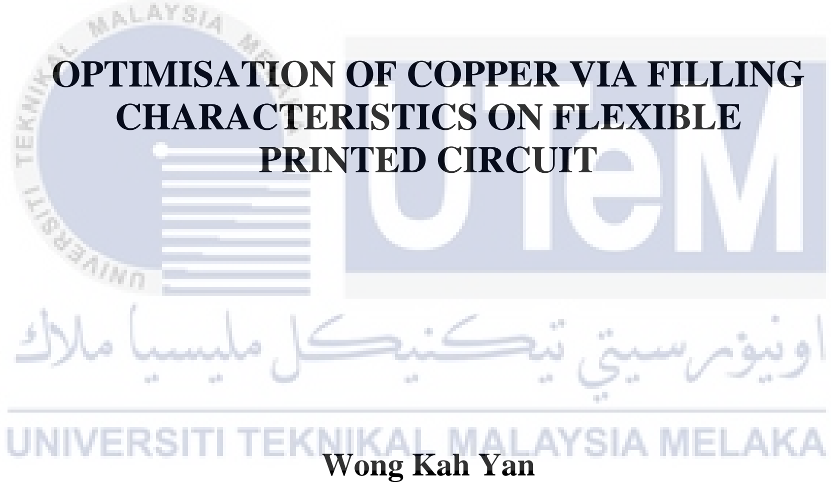
# Faculty of Manufacturing Engineering



## OPTIMISATION OF COPPER VIA FILLING CHARACTERISTICS ON FLEXIBLE PRINTED CIRCUIT

**Wong Kah Yan**

**Master of Science in Manufacturing Engineering**

**2021**

# OPTIMISATION OF COPPER VIA FILLING CHARACTERISTICS ON FLEXIBLE PRINTED CIRCUIT

**WONG KAH YAN**

**A thesis submitted**
**in fulfilment of the requirements for the degree of Master of Science**
**in Manufacturing Engineering**

اونيؤرسيتي تيكنيكل مليسيا ملاك
UNIVERSITI TEKNIKAL MALAYSIA MELAKA

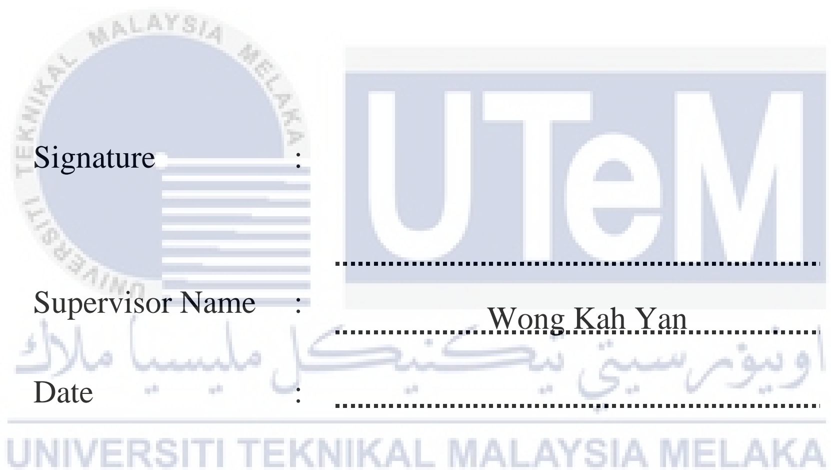
**Faculty of Manufacturing Engineering**

**UNIVERSITI TEKNIKAL MALAYSIA MELAKA**

**2021**

## DECLARATION

I declare that this thesis entitled "Optimisation of Copper Via Filling Characteristics on Flexible Printed Circuit" is the result of my own research except as cited in the references. The thesis has not been accepted for any degree and is not concurrently submitted in candidature of any other degree.




Signature : ..........................................................

Supervisor Name : Wong Kah Yan

Date : ..........................................................

**APPROVAL**

I hereby declare that I have read this thesis and in my opinion this thesis is sufficient in terms of scope and quality for the award of Master of Science in Manufacturing Engineering.

Signature : ......................................................

Supervisor Name : Associate Professor Dr. Liew Pay Jun

Date : ......................................................

**DEDICATION**

To my beloved one.

# ABSTRACT

Within electronics industry, flexible printed circuits (FPC) are compiled in stacks to achieve smaller sizes and higher component density. The architecture size of a computer processor has been shrunk from 10 µm to 7 nm from year 1971 to 2020. In order to meet the market expectation, manufacturers have to decrease the device size while maintain the product performance. However, the shrinking of device could potentially lead to higher failure rates and lower production yields. If the process is not optimise, the yields of the process will become lower as the device size shrink year by year. Therefore, the optimisation of the copper via filling process plays a very crucial role in manufacturing quality and defectless FPC. In this research, the effects of the electroplating copper via filling parameters (current density ($I_d$), fluid flow rate (Q) and filling time ($t_f$)) on the filling characteristics of copper filled micro via (surface thickness, dimple depth and via filling ratio) were investigated and optimized in the study. A Box-Behnken design response surface methodology (BBD RSM) matrix created by Minitab software was used to determine the parameter effects and the optimum parameters of this study. The process was carried out by using the copper via filing machine that was customize for the experiment whereas the electrolytes used in the experiment were according to the industry standard. The findings yielded that current density was significant to surface thickness, whereas fluid flow rate was significant to the dimple depth and via filling ratio. Apart from that, the optimum parameter to achieve thin surface thickness, low dimple depth and high via filling ratio were $I_d$ = 1.5 A/dm$^2$, Q = 25 m$^3$/h and $t_f$ = 60 minutes. The main mechanism affecting the via filling characteristics using fluid flow rate was changing the mass transfer of the electrolyte, whereas filling time and current density affected the filling characteristic by controlling the amount of electron supply to the cathode.

UNIVERSITI TEKNIKAL MALAYSIA MELAKA

# *PENGOPTIMUMAN CIRI-CIRI PENGISIAN LUBANG KUPRUM DALAM LITAR BERCETAK FLEKSIBEL*

## *ABSTRAK*

*Dalam industri elektronik, litar bercetak fleksibel (FPC) disusun dalam timbunan untuk mendapatkan saiz yang lebih kecil dan kepadatan komponen yang lebih tinggi. Ukuran seni bina pemproses komputer telah menyusut dari 10 µm hingga 7 nm dari tahun 1971 hingga 2020. Untuk memenuhi jangkaan pasaran, pengeluar perlu mengecilkan saiz peranti dan mengkekalkan prestasi produk pada masa yang sama. Malah, Pengecutan peranti berpotensi menyebabkan kadar kegagalan yang lebih tinggi dengan hasil pengeluaran yang lebih rendah. Sekiranya proses tidak dioptimumkan, hasil proses akan menjadi lebih rendah apabila saiz peranti menyusut dari tahun ke tahun. Oleh itu, pengoptimuman proses pengisian lubang kuprum memainkan peranan yang sangat penting dalam menghasilkan FPC yang berkualiti dan tanpa sebarang kerosakan. Dalam penyelidikan ini, kesan parameter proses pengisian (kepadatan arus (Id), kadar aliran bendalir (Q) dan masa pengisian (tf)) terhadap ciri-ciri pengisian lubang bersaiz mikro (ketebalan permukaan, kedalaman lekuk dan nisbah pengisian lubang mati) telah dikaji dan dioptimumkan semasa kajian ini dilakukan. Matriks Box-Behnken design response surface methodology (BBD RSM) yang disediakan didalam Minitab telah digunakan untuk menentukan kesan parameter dan parameter optimum daripada kajian ini. Proses tersebut dilakukan dengan menggunakan mesin pengisian lubang kuprum yang disesuaikan untuk kajian ini dan elektrolit yang digunakan dalam eksperimen ini adalah mengikut piawaian industri. Hasil kajian menunjukkan bahawa kepadatan arus signifikan terhadap ketebalan permukaan, sedangkan kadar aliran bendalir signifikan terhadap kedalaman lekuk dan nisbah pengisian lubang mati. Selain itu, parameter optimum yang boleh mencapai ketebalan permukaan yang nipis, kedalaman lekuk yang rendah dan nisbah pengisian lubang yang tinggi adalah Id = 1.5 A/dm2, Q = 25 m3/jam dan tf = 60 minit. Mekanisme utama yang mempengaruhi ciri pengisian lubang kuprum menggunakan kadar aliran bendalir adalah mengubah pemindahan massa elektrolit, apabila masa pengisian dan kepadatan arus mempengaruhi ciri pengisian dengan mengawal jumlah bekalan elektron ke katod.*

UNIVERSITI TEKNIKAL MALAYSIA MELAKA

## ACKNOWLEDGEMENTS

My heartfelt gratitude to my supervisor Associate Professor Dr. Liew Pay Jun from the Faculty of Manufacturing Engineering, Universiti Teknikal Malaysia Melaka (UTeM) for the guidance during my Master career.

I would like to express my appreciation to my co-supervisor, Associate Professor Dr. Lau Kok Tee from the Faculty of Mechanical and Manufacturing Engineering Technology, Universiti Teknikal Malaysia Melaka (UTeM) for his advice and suggestion which always enlighten me during the process of study.

I also extend my appreciation to the MFS Technology (M) Sdn. Bhd on their ceaseless support in terms of material, equipment and knowledge. This research will not be realized without their assistance and efforts in the production line.

Last but not least, I would also like to express my deepest gratitude to my beloved one, my father and mother, my grandfather and late grandmother. Thanks for their love and support throughout my life and my entire study.

UTeM
اونيۏرسيتي تيكنيكل مليسيا ملاك
UNIVERSITI TEKNIKAL MALAYSIA MELAKA

## TABLE OF CONTENTS


| | PAGE |
|---|---|
| **DECLARATION** | |
| **APPROVAL** | |
| **DEDICATION** | |
| **ABSTRACT** | **i** |
| ***ABSTRAK*** | **ii** |
| **ACKNOWLEDGEMENTS** | **iii** |
| **TABLE OF CONTENTS** | **iv** |
| **LIST OF TABLES** | **vii** |
| **LIST OF FIGURES** | **viii** |
| **LIST OF APPENDICES** | **x** |
| **LIST OF ABBREVIATIONS** | **xi** |
| **LIST OF SYMBOLS** | **xii** |
| **LIST OF PUBLICATIONS** | **xiii** |
| **CHAPTER** | |
| **1. INTRODUCTION** | **1** |
| 1.1 Research background | 1 |
| 1.2 Problem statement | 3 |
| 1.3 Research objectives | 5 |
| 1.4 Scope | 5 |
| 1.5 Research significance | 6 |
| 1.6 Research outline | 6 |
| **2. LITERATURE REVIEW** | **7** |
| 2.1 Flexible printed circuit (FPC) | 7 |
| 2.1.1 Type of FPC | 9 |
| 2.2 Properties of via | 10 |
| 2.2.1 Types of via | 10 |
| 2.2.2 Diameter of the via | 10 |
| 2.2.3 Via aspect ratio | 12 |
| 2.3 Copper via filling | 14 |
| 2.3.1 Electroplated copper via filling | 15 |
| 2.3.2 Electroless copper via filling | 17 |
| 2.4 Via filling parameters | 18 |
| 2.4.1 Solution flow and agitation | 18 |
| 2.4.2 Filling time | 21 |
| 2.4.3 Current density | 22 |
| 2.5 Chemical solution parameter | 25 |
| 2.5.1 Acidity of the electrolyte solution | 25 |
| 2.5.2 Concentration of brightener | 26 |
| 2.5.3 Concentration of suppressor | 27 |
| 2.5.4 Concentration of leveller | 29 |
| 2.5.5 Concentration of chlorine (Cl) | 30 |
| 2.6 Defect of copper via filling | 32 |
| 2.6.1 Void | 32 |
| 2.6.2 Dimple | 33 |


UTeM
UNIVERSITI TEKNIKAL MALAYSIA MELAKA

2.6.3 Bumps 34
2.6.4 Seam 35
2.7 Via filling characteristics 36
2.7.1 Surface thickness 36
2.7.2 Dimple depth 37
2.7.3 Via filling ratio 37
2.8 Design of experiment (DoE) 38
2.8.1 Factorial method 38
2.8.2 Taguchi method 39
2.8.3 Response surface methodology (RSM) 40
2.9 Summary 44

**3. METHODOLOGY 48**
3.1 Gantt chart 48
3.2 Flow chart 48
3.3 Experimental method and procedure 50
3.3.1 Preparation of electrolyte 50
3.3.2 Workpiece material 51
3.3.3 FPC preparation 52
3.3.4 Design of experiment (DoE) 55
3.3.5 Machine structure and layout 58
3.3.6 Via filing machine 60
3.3.7 Machine setting 60
3.3.8 Collection of FPC sample 64
3.4 Measurement and data collection 64
3.4.1 Sample cross section fabrication 64
3.4.2 Data collection of surface thickness, dimple depth and via filling ratio 66
3.5 Summary 68

**4. RESULTS AND DISCUSSION 69**
4.1 Effect of parameters to the filling characteristic of copper filled via 69
4.1.1 Cross section of the via 69
4.1.2 Surface thickness 72
4.1.3 Dimple depth 79
4.1.4 Via filling ratio 87
4.2 Optimisation and validation test of the via filling parameters 94
4.2.1 Prediction of the optimum parameters 94
4.2.2 Validation test 95
4.3 Mechanism of copper via filling 97
4.3.1 Effect of fluid flow rate 97
4.3.2 Effect of filling time and current density 99
4.4 Summary 100

**5. CONCLUSION AND RECOMMENDATIONS 101**
5.1 Conclusions 101
5.2 Recommendations 103
5.3 Sustainability element 103
5.4 Complexity of the study 104

UTeM
اونيورسيتي تيكنيكل مليسيا ملاك
UNIVERSITI TEKNIKAL MALAYSIA MELAKA

| | |
|---|---|
| **REFERENCES** | **105** |
| **APPENDIX A** | **121** |

## LIST OF TABLES


| TABLE | TITLE | PAGE |
|---|---|---|
| 2.1 | Summary of via diameter used by previous researchers | 12 |
| 2.2 | Summary of the via dimension used by previous researchers | 13 |
| 2.3 | Summary of agitation type used by previous researchers | 21 |
| 2.4 | Summary of different current density used by previous researchers | 25 |
| 2.5 | Summary of brightener concentration used by previous researchers | 27 |
| 2.6 | Summary of suppressor concentration used by previous researchers | 29 |
| 2.7 | Summary of leveller concentration used by previous researchers | 30 |
| 2.8 | Summary of chlorine concentration used by previous researcher | 32 |
| 2.9 | Summary of outcome of previous research | 44 |
| 3.1 | Name of chemical required and their concentration in the filling bath | 50 |
| 3.2 | The properties of FPC and drilled via | 53 |
| 3.3 | Experimental parameters setup of the DoE matrix | 56 |
| 3.4 | DoE matrix | 57 |
| 4.1 | Result of the surface thickness | 73 |
| 4.2 | ANOVA of surface thickness | 74 |
| 4.3 | Model summary of surface thickness | 75 |
| 4.4 | DoE matrix with dimple depth | 80 |
| 4.5 | ANOVA of dimple depth before model reduction | 81 |
| 4.6 | ANOVA of dimple depth after model reduction | 82 |
| 4.7 | Model summary of dimple depth | 83 |
| 4.8 | DoE matrix with via filling ratio | 88 |
| 4.9 | ANOVA of via filling ratio | 89 |
| 4.10 | Model summary of via filling ratio | 90 |
| 4.11 | Optimisation goal for the optimum parameters | 95 |
| 4.12 | Summary of the optimisation plot | 95 |
| 4.13 | Results of validation test | 96 |


UNIVERSITI TEKNIKAL MALAYSIA MELAKA

## LIST OF FIGURES


| FIGURE | TITLE | PAGE |
|---|---|---|
| 2.1 | The illustration of Ducas's printed circuit (Ducas, 1925) | 8 |
| 2.2 | Cesar Parolini's circuit board (Petherbridge et al., 2005) | 9 |
| 2.3 | Through hole and blind via (Allpcb, 2018) | 10 |
| 2.4 | The effect of diffusion time on bottom up filling (Ma et al., 2013) | 11 |
| 2.5 | Formation of copper via filling in (a) 0 min; (b) 15 min; (c) 30 min and (d) 45 min (Wang et al., 2014a) | 15 |
| 2.6 | The schematic diagram of electroplating via filling (Raval and Solanki, 2013) | 16 |
| 2.7 | The schematic diagram of electroless via filling (Raval and Solanki, 2013) | 17 |
| 2.8 | Via filling ratio versus power of ultrasonic (Wang et al., 2020) | 20 |
| 2.9 | Simulation result of copper deposition in 10 µm diameter via with different via aspect ratio (upper: 2, lower: 4) (Braun et al., 2020). | 22 |
| 2.10 | Current density versus via filling ratio (Wang et al., 2017c) | 23 |
| 2.11 | Cross section of via filling under different current density; (a) 0.5 $A/dm^2$; (b) 0.1 $A/dm^2$ (Miao et al., 2012) | 24 |
| 2.12 | Schematic sketch of copper via filling process (Li et al., 2009a) | 30 |
| 2.13 | The cross-sectional images of through silicon via (a) without pretreatment (b) pretreated by ultrasound vibration and (c) pretreated by vacuuming method (Li et al., 2013) | 33 |
| 2.14 | Image of void and dimple in the via filling (Tang et al., 2017) | 34 |
| 2.15 | The image of bump | 35 |
| 2.16 | Seam formation in a through via filling (Roelfs et al., 2012) | 36 |
| 2.17 | Measurement method of dimple depth (Nikolova et al., 2017) | 37 |
| 2.18 | Experiment design of (a) two factors; (b) three factors and (c) 3 factor Box–Behnken design (Bezerra et al., 2008) | 40 |
| 2.19 | A three-dimensional response surface showing the expected yield (η) as a function of temperature ($x_1$) and pressure ($x_2$) | 42 |
| 3.1 | The research flow chart | 49 |
| 3.2 | Structure of laminated 4 layers FPC | 51 |
| 3.3 | FPC in row shape | 52 |
| 3.4 | FPC in panel shape | 53 |
| 3.5 | The layout of drilled via on the FPC | 54 |
| 3.6 | Layout of copper via filling | 59 |
| 3.7 | Dummy panel and FPC board arrangement | 61 |
| 3.8 | The arrangement of anode, cathode and sparger nozzle in the filling tank (Production Plant, MFS Technology (M) Sdn. Bhd.) | 62 |


UNIVERSITI TEKNIKAL MALAYSIA MELAKA

| | | |
|---|---|---|
| 3.9 | Rectifier of the machine (Production Plant, MFS Technology (M) Sdn. Bhd.) | 63 |
| 3.10 | Fluid flow meter of the machine (Production Plant, MFS Technology (M) Sdn. Bhd.) | 63 |
| 3.11 | Leica S6E stereo optical microscope (IPQC Office, MFS Technology (M) Sdn. Bhd.) | 65 |
| 3.12 | Plato E-FR-M1 grinder and polisher machine (IPQC Office, MFS Technology (M) Sdn. Bhd.) | 65 |
| 3.13 | Keyence VK-X200 series high power laser microscope (IPQC Office, MFS Technology (M) Sdn. Bhd.) | 66 |
| 3.14 | Illustration of different via properties | 67 |
| 4.1 | Copper filled via under different $I_d$, Q and $t_f$ | 71 |
| 4.2 | The main effect plot for surface thickness | 76 |
| 4.3 | The response surface plot of surface thickness between current density and fluid flow rate | 76 |
| 4.4 | The response surface plot of surface thickness between filling time and current density | 77 |
| 4.5 | The response surface plot of surface thickness between filling time and fluid flow rate | 77 |
| 4.6 | Normal probability plot for surface thickness | 79 |
| 4.7 | The main effect plot for dimple depth | 84 |
| 4.8 | The response surface plot of dimple depth between fluid flow rate and current density | 85 |
| 4.9 | The response surface plot of dimple depth between fluid flow rate and filling time | 85 |
| 4.10 | The response surface plot of dimple depth between current density and filling time | 86 |
| 4.11 | Normal probability plot for dimple depth | 87 |
| 4.12 | the main effect plot for via filling ratio | 91 |
| 4.13 | The response surface plot of via filling ratio between current density and fluid flow rate | 92 |
| 4.14 | The response surface plot of via filling ratio between current density and filling time | 92 |
| 4.15 | The response surface plot of via filling ratio between filling and fluid flow rate | 93 |
| 4.16 | Normal probability plot for via filling ratio | 94 |
| 4.17 | Fluid flow of electrolyte | 97 |
| 4.18 | Via filling mechanism | 99 |


UNIVERSITI TEKNIKAL MALAYSIA MELAKA

## LIST OF APPENDICES


| APPENDIX | TITLE | PAGE |
| --- | --- | --- |
| A | Gantt chart of master program by research | 121 |

# LIST OF ABBREVIATIONS

| | | |
|---|---|---|
| Adj MS | - | Adjusted mean square |
| Adj SS | - | Adjusted sum of square |
| ANOVA | - | Analysis of variance |
| BBD RSM | - | Box-Behnken design response surface methodology |
| BMV | - | Blind Micro Via |
| CCD RSM | - | Central composite design response surface methodology |
| CNC | - | Computer Numerical Control |
| DF | - | Degree of freedom |
| DoE | - | Design of Experiment |
| FKP | - | Fakulti Kejuruteraan Pembuatan |
| FPC | - | Flexible Printed Circuit |
| HCl | - | Hydrochloric Acid |
| HDI | - | High-density interconnection |
| IC | - | Integrated Circuit |
| JAMT | - | Journal of Advanced Manufacturing Technology |
| PCB | - | Printed Circuit Board |
| PEG | - | Polyethylene glycol |
| RSM | - | Respond Surface Methodology |
| S | - | Standard deviation |
| SEM | - | Scanning electron microscopy |
| SMT | - | Surface mount technology |
| SPS | - | Sulfopropyl sulfonate |
| TSV | - | Through Silicon Via |
| UTeM | - | Universiti Teknikal Malaysia Melaka |
| VMS | - | Virgin make-up solution |

UNIVERSITI TEKNIKAL MALAYSIA MELAKA

## LIST OF SYMBOLS

| | | |
|---|---|---|
| μ | - | Micro |
| $Cl^-$ | - | Chlorine ion |
| $Cu^{2+}$ | - | Copper ion |
| $I_d$ | - | Current density |
| Q | - | Fluid flow rate |
| $t_f$ | - | Filling time |

# LIST OF PUBLICATIONS

Journal

Wong, K.Y., Liew, P.J., Lau, K.T., and Wang, J., 2020. Optimization of copper via filling process for flexible printed circuit using response surface methodology. *Journal of Advanced Manufacturing Technology (JAMT)*, 14 (2), pp. 1–13.

Conference Proceedings

Wong, K.Y., Liew, P.J., and Lau, K.T., 2019. Copper Filling Of Printed Circuit Board (PCB) Industry: A Review. *International Symposium on Research in Innovation and Sustainability 2019 (ISoRIS '19)*. Penang, Malaysia, 28 - 29 August 2019.

UNIVERSITI TEKNIKAL MALAYSIA MELAKA

# CHAPTER 1

# INTRODUCTION

This chapter provides the background of this study, which focuses on optimisation of copper via filling characteristics on flexible printed circuit. The research background, problem statement, objectives, scope and outline are also presented in this chapter.

## 1.1 Research background

Flexible printed circuit (FPC) or printed circuit board (PCB) is commonly used in many fields such as aviation, automotive, medical equipment, electrical appliances and mobile electronic device (Zheng et al., 2012). Simultaneously, FPC also acts as a media for the final interconnections among all the completed chips and serves as the communication link between the component and the microelectronic circuitry within each packaged integrated circuit (IC). Moreover, FPC is also used to connect circuit components such as resistor and capacitor. In order to ensure all the components are well connected, those components are usually mounted on FPC by soldering or using surface mount technology (SMT) method (Kalpakjian and Schmid, 2014).

The advancement of FPC is attributed to Paul Eisler, which is commonly known as the father of PCB. In 1941, he made a great innovation of PCB by transferring the PCB production from laboratory scale to full-scale production (Petherbridge et al., 2005). However, the origin of FPC needs to be traced back to 20 years before Paul Eisler's contribution. In 1925, Ducas (1925) found an alternative way to manufacture electrical conductors without using the winding of individual strands of wire. This is the first concept formed at the early stage of FPC. Few years later, Parolini (1927) developed a new layout of

FPC, creating a printed circuit by using U-shaped pieces of metal acted as bridges at the intersections of tracks. In 1967, Shortes (1967) invented a new method to connect the conductive layer through a hole. To connect between different layers of copper, a hole was drilled on the PCB where a layer of copper was deposited into it. This invention provides the current connection between layers where the drilled hole acts as a pathway for the current to pass through. Therefore, the drilled hole is also widely known as 'via' referring to road or pathway in the Latin word (Lexico, 2020).

All of these inventions have greatly increased the capability of circuit board and led to the creation of the first modern PCB prototype. This innovation eventually influence the future development of the modern FPC (Petherbridge et al., 2005).

At present, FPCs are usually made in multilayers, with an electrical conductive material layer acting as a conductor and a few layers of insulator materials in between acting as dielectric (Yılmaz, 2008). These insulators are usually made by glass fibre reinforced polymer, epoxy, polyimide and carbon fibre reinforced polymer (Brindley, 1990). To connect between different layers of copper, manufacturers usually drill a hole on FPC and deposit copper onto it so the current could connect between layers. Meanwhile, in order to ensure the best conductivity and low production cost of FPC, copper is used for the electrical conductive layer (Ghosh, 2019) for it is a common material and deemed appropriate for electrical conduction properties (Pan et al., 2017).

Besides, in order to deposit a layer of copper onto the hole wall, the via of FPC will go through a plating process. Hence, a thin layer of copper will be plated onto the hole wall. This is one of a very crucial process in that to deposit certain materials on a subtract (Shacham-Diamand et al., 2015). Plating process is mainly occurred in molecular level where the plating will be able to reach within the narrowest place which is deemed useful in manufacturing miniaturised products, especially in the FPC industry (Yan et al., 2013).

UNIVERSITI TEKNIKAL MALAYSIA MELAKA

However, because of the plated copper layer is very thin, there is a high tendency for the copper layer to crack or deform when stress or bend is applied on the FPC. This will severely influence the performance of FPC such as causing a loss of signal on the data transfer and drop of voltage through the circuit. This problem could even reduce the lifespan of FPC. Therefore, to avoid the problem caused by plating, copper filling has been applied to the industry in order to resolve the quality issue of the FPC (Dow et al., 2008a; Millennium Circuits Limited, 2018).

Copper filling is a method for 3D-stacked packaging technology which has been widely investigated. It is also a technique to deposit copper in a bottom-up or superfilling mode to ensure a voidless fill in a via. Besides, copper via filling provides lot of advantages such as preventing circuits shortage and electromigration and reducing current leakage (Alling et al., 2002). Thus far, this method is still the most promising 3D packaging technology because it is able to enhance the performance of FPC with its small form factor, light weight, higher current density supported, low power consumption, and good electrical performance by interconnecting chips with the shortest vertical path (Wang et al., 2017d; Xiao et al., 2017a).

UNIVERSITI TEKNIKAL MALAYSIA MELAKA

## 1.2 Problem statement

The last two decades have seen a growing trend towards product miniaturisation in electronics industry (Nikolova et al., 2017). With the invention of through hole interconnections and surface-mount technology (SMT) since 1980s, the pace of product miniaturise has been accelerated faster than ever. Along with the prediction of Moore's Law, the market also expects the newly released devices will double their performance every 2 years (Kenny et al., 2012; Encyclopaedia Britannica, 2018).

However, with the limitation of 2D packaging technology, the dimension of miniaturisation and the performance enhancement of the component have reached to a bottleneck (Wang et al., 2017a; Sung et al., 2019). This phenomenon has forced FPC manufacturers to convert their manufacturing methods from 2D into 3D packaging (Zhang and Lu, 2017). As time passes, the production methods used for FPC are no longer the same as 50 years ago (Lau, 2014).

In addition, due to the rising pressure from the consumer market, manufacturers have to create devices in smaller sizes with greater performance (Li et al., 2018). As the device downsizing becomes an unavoidable trend, to some extent, the precise placement of individual dopant atoms will affect the output characteristics of a device. Eventually, the shrinking of device could potentially lead to higher failure rates and lower production yields. In this situation, the FPC fabrication process must be optimised in order to smaller the manufacturing tolerance to encounter the high failure rate (Walker et al., 2010).

During the electroplated copper via filling process, the parameters used must be in an optimum stage in order to prevent the filled via from overplating or underplating (Dow et al., 2008b; Schlesinger and Paunovic, 2010). Both situations will lead to the formation of seam, dimple and bumps on the micro via filling (Huebner et al., 2014). Due to the tight tolerance, the bumps may cause difficulties for the FPC to stack on the overfilled micro via and eventually planarisation issue might arise (Dow et al., 2008b). The seam and dimple may result in the formation of voids between the FPC which may deteriorate the FPC quality in terms of lifespan, performance and reliability (Joshi et al., 2019). Therefore, the optimum process variables of copper via filling must be studied in order to avoid the occurrence risk.

In this study, the effect of the copper via filling parameters (current density, fluid flow rate and filling time) on the filling characteristic of copper filled micro via (surface thickness, dimple depth and via filling ratio) were investigated. The optimisation of the

UNIVERSITI TEKNIKAL MALAYSIA MELAKA

process parameters and a basic fundamental of the mechanism of the copper via filling process were provided at the end of this study.

## 1.3 Research objectives

This study embarked on the following objectives:

i) To investigate the effect of copper via filling parameters (current density, fluid flow rate and filling time) on the filling characteristic of copper filled micro via (surface thickness, dimple depth and via filling ratio).

ii) To optimise and validate the copper via filling parameters in terms of surface thickness, dimple depth and via filling ratio by using Response Surface Methodology (RSM).

iii) To establish the process schematic diagram based on experimental results to reflect the mechanism of copper via filling process.

UTeM
اونيۏرسيتي تيكنيكل مليسيا ملاك
UNIVERSITI TEKNIKAL MALAYSIA MELAKA

## 1.4 Scope

The aim of this study was to focus on the investigation and optimisation of copper via filling parameters (current density, fluid flow rate and filling time) on the filling characteristic of copper filled micro via (surface thickness, dimple depth and via filling ratio). The data were analysed by response surface methodology (RSM) technique using Minitab statistical software. This study was also to determine the effect of the mechanism of the process variables on the copper via filling performance.

## 1.5 Research significance

As the miniaturisation trend is increasing, the FPC build quality had pushed to highest ever in human history. The need to produce a defectless FPC is demanded by the FPC industry. The key is by using the optimum parameters, then, a good quality or defectless FPC during the production could be obtained. This study, then, is to produce a guideline to either industry or future researchers to provide the basic knowledge regarding the mechanism of the FPC via filling process.

## 1.6 Research outline

The study consists of five chapters. The first chapter is introduction, which includes the research background, problem statement, objective, scope, and outline. Chapter 2 reviews the literature pertaining to the subject under study in related journal articles, thesis and textbook. Chapter 3 presents the methodology, detailing the experiments that are carried out, setup and way to analyse data. Then, the results of the experiments are analysed and discussed in Chapter 4. Eventually, Chapter 5 concludes the thesis and recommendation is made according to the results.

UNIVERSITI TEKNIKAL MALAYSIA MELAKA