A 0.6V IMPROVED PSRR BANDGAP REFERENCE FOR POWER MANAGEMENT SYSTEM IN RF ENERGY HARVESTING APPLICATIONS

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UNIVERSITI TEKNIKAL MALAYSIA MELAKA

MASTER OF SCIENCE IN ELECTRONIC ENGINEERING

2021

Faculty of Electronics and Computer Engineering

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MOHD KHAIRI BIN ZULKALNAIN

A thesis submitted
in fulfillment of the requirements for the degree of
Master of Science in Electronic Engineering

UNIVERSITI TEKNIKAL MALAYSIA MELAKA

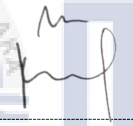
Faculty of Electronics and Computer Engineering

UNIVERSITI TEKNIKAL MALAYSIA MELAKA

2021

DECLARATION

I declare that this thesis entitled “A 0.6V Improved PSRR Bandgap Reference For Power Management System In RF Energy Harvesting Applications” is the result of my own research except as cited in the references. The thesis has not been accepted for any degree and is not concurrently submitted in candidature of any other degree.

Signature : 

Name : Mohd Khairi bin Zulkalnain

Date : 20th October 2021

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APPROVAL

I hereby declare that I have read this thesis and in my opinion, this thesis is sufficient in terms of scope and quality for the award of Master of Science in Electronic Engineering.

Signature :

Supervisor Name : Associate Professor Dr. Wong Yan Chiew

Date : 20th October 2021

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DEDICATION

This thesis is dedicated to my parents.

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ABSTRACT

The scaling of technology to lower process nodes is a major convenience as it allows for power saving by allowing the circuit to operate at a lower voltage. As per the prediction by International Technology Roadmap for Semiconductors (ITRS), the supply voltage will reduce down to 0.4V by 2024. Although the reduction of supply voltage is favourable in terms of power-saving, especially in powering Internet of Things (IoT) devices, the penalty incurred by this is the degradation of power supply rejection ratio (PSRR) due to reduced output impedance of bandgap reference circuits at lower voltage supply. The proposed work aims to mitigate this problem by employing metal oxide semiconductors (MOS) based proportional to absolute temperature (PTAT) and complementary to absolute temperature (CTAT) generator and regulated cascode techniques to improve the PSRR even at lower voltage supply, eliminating the need for voltage doubler circuits which injects noise in the substrate and degrades circuit performance. This improved PSRR bandgap reference circuit will then be used to power-up circuits that require high PSRR and clean power supply to ensure optimal functionality of IoT circuits, particularly sensitive circuits that degrade in functionality when subjected to noise travelling through power supply such as low power sensors and voltage controlled oscillators (VCOs) in frequency synthesizers. The objectives of this work are to investigate the characteristics and performances of the power management unit for radio frequency energy harvesting (RFEH) applications, design and develop bandgap reference with improved PSRR at low voltage supply, design and develop a low dropout (LDO) regulator to provide a constant voltage reference in RFEH system and validate and analyze the performance of the proposed circuit. This work managed to achieve a reference voltage of 0.405V over a wide temperature of -40 to 125°C, a PSRR of -41dB, line and load regulation of 1.188mV/V and 2.506mV/mA respectively and load current range from 0 to 800µA. The current consumption of the bandgap is 20.33µA and the whole power management unit (PMU) is 37µA and the temperature coefficient (TC) is 64.41ppm/°C. The bandgap area is 0.0627mm^2 while the whole PMU is 0.142mm^2. Overall, the design passes all the post layout validations such as design rule check (DRC) and layout vs schematic (LVS) and functions as expected. The post-layout simulations were analyzed and the results closely agree with the pre-layout simulations. On top of that, this work demonstrates the robustness of the bandgap reference circuit when integrated at the top level with the LDO, start-up and biasing circuits as it is able to operate, with 50% improvement in PSRR over conventional design at a supply voltage of 0.6V, making it suitable to power up sensitive IoT circuits.

PENAMBAHBAIKAN 0.6V RUJUKAN SELA JALUR PSRR UNTUK SISTEM PENGURUSAN KUASA DALAM APLIKASI PENUAIAN TENAGA RF

ABSTRAK

Penskalaan teknologi ke nod proses yang lebih rendah adalah satu kelebihan kerana memungkinkan penjimatan kuasa dengan membenarkan litar beroperasi pada voltan yang lebih rendah. Seperti yang dijangkakan oleh halatuju teknologi separuh pengalir antarabangsa (ITRS), voltan bekalan akan berkurang sehingga 0.4V menjelang 2024. Walaupun pengurangan voltan bekalan adalah bagus dari segi penjimatan kuasa, terutama dalam menghidupkan peranti internet benda (IoT), penalti yang ditanggung adalah penurunan nisbah penolakan bekalan kuasa (PSRR) disebabkan oleh pengurangan rintangan litar rujukan sela jalur pada bekalan voltan yang lebih rendah. Teknik yang dicadangkan bertujuan untuk mengurangkan masalah ini dengan menggunakan penjana suhu kadaran mutlak (PTAT) dan suhu pelengkap mutlak (CTAT) berdasarkan separuh pengalir oksida logam (MOS) dan teknik kaskod terkawal untuk meningkatkan PSRR walaupun pada bekalan voltan yang lebih rendah sekaligus menghilangkan keperluan untuk litar pengganda voltan yang menyuntik hingar ke dalam substrat dan menurunkan prestasi litar. Litar rujukan sela jalur PSRR yang diperbaiki ini kemudiannya akan digunakan untuk menghidupkan litar yang memerlukan PSRR tinggi dan bekalan kuasa bersih untuk memastikan fungsi optimum litar IoT, terutamanya litar sensitif yang merosot kefungsian apabila disuntik hingar dari bekalan kuasa seperti litar penderia berkuasa rendah dan litar pengayun dikawal voltan (VCO) dalam pensintesis frekuensi. Objektif kajian ini adalah untuk menyiasat ciri-ciri dan prestasi unit pengurusan kuasa untuk aplikasi penuai tenaga frekuensi radio (RFEH), mereka bentuk dan mengembangkan litar rujukan sela jalur dengan peningkatan PSRR pada bekalan voltan rendah, mereka bentuk dan mengembangkan litar ciciran rendah (LDO) untuk memberikan rujukan voltan pemalar dalam sistem penuaian tenaga frekuensi radio (RF) dan mengesahkan dan menganalisis prestasi litar yang dicadangkan. Kajian ini berjaya mencapai voltan rujukan 0.405V pada julat suhu -40 hingga 125°C, PSRR -41dB, peraturan garis dan beban 1.188mV/V dan 2.506mV/mA dan bebanan arus antara 0 hingga 800µA. Litar rujukan sela jalur ini menggunakan arus sebanyak 20.33µA manakala keseluruhan unit pengurusan kuasa (PMU) menggunakan arus sebanyak 37µA. Jumlah pekali suhu (TC) pula adalah 64.41ppm/°C. Kawasan bentangan litar sel jalur adalah 0.0627mm^2 sementara keseluruhan PMU adalah 0.142mm^2. Secara keseluruhan, reka bentuk litar sela jalur ini melepasi semua pengesahan pasca-bentangan seperti semakan aturan rekabentuk (DRC) dan semakan antara bentangan dan skematik (LVS) dan berfungsi seperti yang dijangkakan. Simulasi pasca-bentangan dianalisis dan hasilnya bertepatan dengan simulasi pra-bentangan. Selain itu, kajian ini menunjukkan kesepaduan rangkaian litar rujukan sela jalur ketika digabungkan dengan LDO, litar pemula dan litar pincang kerana dapat beroperasi dengan peningkatan 50% PSRR berbanding reka bentuk konvensional pada bekalan voltan 0.6V, menjadikannya sesuai untuk menghidupkan litar IoT yang sensitif.

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TABLE OF CONTENTS

		PAGE
DECLARATION		
APPROVAL		
DEDICATION		
ABSTRACT		**i**
ABSTRAK		**ii**
ACKNOWLEDGEMENTS		**iii**
TABLE OF CONTENTS		**iv**
LIST OF TABLES		**vi**
LIST OF FIGURES		**vii**
LIST OF SYMBOLS AND ABBREVIATIONS		**xii**
LIST OF PUBLICATIONS		**xiii**
CHAPTER		
1.	**INTRODUCTION**	**1**
1.1	Background	1
1.2	Power Supply Rejection Ratio (PSRR)	3
1.3	Problem statement	4
1.4	Research objective	5
1.5	Scope of research	6
1.6	Contribution of research	6
1.7	Thesis outline	7
2.	**LITERATURE REVIEW**	**9**
2.1	Introduction	9
2.2	Conventional bandgap reference operation	9
2.3	Bandgap reference topologies	13
2.3.1	PSRR enhancement techniques	13
2.3.1.1	Voltage subtraction technique	13
2.3.1.2	Pre-regulation technique	13
2.3.1.3	Filtering technique	16
2.3.1.4	Cascode technique	16
2.3.1.5	Regulated cascode technique	17
2.3.2	Low voltage supply techniques	19
2.3.2.1	MOS based PTAT and CTAT generators	19
2.3.2.2	Switched capacitor circuits	23
2.4	Low dropout regulator topologies	28
2.5	Research gap	34
2.6	Summary	35
3.	**METHODOLOGY**	**36**
3.1	Introduction	36
3.2	Research design specifications	36
3.3	Project flowchart	37
3.4	Transistor sizing	40
3.5	Proposed bandgap reference operation and design	41
3.6	Low dropout regulator operation and design procedure	49

UNIVERSITI TEKNIKAL MALAYSIA MELAKA

3.7 LDO and top level integration of PMU 53
3.7.1 Top level current mirror for biasing 53
3.7.2 Start-up circuit 55
3.7.3 Top level circuit and layout integration 57
3.8 Layout design techniques 58
3.8.1 Matching 58
3.8.2 Electromigration 58
3.8.3 Floorplanning and routing 59
3.9 Experimental setup 59
3.9.1 Bandgap reference testbench setup 59
3.9.2 Top level bandgap reference and LDO integration testbench 60
3.10 Summary 61

4. RESULT AND DISCUSSION 62
4.1 Introduction 62
4.2 Bandgap reference circuit results 62
4.2.1 Voltage reference 62
4.2.2 PSRR 62
4.2.3 Line regulation 64
4.2.4 Stability 65
4.2.5 LVS and DRC 69
4.2.6 Monte carlo 71
4.3 Top level integration results 72
4.4 Table of comparison 74
4.5 Layout design 81
4.6 Summary 83

5. CONCLUSION AND RECOMMENDATIONS 84
5.1 Conclusion 84
5.2 Future work and recommendations 86

REFERENCES 87

UNIVERSITI TEKNIKAL MALAYSIA MELAKA

LIST OF TABLES

TABLE	TITLE	PAGE
2.1	Comparison of previous work on bandgap reference	26
2.2	Comparison of previous work on bandgap reference (Continued)	27
2.3	Comparison of previous work on LDO	33
3.1	Design specification for the proposed bandgap reference circuit	37
3.2	Design specification for the proposed LDO	37
3.3	Device dimensions for the proposed bandgap reference circuit	44
3.4	Device dimensions for P-Input op amp	49
3.5	Device dimensions for N–input op amp	49
3.6	Device dimensions of LDO	52
3.7	Device dimensions of current mirror circuit	55
3.8	Device dimensions for startup-circuit	57
4.1	Summary of gain and phase margin of all loops	69
4.2	The comparison of the proposed bandgap reference with existing architectures in literature	79
4.3	The comparison of the PMU with existing architectures in literature	80

UNIVERSITI TEKNIKAL MALAYSIA MELAKA

LIST OF FIGURES

FIGURE	TITLE	PAGE
1.1	Typical power management unit (PMU) for RFEH systems	1
1.2	Switching current of digital blocks causing a voltage drop across the inductor and manifest itself in the form of noise	3
2.1	The basic operation of bandgap reference circuit where the CTAT and PTAT are summed up to obtain a stable voltage over temperature. (Allen & Holberg, 2016)	10
2.2	Conventional bandgap circuit by Neuteboom (1997)	11
2.3	Conventional sub 1-V bandgap reference for low power operation by Banba et al. (1999)	12
2.4	Voltage subtraction technique where the power-supply is coupled to the feedback by means of a common source circuit. (Abbasi et al., 2015)	14
2.5	Pre-regulation by means of an LDO which regulates the power supply going into the bandgap reference circuit. (Lee & Chang, 2018)	15
2.6	Pre-regulation by means of isolation of the power supply from the bandgap reference circuit by the current mirror transistors. (Abbasizideh et al., 2016)	15
2.7	The filtering technique in which transistors configured as MOSCAPs and resistors are used to design LPF circuit and filter high frequency variation (Alhassan et al., 2016)	16
2.8	The stacking of transistors or better known as the cascode technique	17

	increases the output impedance and therefore PSRR (Soell et al., 2015)	
2.9	Improved PSRR sub 1-V bandgap reference using regulated cascode to increase output impedance and mitigate channel length modulation. (Kamel et al., 2016)	18
2.10	A MOS based PTAT and CTAT generator bandgap reference circuit for low voltage operation. (Li et al., 2011)	19
2.11	A modification of the work by Banba et al. (1999) bandgap reference by replacing the BJT to MOS based CTAT and PTAT generator. (Yang et al., 2011)	21
2.12	A resistorless and fully MOS bandgap reference for saving area and low voltage supply operation. (Wang et al., 2015)	22
2.13	A bandgap reference utilizing oscillator, charge pump, switch capacitor and a bandgap core. (Mu et al., 2016)	24
2.14	A switch capacitor network based bandgap reference to generate the delta VBE PTAT across a capacitor. (Shristasva et al., 2015)	24
2.15	A bandgap design using charge pump, switched capacitor network as the bandgap core, sample and hold and a clock control block. (Luo et al., 2018)	25
2.16	An LDO architecture with common gate and filter structure for PSRR improvement. (Abbasizedh et al., 2016)	28
2.17	An LDO with class AB OTA and using a PMOS pass transistor in cascode with an NMOS. (Khan et al., 2018)	29
2.18	LDO with improved stability and load transient by using an op-amp in unity gain feedback. (Liu et al., 2019)	30
2.19	An NMOS pass transistor based LDO with charge pump and digital to	31

	analog signal generator. (Tang et al., 2018)	
3.1	Flowchart of the design process of the PMU system	39
3.2	Diode connected NMOS and PMOS to extract small signal DC parameters for a given fixed current	40
3.3	Proposed bandgap reference schematic utilizing regulated cascode and MOS based PTAT and CTAT generator techniques	42
3.4	N-input 2 stage op amp for loop2 of the proposed bandgap reference and LDO	46
3.5	P-input 2 stage op amp for loop 1 of proposed bandgap reference	46
3.6	The conventional LDO architecture used for the proposed PMU system	51
3.7	Basic current mirror operation where current flowing through MN1 and MN2 are equal provided that both transistors have same size and gate voltage	53
3.8	Biasing circuit consisting of current mirrors	54
3.9	Start-up circuit for the bandgap to achieve optimal DC operating point	57
3.10	Top level integration of the PMU system	58
3.11	The bandgap reference testbench with ideal current source and start-up circuit	60
3.12	The setup for the top level PMU system driving a capacitive and current load	61
4.1	Bandgap reference for pre-layout (red) and post-layout (blue) simulation	63
4.2	PSRR of proposed bandgap reference (green) and conventional bandgap reference (pink)	63
4.3	PSRR of proposed bandgap pre-layout (red) and	64

UNIVERSITI TEKNIKAL MALAYSIA MELAKA

	post-layout (blue)	
4.4	Voltage supply is swept from 0 to 1.2V	65
4.5	Line regulation simulation of the bandgap reference at 0.5V, 0.6V and 1.2V	65
4.6	Gain and phase margin of pre-layout for loop 1 in the proposed bandgap reference	66
4.7	Gain and phase margin of post-layout for loop 1 in the proposed bandgap reference	67
4.8	Gain and phase margin of pre-layout for loop 2 in the proposed bandgap reference	67
4.9	Gain and phase margin of post-layout for loop 2 in the proposed bandgap reference	68
4.10	Gain and phase margin of pre-layout for LDO	68
4.11	Gain and phase margin of post-layout for LDO	69
4.12	DRC simulation results showing 0 errors	70
4.13	LVS simulation showing that layout and schematic are identical	70
4.14	Monte Carlo histogram of the reference voltage	71
4.15	Monte Carlo simulation summary	72
4.16	Pre-layout load transient simulation for the whole PMU system	73
4.17	Post-layout load transient simulation for the whole PMU system	73
4.18	The regulated voltage of the LDO output across varying load current	74
4.19	The proposed bandgap reference circuit	81
4.20	The proposed bandgap reference circuit layout design	82
4.21	Floorplan integration of the PMU system comprising of the biasing, startup, bandgap reference and LDO circuits	82

UNIVERSITI TEKNIKAL MALAYSIA MELAKA

4.22 Layout integration of the PMU system comprising of the biasing, startup, bandgap reference and LDO circuits 83

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LIST OF SYMBOLS AND ABBREVIATIONS

AC	-	Alternating Current
ADC	-	Analog to Digital Converter
BJT	-	Bipolar Junction Transistor
CMOS	-	Complementary Metal Oxide Semiconductor
CTAT	-	Complementary to Absolute Temperature
DC	-	Direct Current
DRC	-	Design Rule Check
ECG	-	Electrocardiograms
EDA	-	Electronic Design Automation
EEG	-	Electroencephalograms
EMG	-	Electromyography
IoT	-	Internet of Things
ITRS	-	International Technology Roadmap of Semiconductors
LDO	-	Low Dropout Regulator
LNA	-	Low Noise Amplifier
LVS	-	Layout Vs Schematic
MC	-	Monte Carlo
MOS	-	Metal Oxide Semiconductor
OTA	-	Operational Transconductance Amplifier
PCE	-	Power Conversion Efficiency
PDK	-	Process Design Kit
PEX	-	Parasitic Extraction
PMU	-	Power Management Unit
PLL	-	Phase Locked Loop
PSRR	-	Power Supply Rejection Ratio
PTAT	-	Proportional to Absolute Temperature
PVT	-	Process Voltage Temperature

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RF	-	Radio Frequency
RFEH	-	Radio Frequency Energy Harvesting
SMPS	-	Switching Mode Power Supply
SoC	-	System On Chip
SRAM	-	Static Random Access Memory
TC	-	Temperaturce Coefficient
VCO	-	Voltage Controlled Oscillator
Vref	-	Reference Voltage
Vth	-	Threshold Voltage

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LIST OF PUBLICATIONS

The research papers produced and published during the course of this research are as follows:

1) Zulkalnain, M., Kamsani, N., Mohd Sidek, R., Rokhani, F., Hashim, S. and Hamidon, M., 2019. -81dB PSRR regulated cascode fully MOS bandgap reference for power management in RF energy harvesting systems. *Indonesian Journal of Electrical Engineering and Computer Science*, 14(2), p.706.

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CHAPTER 1

INTRODUCTION

1.1 Background

Radio frequency energy harvesting (RFEH) is a promising way to scavenge energy from the environment to power up Internet of Things (IoT) sensors and low-power applications. The scaling down of technology nodes also contribute to more low-power devices, making RFEH even more desirable. This is because RFEH offers interesting attributes such as reduced cost and lower periodic maintenance which is especially useful when involving IoT devices in harsh environments that complicate the maintenance process. Apart from that, the lifetime of the storage can be extended (Soyata et al., 2016).

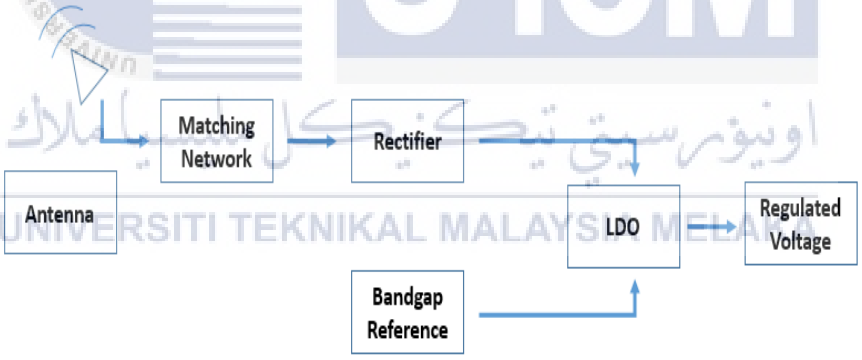

Figure 1.1: Typical power management unit (PMU) for RFEH systems

Circuitry reported in literature that can potentially benefit from RFEH include low power sensors which operate at sub-threshold or near threshold are the perfect candidate for RFEH systems. In order to power low power devices through RFEH, a power management system such as the one shown in Figure 1.1 can be employed.

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The power management system for RFEH contains blocks such as an antenna, a matching network, a rectifier, a bandgap reference and an low dropout (LDO) regulator. The power management system works such that RF signal is first collected through the antenna (Masius, Wong & Lau, 2018) and is fed into a matching network which functions to maximize power transfer and to provide passive amplification. The signal then passes through a rectifier which converts the radio frequency (RF) signal into direct current (DC) signal (Mohd Kamel & Wong, 2019). The DC signal is then fed into the LDO to be regulated. The bandgap serves as a reference voltage to the regulator that provides a stable voltage across variations in temperature.

There is a lot of work being done on RFEH targeting different blocks in the RFEH PMU system. For example, works by Mrnka et al. (2016) and Ramesh and Rajan (2014) focuses on optimizing the antenna performance to obtain a higher power conversion efficiency (PCE). Apart from that, works by Al-Lawati et al. (2012); Liu, Z et al. (2018) and Noghabaei et al. (2018) aim to improve the performance of the rectifier by employing different architectures. The overwhelming amount of research on RFEH has resulted in interesting circuit implementations at the top level. RFEH powered transceivers for sensor and IoT applications such as the designs by Masuch et al. (2012); Taghivand et al. (2015); Rajavi et al. (2016); Kim, Y. et al. (2015) and Gao et al. (2013).

A bandgap reference circuit targeted at improving PSRR on 130nm complementary metal oxide semiconductor (CMOS) technology targeting IoT RFEH devices that operate at sub-threshold and near-threshold region that exhibits improvement over the conventional design. The circuit will be designed at the schematic level and verified pre-silicon. A layout of the proposed circuit will then be designed and post-layout verification will be carried out as a proof of concept of the RFEH system.

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1.2 Power Supply Rejection Ratio (PSRR)

In order to understand the concept of a clean power supply, consider Figure 1.2, in which the power supply has been modeled by an inductor connected to the power supply due to the inductance of the wire bond to the input and output pins. As can be seen, since the analog and digital blocks share same power rails, both voltage supply and ground, the fast transient currents due to switching of digital currents will induce a voltage drop across the inductor, hence creating an unclean power supply or noise and causing problems to analog circuits such as headroom issues among other things. Coming back to the concept of PSRR, an analog circuit is characterized by its ability to reject this noise from the power rails, hence the name PSRR to ensure optimum performance of circuits of both domains.

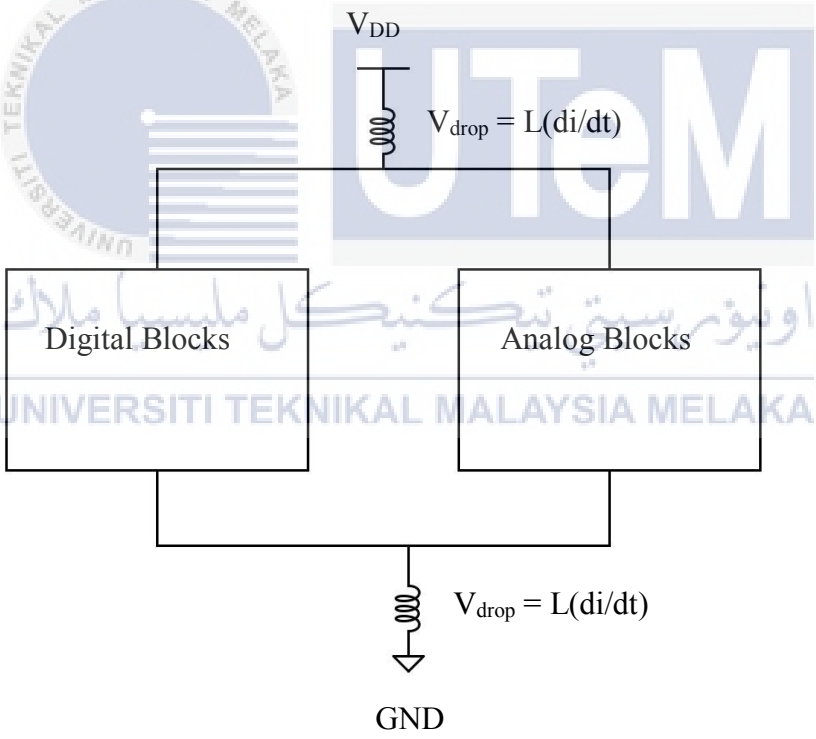

Figure 1.2: Switching current of digital blocks causing a voltage drop across the inductor and manifest itself in the form of noise

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1.3 Problem statement

In low power sensors, the accuracy of the functionality may be affected especially since the sensors are required to detect minute levels of changes in stimuli and are therefore very sensitive to noise. The same applies to the voltage controlled oscillator (VCO) where it is particularly sensitive to noise in the power supply. Digital switching injects noise to the substrate due to the charge and discharge of current from the power supply (Nagata et al., 2001). The effects of this is can be devastating, especially in the era where digital and analog circuits are integrated on the same die. From a digital perspective, an unstable power supply will cause of noise and gate delay in digital design and this conclusion is supported by Andrade et al. (2007) and Charbon et al. (1999).

In a mixed signal environment, power supply noise due to digital switching injected to voltage reference can cause non-linearity in blocks such as mixers and low noise amplifiers (LNAs) and bit errors in analog to digital converters (ADCs) (Ozbas et al., 2003). In a clock generation circuitry, any noise injected through the power supply will affect the control voltage of the VCO to operate optimally, resulting in jitter in the phase locked loop (PLL) affecting the reliability of clock generation (Magierowski et al., 2004). One way to mitigate this is to employ high PSRR in power management circuits such as bandgap reference (Chahardori, Atarodi and Sharifkhani, 2011). As such, this work focuses on the design of bandgap reference circuit in power management system with improved PSRR and discusses the block in detail.

In terms of applications, recently there has been an upsurge of circuitry operating at around 0.4V or near threshold voltage. Low power sensors in works by Ashouei et al. (2011) and Konijnenburg et al. (2013), low voltage supply ADCs and PLLs by Anvesha and Raychowdhury (2017); Hsieh et al. (2018); Lee, P. et al. (2016), Jo et al. (2018) and Moon et al. (2014), memory circuitry by Dubey et al. (2017), image sensor by Chiou et al.

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