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# High efficiency Doherty power amplifier based on asymmetrical matching network

**Mussa Mabrok[1], Zahriladha Zakaria[2], Tole Sutikno[3]**
[1,2]Center for Telecommunication Research and Innovation (CeTRI), Faculty of Electronics and Computer Engineering, Universiti Teknikal Malaysia Melaka (UTeM), Melaka, Malaysia.
[3]Department of Electrical Engineering, Universitas Ahmad Dahlan, Indonesia

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**ABSTRACT**

Doherty power amplifier (DPA) with high efficiency at the output power back off is highly demanded for modern wireless communication systems to achieve high data rates and reduce the power consumption and operation costs. This paper presents a new design strategy for enhancing DPA's back-off efficiency. New design strategy called asymmetrical matching network is used to achieve asymmetric operation, which helps to compensate for the low power delivered by the peaking stage in the conventional DPA. The simulation results showed an enhancement in the back-off efficiency, where the proposed design is able to achieve 46-52 % drain efficiency at 8 dB output power back-off while maintains high efficiency of 73-80 % at saturation over the designed bandwidth of 3.4-3.6 GHz. The proposed design is suitable for high efficiency sub-6 GHz fifth-generation wireless applications.



***Corresponding Author:***

Zahriladha Zakaria
Center for Telecommunication Research and Innovation (CeTRI)
Faculty of Electronics and Computer Engineering
Universiti Teknikal Malaysia Melaka (UTeM)
Hang Tuah Jaya, 76100 Durian Tunggal, Melaka, Malaysia
Email: zahriladha@utem.edu.my

## 1. INTRODUCTION

The requirement for increasing the amount of transmitted data within a limited bandwidth using wireless communication systems is growing rapidly and is expected to continue, especially with the developments of the LTE-Advanced system, where the user is being attracted by the video streaming and multimedia data in addition to the internet of things (IoT) technology revolution [1]–[3]. Hence, the fifth-generation (5G) wireless communication will include several technologies that can help to achieve the promised goals of the 5G. Some of these are the use of massive multi-input multi-output (MIMO), carrier aggregation, beam forming and more complex modulation schemes which produce a high peak to average power ratio (PAPR). From the transmitter point of view, power amplifier (PA) is one of the most important subsystems for radio frequency (RF) and wireless transmitters. In addition, it is also a component which consumes a lot of the energy [2]. PA with high efficiency is always an important research topic; because a low efficiency PA consumes a lot of power, requiring a large heat sink and increasing system operation cost [3]. Modulated signals with high PAPR require PAs to be operated at back-off (BO) power levels from its saturation point (i.e. maximum output power) to avoid signal clipping and distortion. Conventional PAs such as class A, and class AB suffer from low efficiency at BO power regions as their efficiencies determine at the maximum output power. Therefore, to efficiently amplify the modulated signals with high PAPR, the

amplifier's efficiency should be enhanced in the BO region [4]-[6]. In this regard, several techniques have been proposed such as Doherty power amplifier (DPA), sequential power amplifier (SPA), outphasing, and recently load modulated balanced amplifier (LMBA) [7]-[10]. Among all of these techniques, DPA is considered as the most suitable technique for modern wireless communication signals with high PAPR. This is mainly due to its simple structure, ease of implementation, and high performance especially the efficiency at the BO [11]-[15]. However, conventional DPAs are limited to 6 dB BO level which are unable to satisfy the requirements of modern wireless communication systems such as the upcoming 5G. This is due to that the auxiliary (peaking) stage of DPA delivers low saturation output power than the main stage due to its biasing Class-C which leads to incomplete load modulation and as a results low BO efficiency. Although different approaches have been proposed in the literature [16]-[24] to solve this problem and enhance the efficiency at a largest possible BO level (above 6 dB). However, they are still limited. Among all these techniques, asymmetrical DPA is the most used technique. Unlike the previous asymmetrical DPAs, where the asymmetry was achieved based on asymmetrical biasing voltages as in [25] which requires an additional dc voltage source, asymmetrical devices as in [18], [19] which requires using high power transistor at peaking stage to compensate low power caused by its biasing class C, or asymmetrical power divider, which puts some limitations on the implementations when high power division ratio is required [20], [21]. In this work, unequal output power issue can be overcome by balancing the delivered output power from the sub-amplifiers through matching network design. In other words, the output matching network of the sub-amplifiers is designed carefully and optimized to achieve pre-determined output power.

## 2. RESEARCH METHOD

### 2.1. Basic DPA

The DPA was invented by W. H. Doherty in 1936. It consists of two amplifiers called main (carrier) and auxiliary (peaking) connected in parallel as shown in Figure 1. The two amplifiers are biased in class-AB and Class-C respectively. The impedance inverter at the output of the main amplifier is used to modulate the load of the main amplifier from 100 Ω at low power level to 50 Ω at high power level. To compensate for the phases difference introduced by the impedance inverter, a delay line is used at the input of auxiliary amplifier. Two lines called offset lines are used at the output of the two amplifiers for performance optimization [26]. Where, the one at the main amplifier is used to improve the efficiency at the BO region, while the other at the output of the auxiliary stage is used to reduce the power leakage from the main path during the peaking off-state [27]. Power divider is used at the input to distribute the power to the two amplifiers.

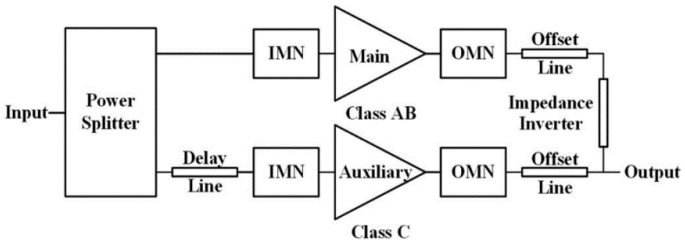



Figure 1. Block diagram of a standard DPA [16]

### 2.2. Design process

In this section, the design procedures are presented. The target frequency band for this design is 3.4-3.6 GHz which is one of the proposed sub-6GHz 5G frequency bands [22]. A 15 Watt GaN-HEMT transistor (CGH35015) produced by wolfspeed/Cree is selected to be used in this design due to its compatibility with design specifications. Table 1 shows the specifications of the proposed design.

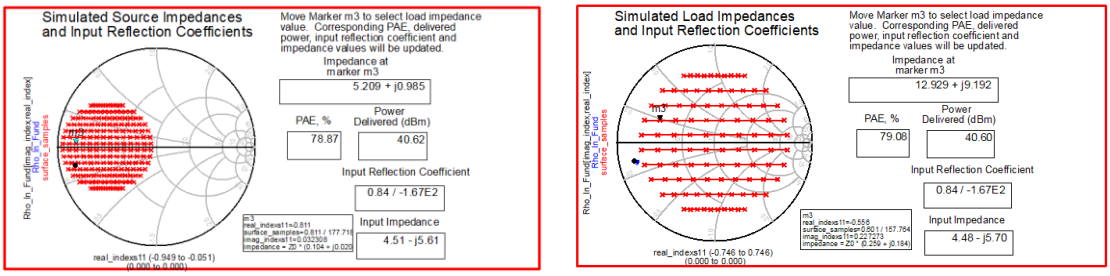
Table 1. Specifications of the proposed design

| Parameter | Value |
|---|---|
| Frequency | 3.4-3.6 GHz |
| Gain | ≥ 10 dB |
| Output power ($P_{out}$) | 42-43 dBm |
| Drain Efficiency (DE) | 40-50 % |
| BO | > 6 dB |

### 2.2.1. Carrier (main) DPA

Before designing input and output matching networks, optimum source and load impedances of the selected transistor should be obtained for the main DPA under class-AB biasing. This is can be done using HB 1Tone source pull and HB-1Tone load pull tools available in advanced design system (ADS). The selected load impedance under class-AB biasing (VDS = 28 V, VGS = -2.9 V) is 12.929 +j9.192 which is capable of delivering output power of 40.6 dBm and maximum drain efficiency of 79.08 % as shown in Figure 2 (a). The selected optimum source impedance from source pull simulation is 5.209+j0.985 as shown in Figure 2 (b). The selected source and load impedances can be used to design input and output matching networks. There are several matching network techniques such as lumped element matching, single stub matching, double stub matching, and quarter wave transformer matching and many more. In this design, quarter wave transformer technique is used. The reason for selecting this technique is its simple structure where it is build based on simple transmission line.

As the main DPA's offset line is used to enhance the efficiency at the BO as we mentioned earlier. So, selecting an appropriate length will result in high BO efficiency. Figure 3 shows simulated drain efficiency with different electrical lengths of main DPA offset line. Offset line of 114° is an appropriate electrical length (E) which can achieve high efficiency over the entire bandwidth of 3.4-3.6 GHz.




(a) (b)

Figure 2. (a) Simulated Source Impedance of carrier DPA and (b) Simulated load Impedance of carrier DPA

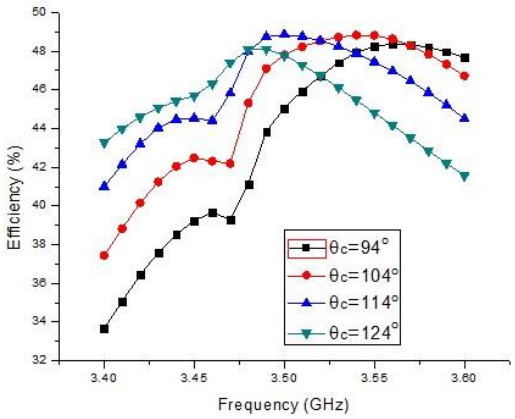



Figure 3. Simulated efficiency with different electrical lengths of main (carrier) Doherty PA offset line

### 2.2.2. Peaking (auxiliary) DPA

The selected load impedance of peaking DPA under Class-C biasing (VDS = 28 V, VGS = -5.5 V) is 7.161+j2.48 which is capable of delivering output power of 41.07 dBm and maximum drain efficiency of 63.66 % as shown in Figure 4. For the sake of simplicity, source impedance selected in main DPA design is used in peaking's input matching design. The peaking's offset line is used to present an open circuit at the DPA's combining point in order to prevent the power leakage from the main DPA to the peaking branch when it is tuned off (off-state). The peaking DPA off-state in this design is in the input power range from 0 to 21 dBm. Based on the analysis in Figure 5, an appropriate line length which reduces power leakage and produces high output power is 132°.

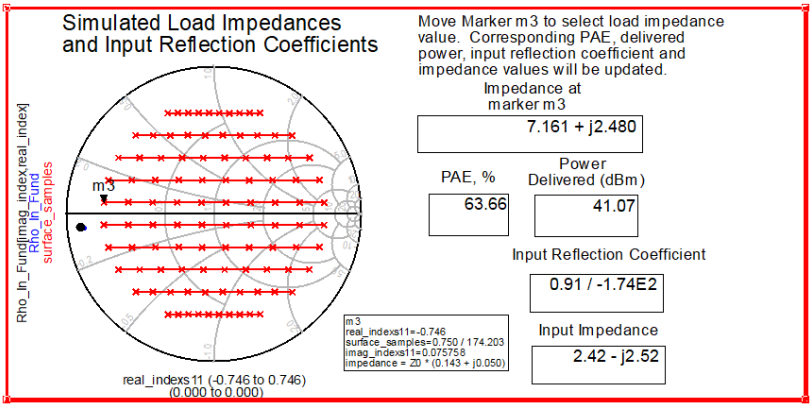



Figure 4. Simulated load Impedance of Peaking (auxiliary) DPA

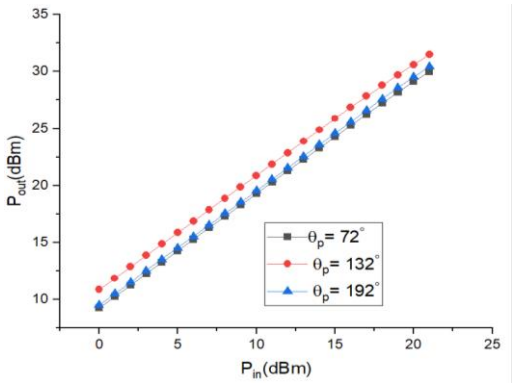



Figure 5. Simulated dpa's output power versus input power with different electrical lengths of peaking offset line

### 2.2.3. Power splitter

Conventional single-section Wilkinson power divider (WPD) is used at the input side of the DPA for power division purpose for the sub-amplifiers (main & auxiliary). The simulated return loss at the all three ports ($S_{11}$, $S_{22}$, and $S_{33}$) is lower than -20 dB over the designed frequency band 3.4-3.6 GHz as shown in Figure 6. The simulated isolation between output ports ($S_{23}$) is better than -20 dB over the whole frequency band as it can be seen from Figure 7 (a). The simulated values of insertion loss $S_{12}$ & $S_{13}$ are -3 dB for the entire frequency band as shown in Figure 7 (b).

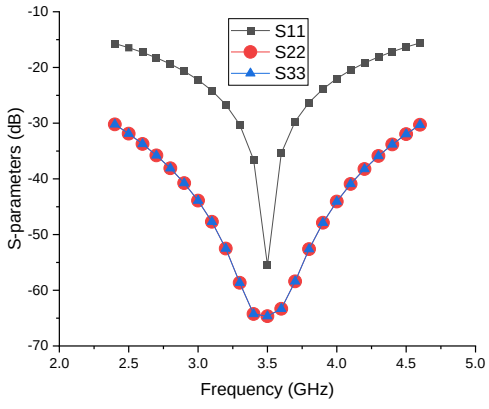



Figure 6. Simulated return loss at all three ports of microstrip single-section Wilkinson power divider

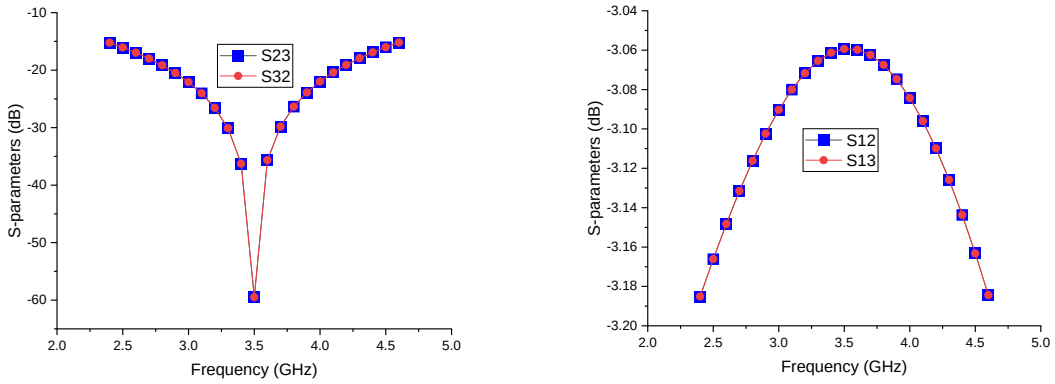



Figure 7 (a) Simulated isolation between output ports ($S_{23}$) of microstrip Wilkinson power divider and (b) Simulated insertion loss ($S_{12}$ & $S_{13}$) of microstrip Wilkinson power divider.

## 3. PERFORMANCE EVALUATION

Finally, the sub-amplifiers (main & auxiliary) designed in previous sub-sections are combined into one circuit to form the full Doherty design in order to evaluate its performance. Figure 8 shows schematic diagram of microstrip full DPA design. The designed circuit simulated using ADS based on duroid5880 substrate with thickness (h) of 0.79 mm and dielectric constant ($\varepsilon_r$) of 2.20. The simulated S-parameters results are shown in Figure 9. The small-signal gain ($s_{21}$) is higher than 10 dB across the target bandwidth 3.4-3.6 GHz. The input return loss ($s_{11}$) is better than -10 dB, while the output return loss ($S_{22}$) is better than -5 dB over the band.

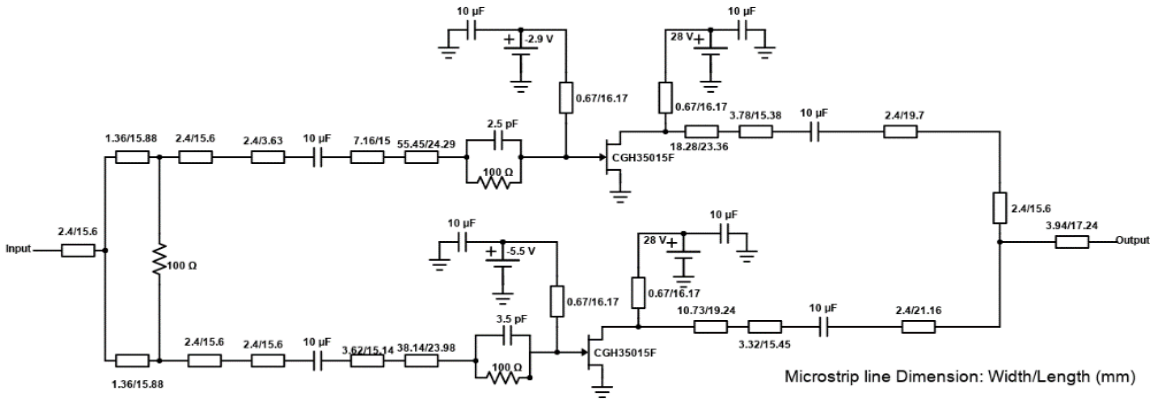



Figure 8. Schematic diagram of proposed DPA

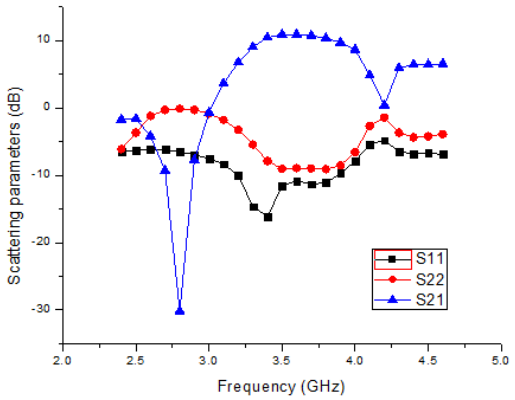



Figure 9. Simulated s-parameter of proposed DPA

The simulated maximum output power versus frequency is presented in Figure 10 (a). The proposed DPA achieves output power of higher than 42.8 ± 0.6 dBm over the entire bandwidth. The simulated drain efficiency versus frequency is shown in Figure 10 (b). At peak output power, the simulated drain efficiency is 73-80 %. Whereas, at 8-dB BO, the simulated drain efficiency is 46-52%.

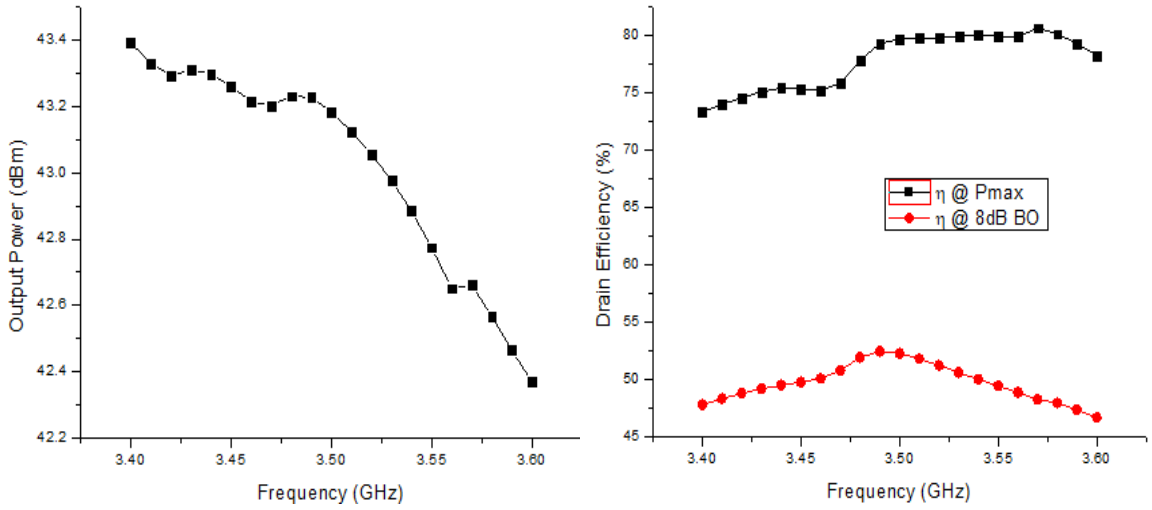



Figure 10. (a) Simulated maximum output power versus frequency and
(b) Simulated drain efficiency versus frequency at peak output power and at 8-dB back-off

Figure 11 shows the simulated drain efficiency of the conventional and proposed DPA at the centre frequency of 3.5 GHz. It can be observed that at 8 dB BO, about 8 % improvement in the efficiency can be achieved by the proposed design. Furthermore, both designs can achieve the same saturation powers (about 43 dBm).

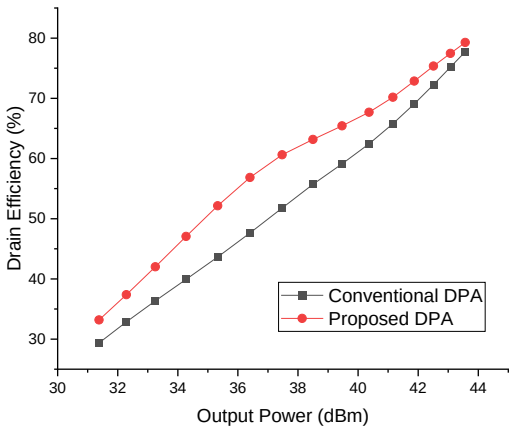



Figure 11. Simulated drain efficiency of conventional and proposed Doherty power amplifier as a function of output power at 3.5 GHz

Comparison between recently published DPAs and proposed DPA in this work is made as shown in Table 2. The proposed DPA has gain, and output power comparable to recent published DPAs. It can be seen that the proposed DPA has higher back-off efficiency with moderate bandwidth compared to other DPA designs.

Table 2. Performance comparison of the proposed DPA with recent published DPA designs

| Ref. | Frequency (GHz) | Tech. | Gain (dB) | BO (dB) | $P_{OUT, avg}$ (dBm) | Eff @ BO (%) |
|---|---|---|---|---|---|---|
| [5] 2013 | 3.4-3.5 | GaN-HEMT | 6.5-9.5 | 9 | 40.4 | 40 (DE) |
| [6] 2014 | 2.0 | GaN-HEMT | NA | 9 | 33.2 | 54 (DE) |
| [11] 2016 | 3.51 | GaN-HEMT | 13.5 | 7.5 | 49.2 | 51.7 (DE) |
| [12] 2018 | 3.3-3.55 | GaN-HEMT | 5.5-12 | 7.5 | 39 | 50.6 (PAE) |
| [14] 2018 | 4.35-4.85 | GaN-HEMT | 12 | 8 | 39 | >45 (DE) |
| [19] 2017 | 2.14 | GaN-HEMT | 16 | 6.5 | 36.9 | 57 (DE) |
| [23] 2019 | 2.8-4.0 | GaN-HEMT | 10 | 6 | 36 | 35-52 (DE) |
| [24] 2021 | 3.5 | NA | 7 | 6 | 39 | 47 (PAE) |
| This work | 3.4-3.6 | GaN-HEMT | 10 | 8 | 35 | 46-52 (DE) |

## 4. CONCLUSION

In this paper, a modified DPA based on asymmetrical matching network approach has been designed and simulated successfully using ADS based on Roger 5880 substrate for the 3.4-3.6 GHz sub-6 GHz 5G frequency band. It has shown through simulation that increasing the BO efficiency can be achieved by increasing the power ratio between peaking and carrier cells through matching network design. The proposed design has achieved a drain efficiency of 46-52 % at 8-dB OBO. For future work, the proposed design needs to be investigated in terms of linearity to meet the efficiency-linearity trade-off.

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