N-TYPE PHOTOVOLTAIC CELL RE-CLAIM QUALIFICATION USING CLEANING PROCESS

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MASTER OF MANUFACTURING ENGINEERING
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A thesis submitted
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DECLARATION

I declare that this Choose an item. entitled " N-TYPE PHOTOVOLTAIC CELL RE-CLAIM QUALIFICATION USING CLEANING PROCESS" is the result of my own research except as cited in the references. The thesis has not been accepted for any degree and is not concurrently submitted in candidature of any other degree.

Signature :

Name : ROSLINA AIDA BINTI RAHIMI

Date :

APPROVAL

I hereby declare that I have checked this thesis and in my opinion, this thesis is adequate in terms of scope and quality for the award of the degree of Master of Science in Maufacturing Engineering.

Signature : .....

Supervisor Name : TS DR SAIFUDIN HAFIZ BIN YAHAYA

Date : .....

DEDICATION

This thesis dedicated first and foremost to myself. I never expected , in a million years that i would able to write this and come to this journey. I also dedicate this to my lovely daughter Arissa Hannah who are being patience when mama is not around. Thank you darling for your love , kindness and support. And finally , thank you to my parents and siblings who always there whenever i need help and support during my journey in completing this project.

ABSTRACT

Yield loss reduction is one of the continuous actions applied in the manufacturing industry to minimize overall operational costs. This study will focus on improving top defects from the diffusion process in the solar industry. In the diffusion process, scratches on the wafer surface are one of the top Pareto for scrap. One of the opportunities to improve the scrap is the cleaning and removing the diffusion layer back to its original condition before the diffusion process. The objective of the study is to study the cleaning recipe for removing the diffusion layer. Selected recipes will be qualified using reliability testing to ensure no additional impact on the product quality. The qualified cleaning recipe and the process will be validated and compared with the standard production wafer in terms of photovoltaic cell Power Conversion Efficiency, Electrical and Cosmetic Yield performance. This study uses the closed interval method in selecting the HFO_3 parameter range for the cleaning recipe and qualified using Autoclave HAST chamber (ACL) and Reverse Biased Test Dielectric (RBTDE) reliability testing to confirm the product performance is fulfilling the standard specification. The statistical analysis in this study uses JMP software and analysis conducted using t-Test, Wilcoxon Test and Mosaic Plot distribution to ensure the rework wafer quality and performance comparable with the existing production wafer. The selected cleaning recipe observed that the combination parameter of 250ml HFO_3 volume dosing and temperature of 70^{o}C HFO_3 bath showed the closest value to the existing product, which is control data. The Reliability testing result of the selected cleaning recipe passed and qualified under RBTDE and ACL tests which showed a probability value of 0.6494 for 0 hour, 0.4695 for 120hour and 0.6150, respectively, defined as an insignificant difference from the control product data. A higher volume run of the selected cleaning recipe was validated as well, which resulted better mean value at 22.94% for Power Conversion Efficiency and a higher Bin A percentage for Cosmetic Yield with a p-value of <0.0001 while the insignificant difference of Electrical Yield probability value of 0.8177 from control data. The implementation of the cleaning recipe for the diffusion layer rework process can improve the yield loss and, at the same time, benefit the industry due to the lower operational cost from the scrap reduction.

ABSTRAK

Pengurangan kehilangan hasil adalah salah satu tindakan berterusan yang digunakan dalam industri pembuatan untuk meminimumkan kos operasi keseluruhan. Kajian ini akan memberi tumpuan kepada menambah baik kecacatan teratas daripada proses resapan dalam industri suria. Dalam proses resapan, calar pada permukaan sel solar adalah salah satu pareto teratas untuk sekerap. Salah satu peluang untuk menambah baik sekerap ialah membersihkan dan mengeluarkan lapisan resapan kembali kepada keadaan asal sebelum proses resapan. Objektif kajian adalah untuk mengkaji resipi pembersihan untuk menghilangkan lapisan resapan. Resipi terpilih akan layak menggunakan ujian kebolehpercayaan untuk memastikan tiada kesan tambahan terhadap kualiti produk. Resipi pembersihan yang layak dan prosesnya akan disahkan dan dibandingkan dengan sel pengeluaran standard dari segi Kecekapan Penukaran Kuasa sel fotovoltaik, prestasi Hasil Elektrik dan Kosmetik. Kajian ini menggunakan kaedah selang tertutup dalam memilih julat parameter HFO_3 untuk resipi pembersihan dan menggunakan ujian kebolehpercayaan Autoklaf kebuk HAST dan Dielektrik Ujian Pincag Songsang untuk mengesahkan prestasi produk menepati spesifikasi standard. Analisis statistik dalam kajian ini menggunakan perisian JMP dan analisis yang dijalankan menggunakan ujian-t, ujian Wilcoxon dan taburan taburan Mosaic untuk memastikan kualiti dan prestasi sel solar kerja semula setanding dengan sel solar pengeluaran sedia ada. Resipi pembersihan yang dipilih mendapati bahawa parameter gabungan dos HFO_3 250ml dan suhu HFO_3 70^{o}C menunjukkan nilai yang paling hampir dengan produk sedia ada, iaitu data kawalan. Keputusan ujian Kebolehpercayaan resipi pembersihan terpilih lulus dan layak di bawah ujian RBTDE dan ACL yang menunjukkan nilai kebarangkalian 0.6494 untuk 0 jam, 0.4695 untuk 120 jam dan 0.6150, masing-masing, ditakrifkan sebagai perbezaan yang tidak ketara daripada data produk kawalan. Jumlah kuantiti yang lebih tinggi bagi resipi pembersihan terpilih telah disahkan juga, yang menghasilkan nilai min yang lebih baik pada 22.94% untuk Kecekapan Penukaran Kuasa dan peratusan Bin A yang lebih tinggi untuk Hasil Kosmetik dengan nilai $p < 0.0001$ manakala perbezaan Hasil Elektrik yang tidak ketara nilai kebarangkalian 0.8177 daripada data kawalan. Pelaksanaan resipi pembersihan untuk proses kerja semula lapisan resapan boleh meningkatkan kehilangan hasil dan, pada masa yang sama, memberi manfaat kepada industri kerana kos operasi yang lebih rendah daripada pengurangan kecacatan produk.

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LIST OF SYMBOLS AND ABBREVIATIONS

ACL	-	Autoclave
APCVD	-	Atmospheric pressure chemical vapor deposition
BRL	-	Boron Rich Layer
BSG	-	Borosilicate Glass
BSoD	-	Boron Spin-on Dopant
CDA	-	Clean Dry Air
CPV	-	Concentrating Photovoltaic
c-Si	-	Crystalline Silicon
CSP	-	Concentrated Solar Power
CTEG	-	Concentrator Thermoelectric Generator
CVD	-	Chemical Vapor Deposition
DI	-	Deionized
DSSC	-	Dye Sensitized Solar Cell
EL	-	Electroluminescence
HAST	-	High Accelerated Stress Test System
HCL	-	Hydrochloric Acid
HCPV	-	High Concentration Photovoltaics
HF	-	Hydrogen Fluoride
HFO_3	-	Fluoric acid
HNO_3	-	Nitric Acid
IBC	-	Interdigitated Back Contact
IR	-	Infrared
KOH	-	Potassium Hydroxide
LCPVs	-	Low Concentrator Photovoltaics
$NaNO_2$	-	Sodium Nitrite
PCT	-	Pressure Cooker Test
PECVD	-	Plasma Enhanced Chemical Vapor Deposition
poly c-Si	-	polycrystalline

PSG	-	Phosphorus Silicate Glass
PV	-	PV
PN		P-type - N-type
RBTDE	-	Reverse Biased Test Dielectric
SEM	-	Scanning Electron Microscopy
SiH_4	-	Silane
SiNx	-	Silicon Nitride
SiO_2	-	Silicon Oxide
SiOx	-	Amorphous Silicon Oxide
USPCT	-	Unsaturated Pressure Cooker Test

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CHAPTER 1

INTRODUCTION

1.1 Background

There is always demand for cost reduction in the manufacturing industry in order for a company to sustain or stay relevant in the industry. Cost reduction can be in terms of labour utilization, switching to alternative material with a cheaper cost, or it can be from scrap yield loss reduction. This study will focus on scrap yield loss reduction and identify rework methods using cleaning machines to improve the yield loss.

The rework process is standard in the industry to reduce yield loss costs to the company. There is numerous method of rework applied in the industry. However, it is crucial to ensure the rework process does not jeopardize the quality of the product. This study will utilize a cleaning machine of N-type silicon photovoltaic technology for rework flow with reliability testing and experiment validation to ensure no additional impact on the quality of the product.

Photovoltaics (PV) is one of the most rapidly growing energy generation options in the modern energy sector. Because of favourable energy policies, PV is one of the primary renewable energy sources being adopted globally to reduce greenhouse gas emissions in the energy sector. Moreover, its unique selling point of scalability and adaptability to any regional condition contributes to its rapid dissemination and successful implementation in various global regions (Kumar et al., 2020). Photovoltaics (PV) generates electricity that utilizes semiconductors that exhibit the photovoltaic effect to convert solar radiation to direct current electricity. Photovoltaic energy generation utilizes solar panels comprised of several

photovoltaic solar cells. These cells are assembled into solar panels as part of a photovoltaic system to generate solar power from sunlight. (Kurtz, 2012).

N-type silicon has more electrons than silicon, including phosphorus (making it negatively charged). In contrast, P-type silicon has fewer electrons than silicon and uses boron (making it positively charged cells). For crystalline silicon photovoltaics, the most efficient modules are produced from N-type silicon wafers. This is because N-type silicon seems to have a much higher tolerance for defects than P-type silicon (Macdonald, 2012).

In crystalline silicon photovoltaics, a WET cleaning machine is one of the critical processes that can perform silicon thickness etching and clean the wafer from contamination that adheres to the surface cell. Wafer cleanliness is essential for preparing the wafer before loading downstream or the next process step. On the other hand, a bad cleanliness wafer may cause other quality issues such as bad deposition and printing issues that will lead to electrical junction issues and rejection in the cell tester process. Reject wafers can be considered a loss to the company, and engineers are working hard to ensure fewer rejects or scrap for better yield performance.

1.2 Problem Statement

In the manufacturing industry, scrap is usually generated from a failure in a process. Therefore, an industry maker needs to work towards scrap reduction as it will directly impact the overall operational cost. Scrap somehow can either be discarded, recycle or reworked to salvage it. In photovoltaic wafer manufacturing, one of the biggest scrap issues happens in the boron diffusion process due to operator manual handling. Manual handling is usually because of automation failure that requires manual collection of the wafer in the reject bin. Those defect wafers must be scrapped and thrown away as the handling causes scratches on

the diffusion layer that will be captured as electrical shunt loss at the end of the line cell tester.

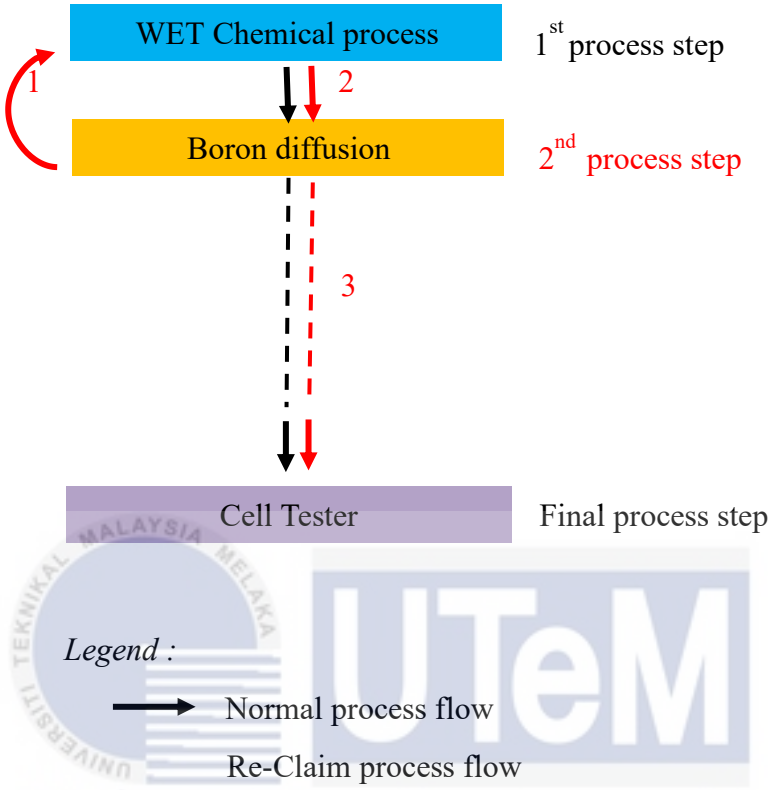


Figure 1.1: Silicon Cell Processing – Normal and Re-Claim Flow (Neuhaus and Münzer, 2007)

There is an opportunity to rework or salvage the scrap wafer if the diffusion layer can be entirely removed and cleaned like the original bare silicon wafer. One of the methods that can perform the boron diffusion removal is the WET chemical process. For this rework process flow, the re-claim will require the wafer for the second run in WET Chemical (cleaning module) to remove the diffusion layer. In this study, developing the cleaning recipe is critical to ensure the cleaning module can remove the diffusion layer and the re-claim flow illustrated in Figure 1.1.

The selected recipe will be verified through reliability testing to ensure the recipe will not impact the product quality. At the same time, monitoring of the N-type silicon

thickness is also needed after the re-claim process to ensure no reduced thickness of the silicon layer. Validation of the actual performance of the cleaning recipe will be needed, and the result should be analyzed. It will not cause issues regarding Power Conversion Efficiency, Electrical Yield, and Cosmetic Yield. This study's success will help improve the operational cost as no more wafers will be thrown away and scraped if the defective wafer undergoes the re-claim cleaning process.

1.3 Objectives of the Study

The research objectives for this are such as :

a) To study the cleaning recipe in removing diffusion layer using HFO_3 parameter of chemical dosing volume and bath temperature range.

b) To qualify the cleaning recipe using Reverse Biased Test Dielectric (RBTDE) and Autoclave HAST chamber (ACL) Test for Reliability Testing.

c) To validate experimantal run data of Power Conversion Efficiency (EFF), Electrical Yield and Cosmetic Yield performance of the selected cleaning recipe using JMP Statistical Analysis software.

1.4 Scope of Study

The scope of this research is only suitable for improving defects with scratches in the diffusion process. To remove the diffusion layer, the rework flow will utilize a cleaning module in N-type photovoltaic cell manufacturing. The selected cleaning recipe will be qualified using reliability testing to ensure no other product quality. The wafer that has undergone a cleaning process will be validated from the experimental run and analyzed using JMP software to confirm that this change will cause no impact on the product cell Power Conversion Efficiency, Electrical Yield, and Cosmetic Yield.

1.5 Contribution of Research

Contributions of this thesis are made in the following related areas as the cleaning recipe study will be conducted on $HF0_3$ parameter chemical dosing volume and bath temperature range. The selected recipe will be chosen based on higher effectiveness in removing the diffusion layer. This study approach to the cleaning parameter will develop a cleaning recipe that can remove the damaged diffusion layer defect, thus improving product yield loss.

Verifying the cleaning recipe through reliability testing will ensure that the recipe will not cause product performance degradation. The passing reliability test will ensure that the cleaning recipe will not impact the cell function and is reliable up to the committed product warranty.

The experimental run using a cleaning recipe will provide data for an analytical study on product performance. The analysis conducted using JMP statistical software will able to tabulate Power Conversion Efficiency (EFF), Electrical and Cosmetic Yield performance. The validation result of the experimental data versus the existing product will confirm that the cleaning recipe will not cause additional product issues once implemented.

1.6 Thesis Organization

Chapter 1 presents the background of the study, research problems, objectives of the study, scopes of the study, contributions and significance of the study.

Chapter 2 covers on literature study that starts with a brief overview of current solar technology such as Solar Thermoelectricity, Dye Sensitive Solar Cell (DSSC), Concentrated Solar Power (CSP) and Photovoltaic (PV) Solar Panels. This study mainly uses Photovoltaic (PV) Solar Panels, so a summary of different photovoltaic technology like Thin Film PV modules, Concentrated PV modules and Crystalline Silicon PV modules will be included.

This chapter explains Crystalline silicon type, Monocrystalline and Polycrystalline silicon, and N-type silicon manufacturing. Then, this chapter presents various literature on various methodologies in the diffusion and cleaning development process in silicon photovoltaic manufacturing.

Chapter 3 explains the methodology developed to qualify the cleaning recipe for removing the diffusion layer. The concept of Extreme Value Theory (EVT) will be explained in this chapter for parameter range selection of HFO_3 chemical dosing and temperature. The qualification study describes the selection of the best cleaning recipe in this chapter. The best cleaning recipe will be submitted for two types of reliability testing: Autoclave HAST chamber (ACL) and Reverse Biased Test dielectric (RBTDE). Validation of the cleaning recipe will be made through a high volume and small quantity experimental run. The step by step of JMP analysis using t-Test, Wilcoxon Test and Mosaic Plot distribution will be included in this chapter for further understanding of product conformance verification to Power Conversion Efficiency, Electrical Yield and Cosmetic Yield.

Chapter 4 presents the result and discussion of this study. The qualification result of visual inspection, microscopic inspection and boron layer thickness measurement data will be shared in this chapter. The result of the selected cleaning recipe will be analyzed and verified from two types of reliability testing: Reverse Biased Test Dielectric (RBTDE) and Autoclave HAST chamber (ACL). The experimental validation result from Power Conversion Efficiency (EFF), Electrical Yield, and Cosmetic Yield will be analyzed using JMP software and compared with the existing product quality performance.

Chapter 5 summarize the study and recommend future works. This chapter will include the study's main conclusions and achievements of the study and suggests areas for future work.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction to Solar Technology

The world's energy demand is rapidly increasing due to population growth and technological improvements. It is consequently critical to choose a stable, cost-effective, and continuous renewable energy source for future energy demand. Like other renewable energy sources, solar energy is a promising and readily available source of energy for addressing long-term difficulties in the energy crisis. Because of the tremendous need for energy, the solar business is steadily growing worldwide, despite the fact that the main energy source, fossil fuel, is finite and other sources are expensive. It has become an instrument for developing countries' economic position and sustaining the lives of many poor people because it is now cost-effective due to years of intensive research to speed up its growth. Compared to other renewable energy sources, the solar sector would undoubtedly be the best alternative for future energy demand because it is readily available, cost-effectiveness, accessibility, capacity, and efficiency (Kannan and Vakeesan, 2016).

2.2 Types of Solar Technology

Solar technologies are currently available in a variety of design. However, each is dependent on a different set of principles and research, and each has its own set of benefits. Analysis and comparison of several technologies will assist in selecting the most effective and helpful technology for a given set of circumstances. The overview of available solar technology simplified and lay out in Figure 2.1.

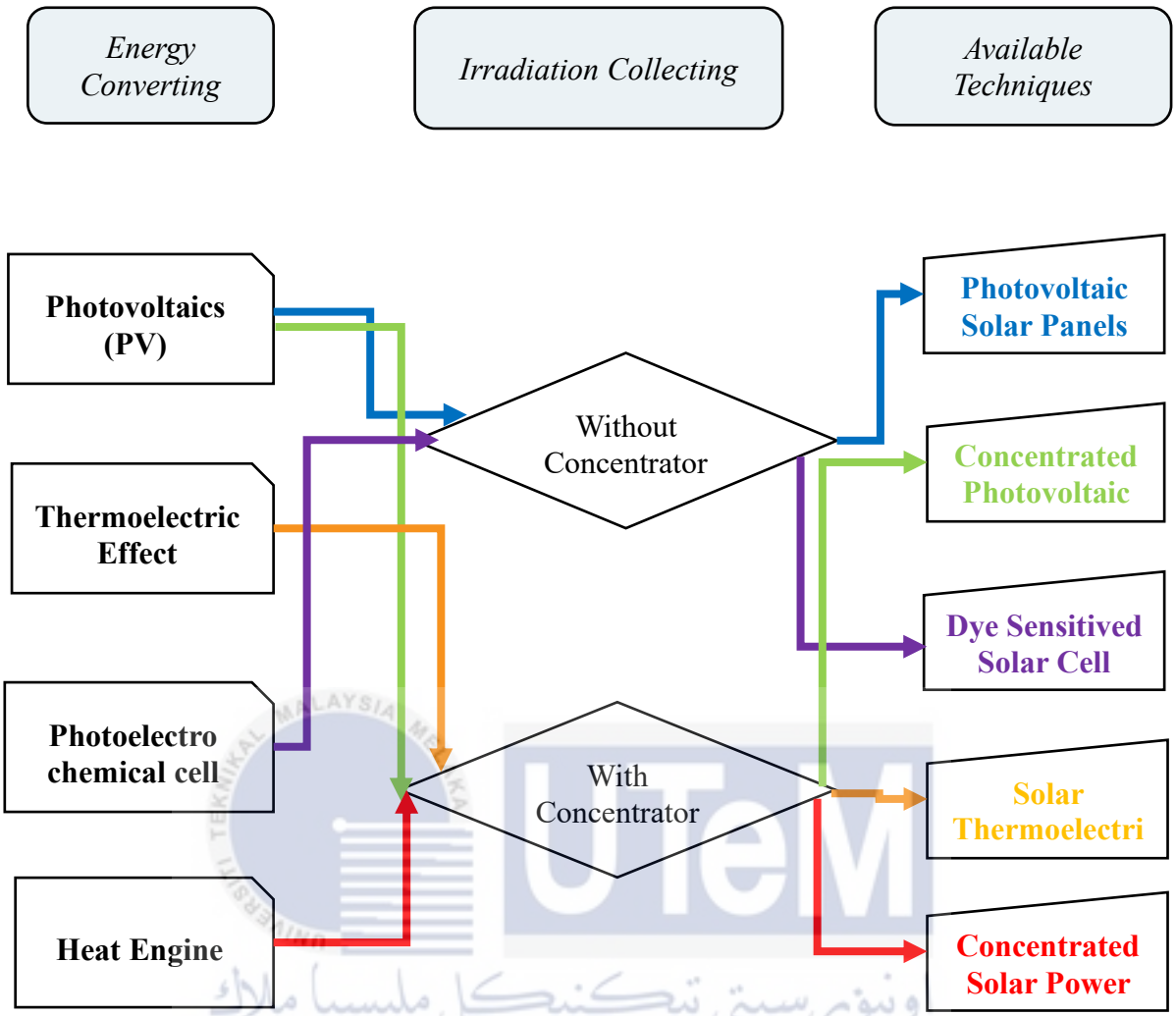


Figure 2.1: Overview of Solar Technology (Chu and Meisen, 2011)

2.2.1 Solar Thermoelectricity

Solar thermoelectricity utilizes the thermoelectric effect by using parabolic disc technology. A concentrator thermoelectric generator (CTEG) is used to generate electricity. A thermoelectric device is made of two components. IT generates energy by converting temperature differentials between two parts into volts via a semi-conductor.

In contrast, a temperature difference is created when a voltage is provided to a device. At the atomic level, a temperature gradient induces the movement of charged carriers in

material from the hot to the cold side. We can now observe that it works in spacecraft and vehicle engine systems. Solar thermoelectricity is a relatively new concept in the laboratory and has not matured sufficiently to fulfil market requirements. However, it offers numerous unique benefits and will almost certainly occupy a niche market in the future. Due to the thermoelectricity generator's unique characteristics and use of low-grade thermoenergy, it should be used in conjunction with other solar technology systems (Chu and Meisen, 2011).

2.2.2 Dye Sensitized Solar Cell (DSSC)

A dye-sensitized solar cell (DSSC) is a photoelectrochemical system comprised of a semiconductor produced between a photo-sensitized anode and an electrolyte. DSSCs operate at a high rate of efficiency. Due to their "depth" within the nanostructure, photons have a very high probability of being absorbed, and the dyes are incredibly effective at converting them to electrons. Most of the system's small losses are caused by conduction losses in the TiO_2 and transparent electrodes or optical losses in the front electrode. DSSC technology may not be attractive for large-scale installations because higher-efficiency cells are more viable but much more expensive. However, even slight improvements in the efficiency of DSSC conversion may make them viable for some of these roles(Chu and Meisen, 2011).

2.2.3 Concentrated Solar Power (CSP)

Concentrated solar energy systems use mirrors or lenses to focus a huge amount of sunlight, or solar thermal energy, onto a small area. When concentrated light is converted to heat, it powers a heat engine (often a steam turbine) coupled to an electrical power generator (Sawin, 2011). Unlike photovoltaic solar cells, CSP systems convert energy from sunlight

to electricity through a heat engine, rather than the photovoltaic effect, which converts photon energy directly into electricity energy (Chu and Meisen, 2011)

2.2.4 Photovoltaic Solar Panels (PV)

Photovoltaic modules are considered to be the first generation of solar panels configurations (Mathew et al., 2018). Photovoltaics (PV) generates electricity that utilizes semiconductors that exhibit the photovoltaic effect to convert solar radiation to direct current electricity. Photovoltaic energy generation utilizes solar panels comprised of a number of photovoltaic solar cells. Monocrystalline silicon, polycrystalline silicon, amorphous silicon, cadmium telluride, and copper indium gallium selenide/sulfide are currently utilized in photovoltaics. Solar photovoltaic panels are the most often utilized solar technology for generating power (Kurtz, 2012).

2.3 Type of Photovoltaic Module

2.3.1 Thin-Film PV Modules

Thin-film photovoltaics module is made up of many solar cells that are connected by wires. A generic anatomy layout of a thin layer solar cell is shown in Figure 2.2. The semiconductor was sandwiched between two sheets of glass and sealed with an industrial laminate in a conventional thin-film solar panel. To minimize light reflection from the surface of the panels, an anti-reflective coating is usually applied. Thin-film modules use numerous thin absorbing layers that are less than 300 times thinner than traditional crystalline silicon (c-Si). PV active layers range in thickness from a few nanometers to tens of micrometres. One of the essential objectives of thin-film module production is to lower the high cost of producing monocrystalline and polycrystalline silicon modules. On the other

hand, thin-film modules are less powerful and durable than crystalline c-Si solar panels (Kumar et al., 2020).

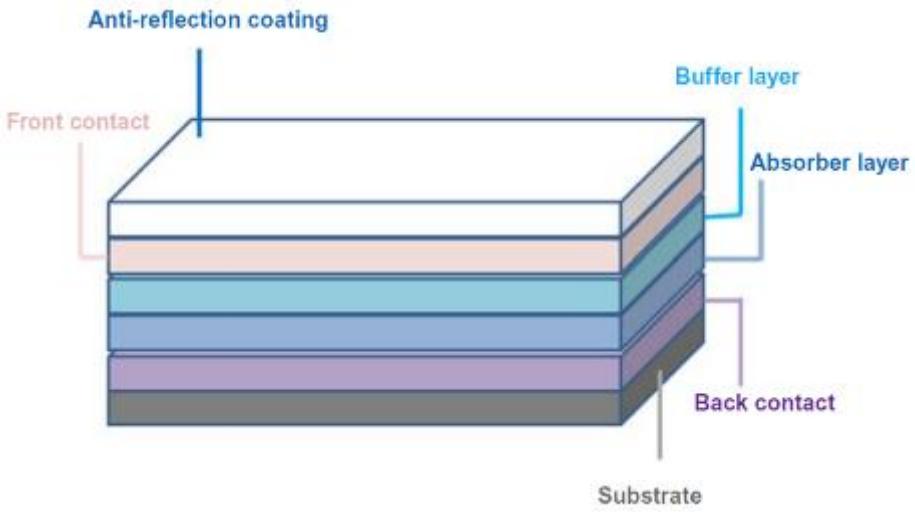


Figure 2. 2: A Thin Layer Solar Cell Anatomy (Kumar et al., 2020)

2.3.2 Concentrated PV Modules

Concentrating PV (CPV) uses mirrors and lenses to collect large amounts of sunlight. The technology has progressed to the point that it now achieves the highest efficiency level. At the same time, these modules are quite expensive, making them unsuitable for traditional PV applications. However, these modules are mainly employed for space applications to justify their expense. Multijunction solar cells from the III-V semiconductor group (alloy having elements from groups III and V in the periodic table) are commonly employed in high concentration photovoltaics (HCPV), making this technology more difficult to mass-produce. Various systems and technologies have arisen since PV was integrated into the electricity market. High-efficiency multijunction cells are used in most CPV modules, and they are optically addressed to concentrate the largest amount of sunlight (Bett et al., 2006).

According to Philipps et al. (2015) , CPV modules perform best in geographic areas with high levels of direct normal irradiance (DNI), often above 2000kWh/(m2a) despite of its smaller cell size. The use of collectors and mirrors in CPV modules concentrates the

incoming irradiance. Fresnel lenses, Cassegrain primary reflectors, and waveguiding devices are examples of their optics (Sellami and Mallick, 2013).

High concentrator Photovoltaics (HCPVs) and Low Concentrator Photovoltaics (LCPVs) are the two types of concentrators found in CPVs. Solar cells from the III-V semiconductor group are used in HCPVs, designed with double-axis sun trackers to concentrate the light with intensities ranging from 300 to 1000 suns. LCPV systems are made of c-Si or other semiconductor materials, and they can contain double or single-axis trackers that concentrate light with an intensity less than 100 (Belkasmi et al., 2014 , Burhan et al., 2016). The typical examples of solar concentrators and the parabolic dish concentrator are shown in Figure 2.3.

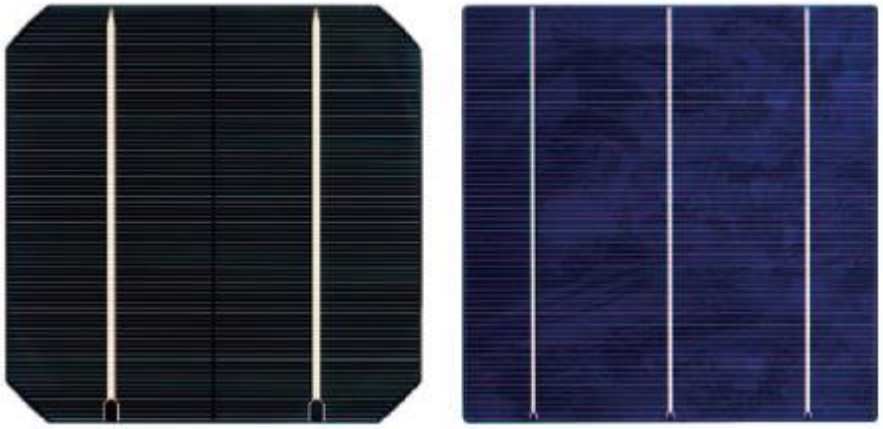
(a) (b)

Figure 2.3: (a) Fresnel Lenses Solar Concentrator and (b) Parabolic Dish Concentrator (Kumar et al., 2020)

2.3.3 Crystalline Silicon PV Modules

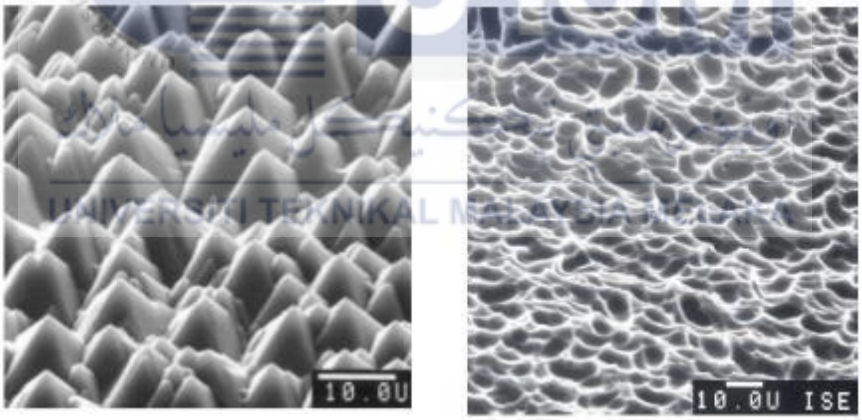
Two distinct types of c-Si modules are available in the industry are polycrystalline (poly c-Si) and monocrystalline (mono c-Si) while the Solar Cell and SEM images of the differences shown in Figure 2.4 and Figure 2.5. These modules constructed by interconnecting c-Si photovoltaic cells in series and parallel configurations (Mathew et al.,

2018). In terms of cell structure, c-Si photovoltaic cells are made up of silicon slices typically visible as wafers. These wafers were used to create the c-Si cells, which are subsequently joined manually by adding the electrical contacts (Duflou et al., 2018).



(a) (b)

Figure 2.4: Solar Cell of (a) Monocrystalline Silicon and (b) Polycrystalline Silicon (Di Vece,2019)



(a) (b)

Figure 2.5: SEM Images of (a) Monocrystalline Silicon and (b) Polycrystalline Silicon (Glunz et al., 2012)

Duflou et al. (2018) illustrated a simplified structure of a crystalline silicon photovoltaic module shown in Figure 2.6. The silicon solar cells are coated with a silver-and-aluminum metallization paste and connected via silver-coated copper bus bars. Antimony-containing, low-Fe hardened glass provides long-term physical protection and

good light transmission. The sandwich structure is completed on the non-illuminated side by a polymer layer, typically PET. PV panels are frequently constructed and placed using an aluminum frame. A junction box adhered to the backside includes the electronic components that connect the solar cell chains to the photovoltaic network (Duflou et al., 2018).

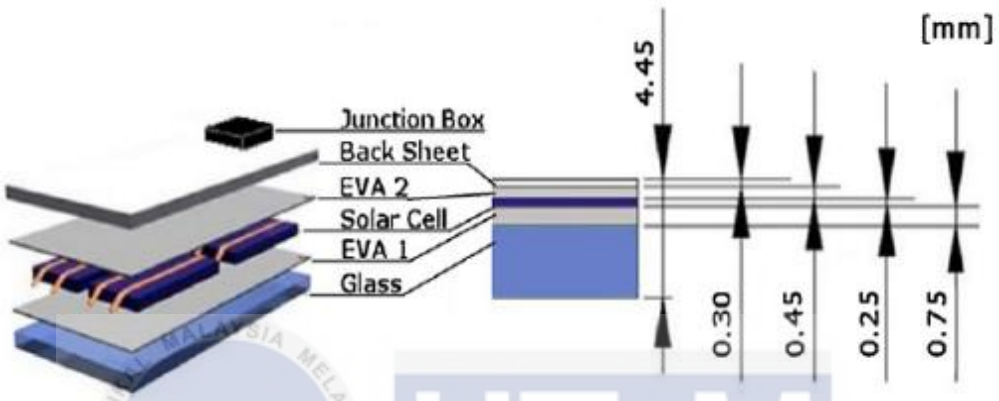


Figure 2.6: Structure of Crystalline Silicon PV Module (Duflou et al., 2020)

2.3.3.1 Monocrystalline Silicon (Mono c-Si)

This c-Si module is widely used and will become the PV market's leader. These modules appear to be widely available now, and the existing benefits are considerable. Low cost is the sole primary motivator. P-doped wafers with P–N junctions are employed to produce c-Si modules. The c-Si ingot is initially created during the fabrication process. After that, the c-Si ingot is sized into wafers with less than 0.3mm thickness. Under full lighting conditions, this produces the total solar cell structure, which can generate a 35mA current at 0.55V. These modules typically have a unique textured surface that resembles a pyramid structure. Such solar cells are put together to form a PV module based on the required voltage and currents. These cells are placed in series and parallel patterns with conductive contacts while constructing the module (Parida et al., 2011 and Kumar et al., 2020).

2.3.3.2 Polycrystalline Silicon (Poly c-Si)

The poly c-Si PV module is the next c-Si PV module, with a slightly lower market than mono c-Si. Metal contamination is an issue with mono c-Si cells; hence the industry has developed poly c-Si cells to address it. Modules are arranged in series and parallel arrangements, just like mono c-Si. Different crystal forms are used in the manufacturing of the cells. Silicon is melted and then solidified. Crystals with only one orientation are created in this method, formed into thin blocks and eventually wafers. These solar cells have random shapes on their surfaces and an extra layer that reduces light reflection (Parida et al., 2011,Kumar et al., 2020).

2.3.4 Fundamental Structure of Crystalline Silicon Solar Cell

According to Glunz et al. (2012), a functional solar cell requires at least three necessary elements. First, an absorber was required, absorbing photons and converting their energy to an excited state of a charge carrier. The absorber is often a semiconductor such as silicon. The absorption process generates an electron in the conduction band where an electron from the valence band is transported to the conduction band, leaving a "hole" in the valence band. Second, a membrane prevents the excited carrier from recombining to its ground state. This recombination converts the electron's excitation energy into the excitation energy of a photon, which sends its power to another previously excited electron or a lattice vibration. The PN-junction, created by adjacent areas of p- and n- conducting semiconductor layers, is used in current technology. Third, contacts that allow carriers to be collected and connected to other solar cells or an external load.

2.3.4.1 N-type and P-type Silicon

The most efficient modules are produced from N-type silicon wafers. This is due to the fact that N-type silicon seems to have a much higher tolerance for defects than P-type silicon (Macdonald. 2012)

N-type silicon wafers represent a substantial possibility for high-efficiency silicon solar cells commercially. The stability of recombination and device parameters has been demonstrated under illumination. Solar cells manufactured on multi-crystalline, Czochralski, and float-zoned wafers have been claimed to have a high lifetime. In contrast, solar cells made on N-type wafers are presently reported to have high efficiency. Regarding feedstock considerations, the growing list of defects with a high hole lifetime and a low electron lifetime and the effect of associated a-SRH recombination on the terminal characteristics of solar cells suggests that N-type silicon wafers are more suitable for high-efficiency commercial silicon solar cells. For industrial manufacturing processes, the excellent resistance of N-type wafers to induced or introduced faults indicates the same. In general, N-type wafers appear to have a significant advantage over P-type wafers in terms of the electrical requirements of a solar-grade wafer for industrial high-efficiency silicon solar cells (Cotter et al., 2006).

The issues do not appear to be dire in the broader perspective of the P-type versus-N-type debate. The cost of N-type wafers is comparable to that of P-type wafers. Module manufacturing technology should manufacture N-type solar cells, and system integrators should have no difficulty integrating N-type modules. The most significant challenges are diffusion technology (particularly, producing the p+ emitter), metallization technology, and the unusually high phosphorus segregation resulting in doping fluctuations during crystal growth. While more challenging than phosphorus diffusion, Boron diffusion is not impossible with caution, and positive results with printed and plated metallization have

already been described. Tolerance for changes in wafer doping will necessitate some vigilance. New device concepts and designs are already based on N-type solar cells developing. N-type silicon wafers represent an undeniable opportunity for high-efficiency commercial silicon solar cells (Cotter et al., 2006).

According to study made by Yin et al. (2020) the contact ratio of the emitter and the thermal drive-in duration optimized to achieve a 22% conversion efficiency in N-type silicon solar cells with boron-doped rear emitter and phosphorus-doped front surface field (FSF) . On the other hand , Shanmugam et al. (2019) proved that front boron-diffused emitter and a rear phosphorus diffused back surface yield for N-type silicon observed excellent reverse bias characteristics with a reverse current of only 3 mA at −10 V for the APCVD process flow without diffusion masks.

2.3.5 Crystalline Silicon Cell Processing

The manufacturing of crystalline silicon cell in industrial operations start with the wet etching and cleaning techniques prior to diffusion process. A random texture is generated using a simple texturing technique on the front side. Silicon nitride is deposited using APCVD and PECVD. To lower fabrication costs, the design for boron and phosphorus diffusion on the reverse side of IBC solar cells was produced using low-cost screen-printing technology to substitute photolithography in their manufacture (Cudzinovic and McIntosh,2002). Silicon dioxide forms on the entire rear side, and a pattern of holes in the oxide is developed in the diffused boron and phosphorus locations. Aluminum is deposited as the initial metal layer on the planar silicon dioxide covered rear side and structured to correspond to the p- and n-doped regions for improved light reflection. Electrical conductivity is achieved by plating the patterned aluminum portions with Ni to act as a diffusion barrier and achieve a high contact resistance against Cu. A flash of Ag follows Ni

plating to protect the Cu. After that, the solar cell construction process is completed with an annealing phase to ensure proper contact formation. The IBC solar cell structure is depicted in Figure 2.8, and the solar cell production methods extrapolated from (Mulligan et al., 2004) showed in Figure 2.7 (Neuhaus and Münzer, 2007).

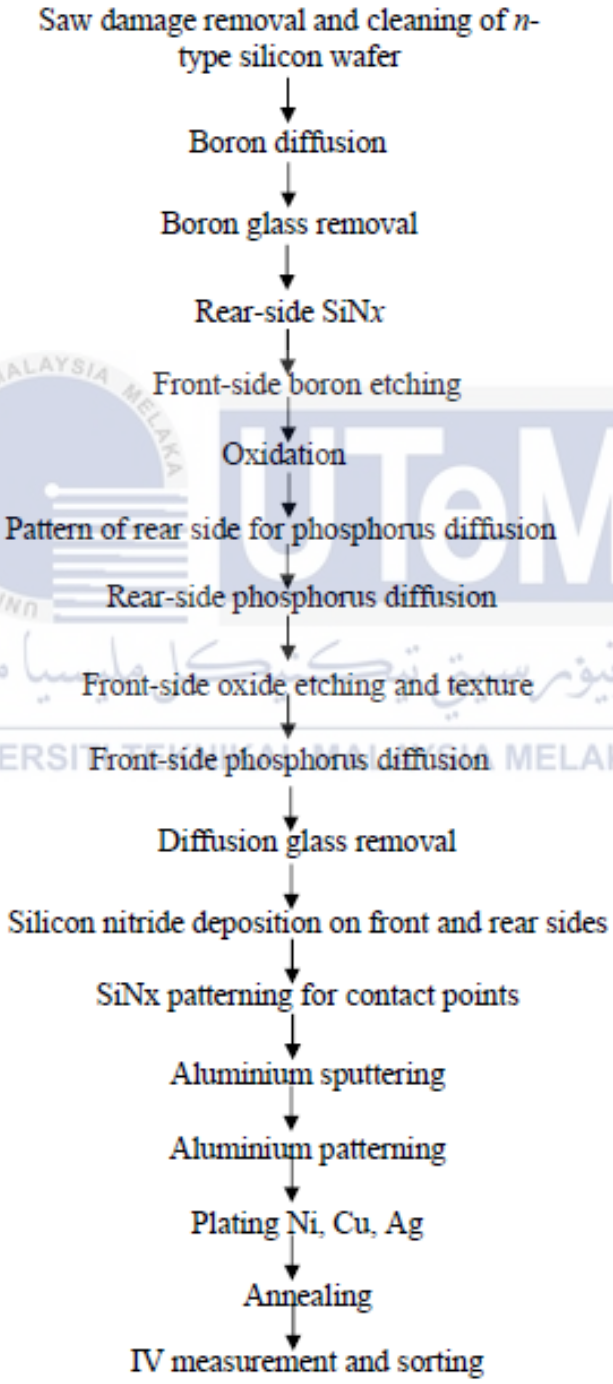


Figure 2.7: IBC Solar Cell Fabrication Step (Neuhaus and Münzer, 2007)

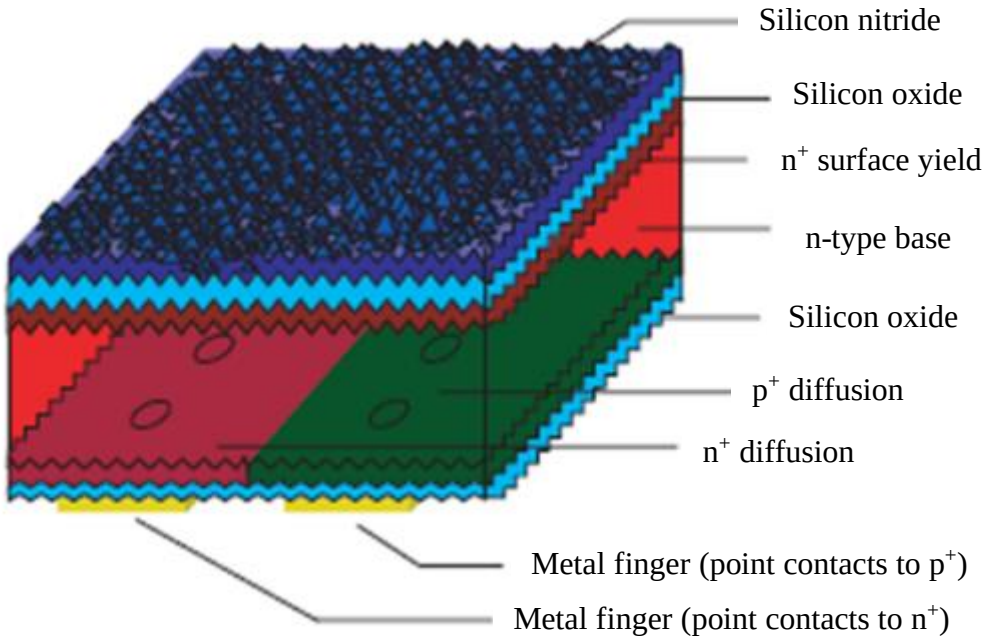


Figure 2.8: IBC Solar Cell Schematic Drawing (Neuhaus and Münzer, 2007)

2.3.6 Silicon Cell Processing – Atmospheric Pressure Chemical Vapor Deposition (APCVD)

As the name implies, Atmospheric pressure chemical vapor deposition (APCVD) procedures take place at atmospheric pressure (i.e., 1 atmosphere = 101,325 Pa = 760 Torr). APCVD is compatible with vacuum-free, continuous in-line processes; it is particularly well-suited for cost-sensitive, high-Atvolume manufacturing applications such as photovoltaic cell fabrication (Davis,2015). APCVD-deposited borosilicate glass layers (BSG) as a doping source used in Meier et al. (2018) study on the effect of oxygen concentration on boron diffusion at temperatures ranging from 875°C to 950°C. There are low saturation current densities reported at peak temperatures of 875 °C at a resistance of Rsh = 121 /sq (planar surface, Al2O3/SiNx passivation) of J0 = 16 fA/cm2. This is critical because, depending on the amount of boron and the temperature of the process, high oxygen concentrations lead to the decoupling of the doping source completely.

As illustrated in Figure 2.9, N_2-diluted precursors are delivered to a CVD injector zone isolated from the rest of the system by N_2 gas curtains. Since the deposition is carried out at atmospheric pressure and the CVD injectors are separated, numerous CVD injectors can be included in a single system, allowing for the deposition of multilayer films in a single process run. The principal single-lane system consists of a continuously moving Ni alloy (Inconel 601) belt that takes the wafers through preheating zones and three N_2 isolated CVD injectors (Davis, 2015).

Borosilicate glass (BSG) layers deposition by atmospheric pressure chemical vapor deposition investigated by Meier et al. (2019) for their effect on boron diffusion at 950°C under various oxygen concentrations. It follows that a variety of parameters, such as BSG layer boron content and high-temperature step oxygen content, are varied during fabrication. Sheet resistance and electrochemical capacitance voltage measurements are used to determine the boron doping profile as part of the characterization process. An other method of determining the recombination parameters of an oxygen-diffused surface is quasi-steady-state photoconductance measurements. Low recombination current densities J0 of J0 are recorded with a sheet resistance of 54 /sq.

Study made by Chen et al. (2019) observed that in order to have higher efficiency by adjusting the phosphorus contents in the PSG layer, the APCVD process is further improved. A lower phosphorus content (greater BSF sheet resistance) increases cell Jsc, whereas a higher phosphorus content (better rear contact resistance and low BSF sheet resistance) results in a high fill factor (FF). It is more difficult to produce N-type solar cells than P-type Si solar cells. The boron-doped rear emitter and phosphorus-doped front surface field (FSF) are generated by Yin et al. (2020) in a single high-temperature phase in the production of N-type silicon solar cells. The conversion efficiency of N-type solar cells can be increased by adding a selective FSF structure. The contact ratio of the emitter and the length of the thermal

drive-in were optimized, resulting in a record-breaking batch conversion efficiency of 22%. Yin et al. (2021) proposed using a single high-temperature operation to create the boron-doped emitter and the phosphorus-doped back surface field (BSF) on N-type silicon photovoltaic cells. The conversion efficiency of solar cells can be enhanced by introducing a selective BSF structure that is produced via laser doping.

A variety of boron emitter profiles (emitter surface concentration vs. emitter junction depth) were tested by Mojrová et al. (2016) on n-PERT solar cells. Cell-level efficiency is improved by using deeper doping profiles since metal recombination losses are significantly increased when using shallow doping patterns. It was shown that a lower RSh resulted in improved passivation regardless of emitter depth.The SiOx layer on top of BSG serves as a phosphorus cross-doping masking layer as well as a boron out-diffusion blocking layer. A research made by Ryu et al. (2018) on co-diffusion of BSG/SiOx stack formed by APCVD and a $POCl_3$ back surface field diffuse into the wafer to generate the boron doped emitter and phosphorus doped back surface field in a single high temperature stage. After removing the boron rich layer, the initial sheet resistance was 76 Ω/ with good uniformity, and the final p+ emitter sheet resistance was 97 Ω/. Additionally, the bulk lifetime increased the bulk lifespan from 1.2 to 1.5 ms in a $POCl_3$ gettering effect.

In the boron diffusion process, a boron-rich layer (BRL) is typically produced on the surface of a silicon wafer, and the BRL can significantly limit the effective carrier lifespan. Bulk lifetime deterioration occurs as a direct result of boron rich layers (BRLs), which are frequently formed during the manufacture of N-type crystal silicon solar cells with boron diffused emitters (Singha and Solanki,2016, Ryu et al., 2016).Yu et al. (2017) employed high temperature nitric acid(HT-HNO_3), chemical etching treatment(CET), and low temperature thermal oxidation (LTO) oxidation to remove BRL from the surface. Compared to other approaches, the CET method has less impact on doping profiles but has a bigger

impact on surface reflectivity. Singha and Solanki (2016) use hot HNO_3 along with a diluted dopant source and in situ oxidation can completely remove BRLs 50 nm thick on the emitter surface in this study. Hou et al. (2018) create boron-doped silicon (Si) solar cells, boron diffusion is used in an open-tube furnace using borontribromide (BBr_3), which serves as the precursor. It has been shown from this study that chemical etch treatment (CET) with the right etching time can be an effective way to remove BRL using three distinct ways that were used to examine their impact on device performance with resulted Voc of 680 mV, which is rather high. It is supported by Jiang et al. (2019) that no degradation in bulk lifespan would be caused by using chemical etch treatment (CET) to entirely remove the boron-rich layer (BRL)which observed efficiency of 21.17%.

According to study made by Ryu et al. (2016) describe that gradual removal of the boron rich layer (BRL) enhances surface passivation and bulk lifespan in the completed cell, however over-etching causes a sharp decrease in fill factor due to higher n-factor and series resistance for N-type silicon. Mihailetchi et al. (2018) offer a method for passivating p+ - doped regions by combining in situ produced SiO_2 with a plasma-enhanced-chemical-vapour-deposited SiNx layer. The BSG layer etching rate in a hydrofluoric acid (HF) solution varies across the wafer. The etching rate is determined by the BSG's local B_2O_3 composition and is significantly higher than the SiO_2 layer. The variation in etching rates can be utilized to controllably etch back the BSG layer, resulting in a thin and uniform passivating oxide layer for solar cell applications. Other studies made by Tao et al. (2017) proved that front-junction N-type Si solar cell with APCVD deposited shows excellent performance with a high Voc of 682.8mV and efficiency of 21.04 % of etch-back procedure on heavily boron doped emitter by developing porous Si in a proper chemical solution with $NaNO_2$ catalyst and then removing it. On the other hand, the boron-rich layer (BRL)

formation can be reduced by diluting the boron spin-on dopant (BSoD) source, in situ oxidation and hot HNO_3 treatment followed by a 2% HF dip.

A method for blending sintering aids is proposed by Chen et al. (2021) as a way to digest the SiO_2 layer and eliminate contaminant boron from diamond wire saw silicon powder waste (DWSSP). Pressure-less sintered DWSSP-ceramics were made at 1300°C, and low-boron silicon was removed by smelting treatment. After just 10.11 wt % of sintered aids were mixed with DWSSP, the findings revealed that an ideal removal effect of 45.32 % was achieved. Similar study performed by Qian et al. (2021) on boron removal using electroslag remelting (ESR) that relies on the dynamic refinement of Si alloy moving through the slag layer in droplet form, which discovered to remove more than 80% of the B and P during this process. Droplet entrance into the slat rises linearly with droplet size under the same slag condition and specific droplet surface area also plays an important effect in the removal of Boron.

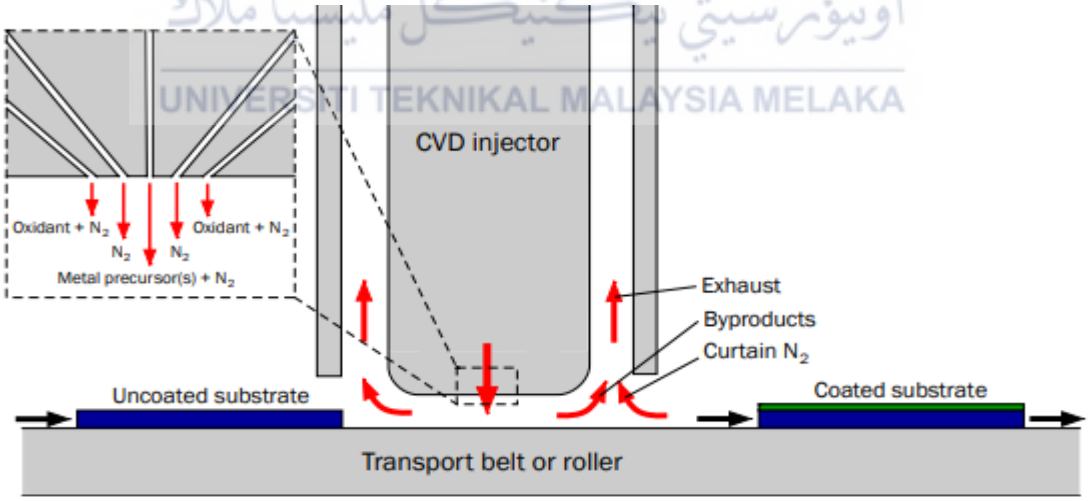


Figure 2.9: APCVD Process Diagram (Davis, 2015)

On the other hand for technology of PERT (Passivated Emitter, Rear Totally diffused) solar cells based on N-type crystalline may benefit from a low-cost co-diffusion

stage thanks to the deposition of single-sided doped glass layers. Precursor gases such as diborane, phosphine and oxygen are used to deposit layers of high-quality borosilicate glass (BSG) or phosphorus silicate glass (PSG). For BSG and PSG, Geml et al. (2020) exhibit the effects of an atmospheric treatment and a capping layer, respectively PERT solar cells may be made using high-efficiency, low-cost emitters dispersed from these glasses.

2.3.6.1 Diffusion Layer - Silicon Oxide

SiO_x deposition through APCVD has been extensively studied, notably within the integrated circuit research and development community. Perhaps the most often used method employs SiH_4 and O_2 as precursors at a substrate deposition temperature (T_{dep}) of ≈400-450ºC (Barron,2013). This results in a nearly stoichiometric SiO_2 coating when the precursor gas ratio is optimized (O_2 to SiH_4). This is the principal technique employed in this work, which results in SiO_x sheets (x ≈2) with optical characteristics identical to SiO_2. Intrinsic SiOx is employed as an intermediate rear reflector layer for rear passivated cells and as a capping layer to prevent phosphorus and boron atoms from escaping during doping processes (Davis, 2015).

2.3.6.2 Diffusion Layer - Borosilicate Glass

Borosilicate glass (BSG) films can be created by adding a dopant-containing hydride (in this case, diborane, B_2H_6) to the SiOx precursors SiH_4 and O_2. Boron concentration is extremely adjustable within these silicate sheets. BSG is considered as a boron dopant source for c-Si solar cells in this work. This is especially applicable when p+ emitters are formed in N-type cell topologies (Davis, 2015). Heilig et al. (2019) employed doping source for laser drive-in on mono-crystalline silicon wafers, APCVD silicate glasses. Doping profiles that are 100–200 nm deeper are caused by the existence of shallow emitters prior to laser doping.

In order to eliminate laser-induced defects, low sheet resistances allow for a wider range of parameter values to be used.

A simple layout of boron diffusion illustrated by Rothhardt et al. (2013) in Figure 2.10 whereby a borosilicate glass (BSG) layer is diffused on one side of the wafer, followed by an amorphous silicon oxide (SiO_x) layer, both deposited through air pressure chemical vapor deposition (APCVD).

Figure 2.10: Simplified Presentation of Boron Diffusion Layer (Rothhardt et al., 2013)

2.3.7 Silicon Cell Processing – WET Chemical Process

In the manufacture of solar cells, the etching and cleaning processes are frequently combined into the same equipment. Inline or batch-type tools are employed depending on the treatment period, primarily determined by the etching bath. Fresh chemicals are added, and used chemicals are emptied in pre-defined intervals ("feed-and-bleed processing") to maintain consistent treatment conditions, which may be after a given wafer throughput number and/or after a specified period (idle or in production). An overflow system frequently extracts the excess treatment solution in the bath or matching tank (Buchholz et al., 2021).

In batch-type equipment, wafers are packed in carriers—usually one hundred pieces per carrier. Plastic carriers are commonly used for wet processing. Fluoridated polymers are required if oxidative chemistry is used; else, less expensive polymers can be used. Currently,

up to six carriers are assembled into batches and moved from bath to bath by a robot before being immersed in the pools. The number of carriers (wafers) each batch and the longest treatment time determine the throughput. Redundant baths are installed to boost throughput when longer treatment times are required. With four carriers (400 wafers) per batch, throughput is currently in the range of 7,000 to 8,000 wafers per hour (Buchholz et al., 2021).The different treatment bath listed in Table 2.1 while the bath schematic diagram illustrated in Figure 2.11 .

Table 2.1: Batch type treatment bath and its functionality (Buchholz et al., 2021)

Type of bath	Functionality
(a) Dipping bath	The carriers are immersed in the bath. For better mixing, nitrogen or clean, dry air (CDA) bubbling can be employed.
(b) Recirculated bath	The bath is circulated for tempering and/or gas injection (through a static or membrane mixer).
(c) Overflow rinse bath	The freshwater input is at the bottom of the rinse, and the water flow is steady throughout the process. Bubbling with nitrogen or CDA is an option.
(d) Dump rinsing bath	After the carrier has entered the bath, the water is promptly drained via a big valve at the bottom to reduce rinse time. This can be paired with a spraying unit that replenishes the bath while the carrier is still inside.
(e) Spray rinsing bath	Spray nozzles are used to introduce rinsing water.

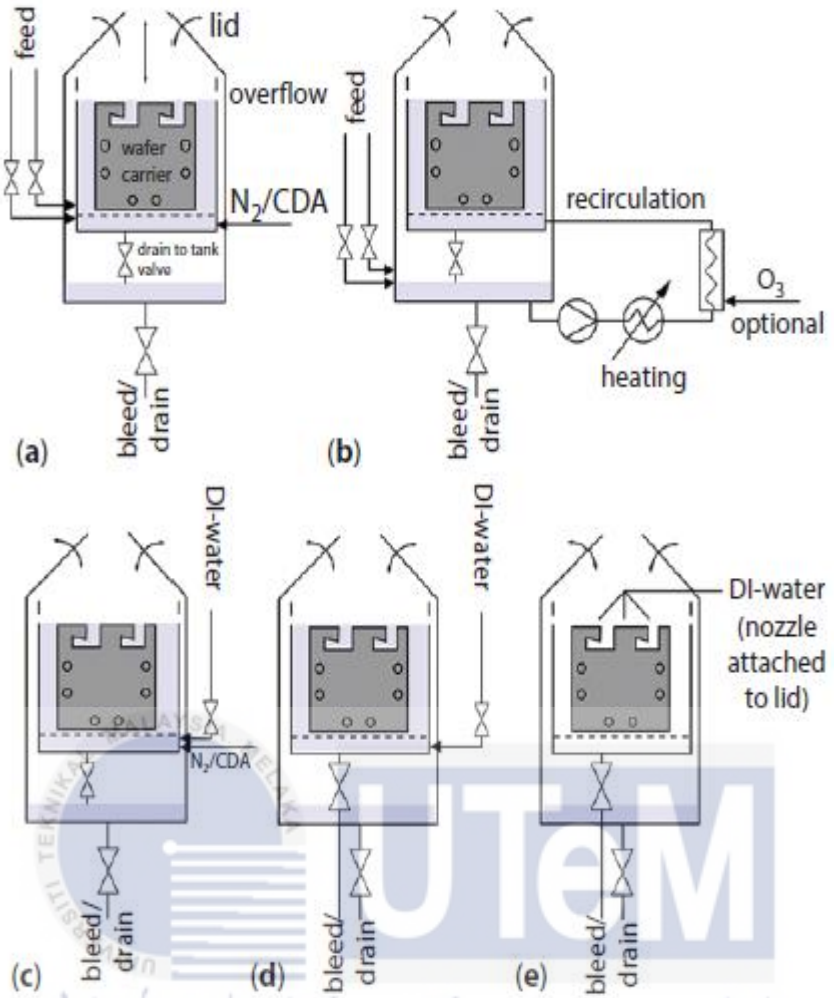


Figure 2.11: Wet Processing Bath Layout (a) Simple Dipping Bath, (b) Recirculated Bath, (c) Overflow Rinsing Bath, (d) Dump Rinsing Bath, (e) Spray Rinsing Bath (Buchholz et al., 2021)

The etching and cleaning baths (a) and (b) are the most common. Simple dipping baths are commonly applied for HF or HF/HCl dips. When the solution needs to be heated (for alkaline texturing or saw damage etching, for example), or gas (usually ozone) needs to be introduced, recirculated baths are required. There are only two feed lines drawn. More may be required depending on the bath makeup (the quantity of combined chemicals). To avoid contamination and stains on wafer surfaces, thorough rinsing with deionized (DI) water is essential to eliminate process chemical carry-over. In (c) through (e), possible bath configurations are drawn (e). The most common types are overflow rinses with an optional

bubbling function. When sticky chemicals are utilised, dump rinsing may be required to speed up processing times. The wafers are dipped into the full bath, then the water is quickly drained, and the rinse refilled. Alternatively, the dumping might be scheduled to occur after the treatment period has passed in order to restore low conductance values. Spray rinsing is a water-saving alternative. Another option for reducing water use and processing times is to cascade the rinsing baths. Electrical conductance measurement is often used to determine the quality of the rinse process. Hot water and hot air driers are used to dry wafers (Buchholz et al., 2021).

2.3.7.1 WET Chemical Process - Etching

The most critical etching stage of the silicon surfaces is to remove saw damage caused by the wire sawing process of the solar wafer as received. This is frequently used with a surface texture etch to create a "rough" surface that improves the finished device's light-trapping capabilities.

Without the organic ingredient and in a more concentrated alkaline solution, "flat" polished surfaces are obtained (Buchholz et al., 2021). The highest etch rates above 1 m/min are observed at temperatures greater than 80°C in the range of 15% to 20% wt. KOH. The etch rate is not affected by the presence of alkali metal cations (Na+, K+, or Li+) (Seidel et al., 1990).

The effects of temperature, dopant concentration, and metal contamination of etch pit density (EPD) on mc-Si are examined in study by Fleck et al. (2019). Drop in EPD following etching that is independent of the etchant used, proving that this impact is purely physical. For wafers that have been gettered only on one side, the EPD analysis yields distinct EPD values for the two sides. EPD reduction mechanisms are constrained by this fact. The studies support the notion that EPD reduction occurs because the defect etching

procedure for impurity-lean dislocations is different from dislocations adorned with impurities.

2.3.7.2 WET Chemical Process - Cleaning

Silicon etching can have two distinct effects on the cleanliness of the silicon surface. On the one hand, it eliminates previously present contamination; on the other hand, it may increase the contamination level on the surface. Three distinct types of contaminants are frequently distinguished were inorganic contamination on the molecular level, such as ions, uncharged compounds, or atoms , organic contamination (molecules, thin films, or layers) and particle contamination (silicon-based particles or dust from the surrounding) (Buchholz et al., 2021). Nguyen et al. (2019) defined that catalytic chemical vapor deposition (Cat-CVD) of silicon nitride (SiNx) and a-amorphous silicon (a-Si) layers requires chemical cleaning in order to achieve high-quality surface passivation. Hydrofluoric acid (HF) solutions were employed in the study to remove surface oxides during the cleaning process. The wettability of the solutions adjusted by varying the amount of methanol in each solution which observed an increase in the effective minority carrier lifetime (eff) from a few milliseconds to 7.8 ms, that corresponds to an extraordinarily low surface recombination velocity (SRV).

Transition metals are the most concerning inorganic contamination species. Once trapped (physisorbed or chemisorbed) at the silicon wafer's surface, they can easily permeate the silicon bulk, some even at low temperatures (Graff , 2000). They represent a threat of minority charge carrier recombination sources within the bulk or at the interface (Istratov et al., 2003). Charge carriers cannot reach the contacts due to defect-induced recombination; as a result, the device's efficiency is lowered. Inorganic contamination sources include impure chemicals, contact of the wafer with metal surfaces, and dust generated by machine

component corrosion. Organic pollutants are primarily found in sawing residues, like glues and fingerprints. Inadequate removal of these residues has been shown to cause problems with alkaline etching in particular (Moldovan et al., 2014) and other process steps (Buchholz et al., 2021).

In order to improve silicon solar cell performance, a precise control of the metal impurity density on the silicon surface is required. A silicon surface was used by John et al. (2019) to investigate the isothermal adsorption behaviour of many common metal impurities in acidic liquid (Fe, Cu, Ti, Cr and Zn). In commercially available N-type Cz-silicon, the effect of Co, Fe and Cu contaminants then identified causing carrier lifetime deterioration.

Wang et al. (2020) developed a combined cleaning process of inline HF/HNO_3 etching with batch-type etching process using the KOH/polish additives solution treatment to successfully solve optical property problems and achieve a low reversed-biased junction leakage current. The optimised cleaning method did not destroy the boron-doping layer on the front side and the poly-Si layer on the back side.

The cleanliness of a semiconductor's surface is critical to its performance and yield. Despite its simplicity, UV-ozone cleaning provides a surface passivation quality that is equivalent to high-end RCA cleaning. In addition, Bakhshi et al. (2018) provide an efficient method for obtaining cross-sectional values of the electron/hole capture for the purpose of evaluating the passivation quality of the interface. Study made by Pasanen et al. (2018) identified that front texture for high-efficiency silicon solar cells, black silicon (b-Si) is expected to gain a significant part of the industry. Cleaning b-Si surfaces is frequently an essential process step for high-efficiency cell processes, which necessitates extremely clean bulk materials. Standard clean (SC) 1 eliminates contaminants from wafer surfaces effectively, although it may be a problem for b-Solar cells. When immersed in SC1 solution

for 30 or 60 minutes, the surface reflectance approximately doubles and more than triples, respectively, due to a significant change in the nanostructure morphology.

2.3.7.3 WET Chemical Process - Rinsing

Typically, each phase of etching and cleaning is followed by rinsing with DI water to eliminate any remaining chemicals. Multiple rinses may be utilised to reduce process times and water consumption by cascading the rinsing tubs. Prior to drying the wafers at the machine's conclusion, the surfaces are turned hydrophobic by soaking them in diluted HF or HF/HCl mixes (Buchholz et al., 2021).

Similarly, elevating the wafer carriers in batch-type tools across a horizontal hot air stream produces a similar effect. While a hot water bath may be advantageous in batch-type equipment prior to air drying to pre-heat the wafers and carriers, unfavourable impacts of the hot water drier have been found in the field, particularly for very surface-sensitive processes sequences (Buchholz et al., 2021).

2.4 Summary

Solar energy has become an essential renewable energy method as it has become worldwide demand. Like other renewable energy sources, solar energy is a promising and readily available source of energy for addressing long-term difficulties in the energy crisis. Among all solar technologies, predominantly crystalline silicon, photovoltaic has led the technologies due to cost-effectiveness, ease of manufacturing, and lower maintenance. This chapter mainly focuses on improving process defects in the boron diffusion step in crystalline silicon process manufacturing. The researcher has developed numerous efforts to improve boron layer diffusion and remove the boron layer for preparation for device contact. Current studies made by researchers utilize the etching module instead of the cleaning

module in boron diffusion removal. However, none of the published literature works on applying the cleaning process in removing the boron diffusion layer. Besides that, no study was performed on double cleaning of the silicon material. Double cleaning of silicon material will increase wafer cleanliness from metal and organic contaminants, thus increasing the end of line product efficiency. This literature study aims to understand related past research to improve defects in the boron diffusion step. A clear understanding of the process and technologies in boron diffusion is essential to ensure no quality degradation on the re-claim cell after the total removal of the boron layer.

CHAPTER 3

METHODOLOGY

3.1 Introduction

This chapter will focus on getting an effective cleaning recipe for re-claim flow. The first step is to identify the top Pareto defect that contributes the most to diffusion process yield loss. The next is to identify re-claim flow to salvage the defect wafer, the step continues with identifying a cleaning recipe to re-claim the defect wafer.

The identified cleaning recipe will then be verified through reliability testing before qualification to ensure no additional impact on the product quality. The passing results from reliability testing will determine the qualified cleaning recipe. Finally, an experimental run will be conducted in a larger scale wafer to validate efficiency, cosmetic yield, and electrical performance. Data collection from the experimental run will be analyzed and compared to the standard production wafer through Statistical analysis software (JMP).

3.2 Research Flowchart

The research flowchart is simplified in Figure 3.1 and starts with identifying the highest Pareto in the Boron diffusion process. Once the type of defect is identified, the rework flow is developed to organize the correct procedure for managing the defects in the rework process. The next step is to develop a cleaning recipe to rework the identified defect wafer in the Boron diffusion step. The cleaning recipe will need to be improved, and repeat the cleaning recipe study if the oxide layer cannot be removed. For the selected cleaning recipe that can remove the layer the boron diffusion layer, the wafer will proceed with reliability testing. Two types of reliability testing, Reverse Biased Test Dielectric (RBTDE)

and Autoclave HAST chamber (ACL) Testing, will be conducted on the wafer before qualifying the selected cleaning recipe. Once passing the reliability testing, a higher volume run of 1000pieces needs to be conducted to validate the wafer performance that could represent a mass production run. Analysis of the experimental data will be using JMP Statistical software to verify the performance of Power Conversion Efficiency (EFF), Electrical Yield and Cosmetic Yield. Once the experimental data is validated as comparable to the existing product, the cleaning recipe is qualified and approved for a cleaning process step of N-type solar cell manufacturing.

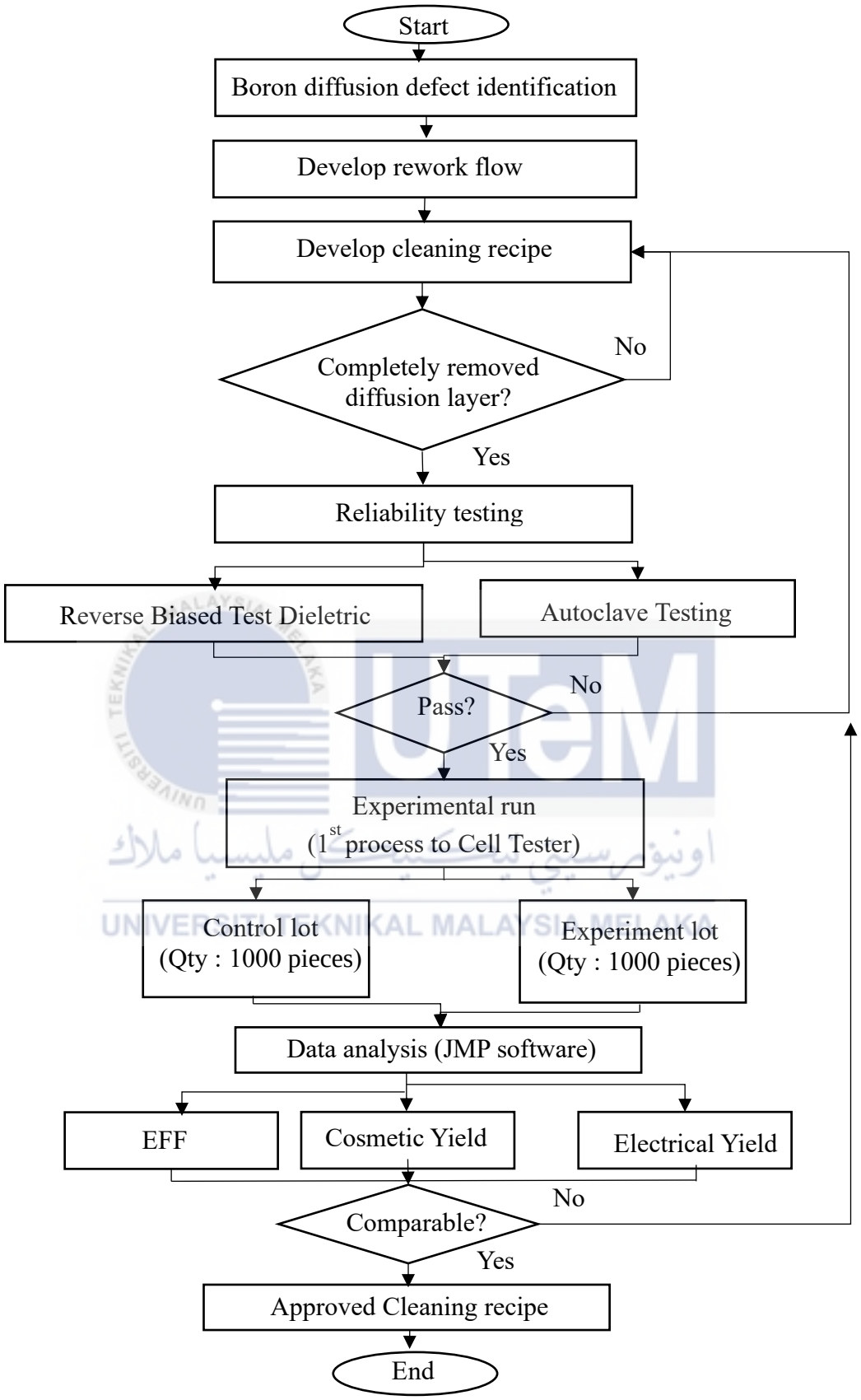


Figure 3.1: Research Flowchart

3.3 Defect Identification

Any wafer not meeting specifications will be scraped, disposed and recorded as part of process yield loss in the boron diffusion process. An example of the scrap defect will be collected at the automation reject bin, as shown in Figure 3.2. As part of cost improvement on scrap reduction, the overall defect will be monitored using the Pareto table to identify the top yield loss.

(a) (b)

Figure 3.2: (a) Reject Bin in Diffusion Process Automation and (b) Defect Wafer Accumulation in Reject Bin

3.4 Development of Re-Claim Flow

Reject wafer from diffusion process can be salvaged using cleaning module in wet chemical tools. However, the re-claim process can only be done on a good physical wafer without any chips or cracks. Figure 3.3 is the flow of re-claim which details the step from collecting the defects from the automation reject bin, and the defective wafer will be separated from the production flow to prevent it mixed with the excellent wafer. Then, the wafer will go through a cleaning process in the WET tool to remove the diffusion layer. The wafer will be scrapped post cleaning process if there is a remaining oxide layer on the wafer

surface. Meanwhile, the wafer will follow the downstream process if the oxide layer is completely removed. The wafer will continue to run until the last process, the Cell Tester, to check on its functionality and generate current. The finished good of the wafer is in Cell form and will be packed in proper packaging before being shipped to the customer. This re-claim flow was developed to organize the correct step by procedure in managing the defects, re-claim the cleaning process and finally, until the wafer can ship to the customer.

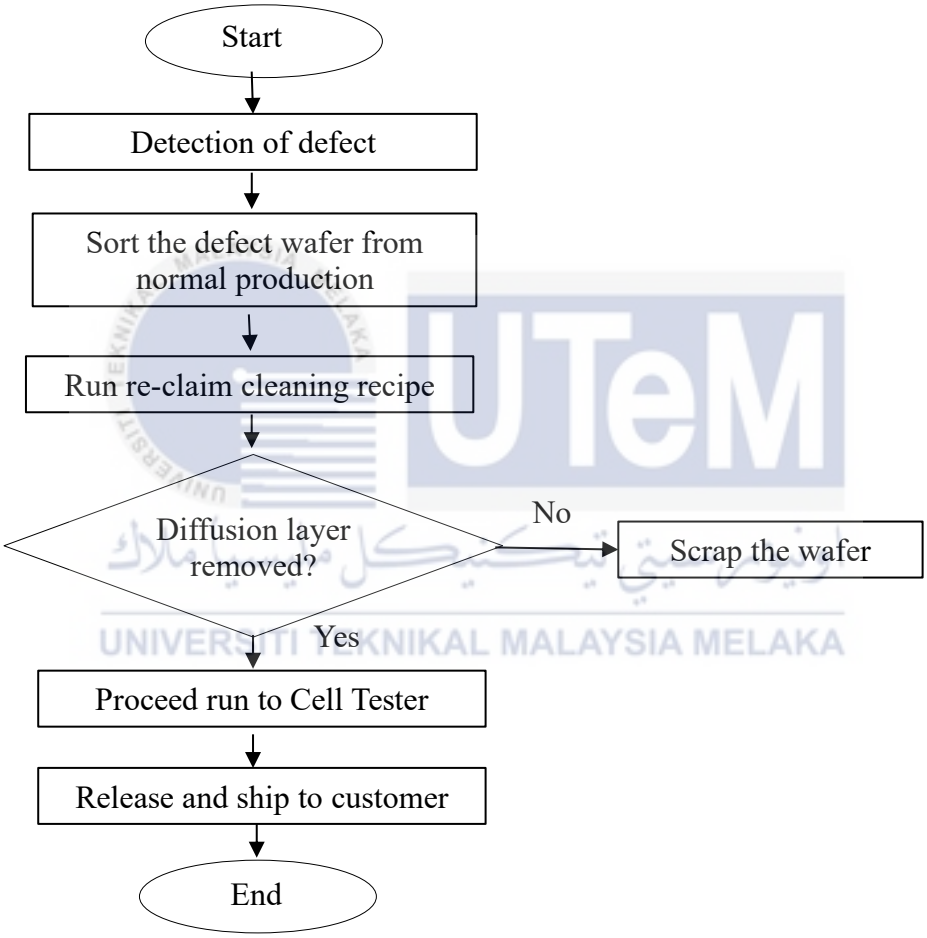


Figure 3.3: Re-Claim Recipe Testing Flow

3.5 Study of Re-Claim Cleaning Recipe

The original cleaning recipe consists of several modules: etching rinses for post chemical module, DIO_3 cleaning and HFO_3 dryer, shown in Figure 3.4. The etching module

aims to remove damaged layers on a bare silicon wafer. Once the wafer has completed etch, it will need to be rinsed to remove the remaining chemicals on the wafer surface and prevent cross contamination of chemicals to the next module. The next module will be DIO_3 cleaning, which will remove organic contaminants that adhere to the wafer surface. The wafer will need to go through another rinse module post DIO_3 cleaning with the same purposes to remove the DIO_3 chemical attached to the wafer. HFO_3 dryer module will dry the wafer and, at the same time, remove non organic contaminants on the wafer.

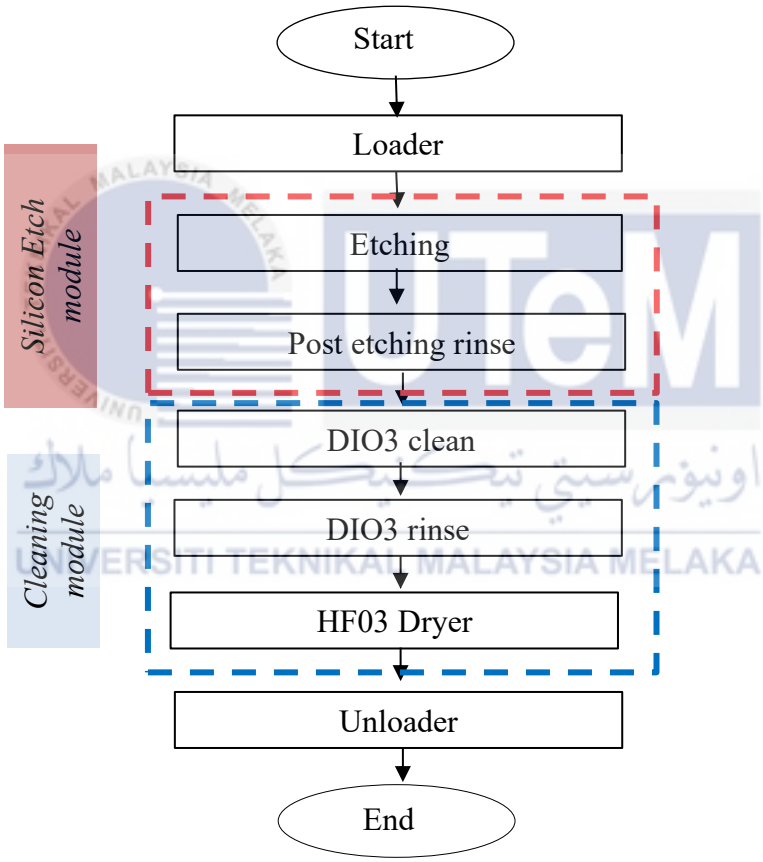


Figure 3.4: WET Chemical Process by Module

The re-claim recipe will need to be modified and adjusted from the original cleaning recipe. Besides that, the re-claim recipe must also maintain the same quality and thickness as a standard good production wafer.

This section will collect and separate the defective wafer from the good production wafer. Accumulation of defect wafer will be stacked inside cassette of 50 pieces slot and loaded into wet chemical tools for diffusion layer removal. Before testing the re-claim recipe, the wet chemical tools setting will be adjusted according to the specific range defined in the HF03 module. A total of 6 sets of defect wafers will be loaded following the specific HF03 parameter range in Table 1.1 set of wafers consisting of 100 pieces will be used in two cassettes for re-claim recipe testing and validation. Figure 3.5 describes the wafer stack into 50 pieces cassette slot and loaded arrangement into the wet chemical tool.

Table 3.1 : HFO_3 Parameter Table

Parameter	Range	Target	Recipe 1	Recipe 2	Recipe 3
HF chemical dosing (ml)	100-250	200	150	200	250
HFO_3 bath temperature (^{o}C)	60-70	65	60	65	70

Once the wafer is unloaded from the wet chemical tool, a visual inspection setup during post-cleaning process to verify whether the diffusion layer is completely removed, the effectiveness of diffusion layer removal will define the selected $HF0_3$ parameter to be used as a re-claim recipe.

(a) (b)

Figure 3.5: (a) Image of Loading Full Wafer Cassette into Machine (b) Wafer Slotted in Cassette

The wafer that can remove the diffusion layer completely will proceed to run until the final process, Cell Tester. In Cell Tester, the wafer will be sorted according to yielding and non-yielding bin. The yielding bin categorizes as passing with good electrical yield and will be shipped to the customer, while non-yielding is a wafer with low electrical yield and will be rejected into the reject bin. The purpose of loading the wafer into the Cell Tester is for Pre Test data collection, which will be a prerequisite in reliability testing.

3.5.1 HFO_3 Parameter Adjustment Through Extreme Value Theorem (EVT) Method

This project will focus on HFO_3 parameter adjustment to create the cleaning recipe. The selection of the parameter range in Table 3.1 uses Extreme Value Theorem (EVT), which focuses on the maximum and minimum values between the range. The extreme value theorem states that a continuous function can have extrema if defined on an interval that is both closed and bounded. A function f(x) has a maximum and a minimum value on [a, b] if it is continuous on the closed interval [a, b] (Strang,1991).

Strang (1991) justified that the maximum or lowest may occur at a specific location inside the interval described by f() and df/d based on the concept of a "local maximum" or a

"local minimum". If f'()=0, then "local" provides for the potential that f() may go higher or lower in other intervals. Begin by taking f(+) – f(). If f() is the maximum, this difference is either negative or zero.The step Δx might be forward or backward and defined as below :

If $\Delta x > 0$:

$$\frac{f(x+\Delta x)-f(x)}{\Delta x} = \frac{negative}{positive} \leq 0 \; and \; in \; the \; limit \; \frac{df}{dx} \leq 0 \qquad (3.1)$$

If $\Delta x < 0$:

$$\frac{f(x+\Delta x)-f(x)}{\Delta x} = \frac{negative}{positive} \geq 0 \; and \; in \; the \; limit \; \frac{df}{dx} \geq 0 \qquad (3.2)$$

Khalil (2017) defined that the extreme value theorem (EVT) is a widely used statistical method for analyzing stochastic series of identically distributed random variables (iid RVs). EVT studies the behaviour of EVs even though these values have a very low probability of occurrence but can have a significant impact on the studied system. Skou et al. (2017) explained in their study that extreme values in the process parameters would occasionally occur during production and thus impact the final product's composition. A better description and understanding of these events, even if no direct consumer concerns are presented, can be a beneficial tool for management or control and optimization purposes. Although extreme events infrequently occur in nature, the repercussions can be substantial, and with the ever-increasing size of business operations, the ability to characterize extremes is economically vital. Key-processing parameters with extreme values are often considered outliers or statistically insignificant in process monitoring.

3.5.2 Qualification Test of Re-Claim Cleaning Recipe

There will be three qualification test in this stage to determine passing criteria for the cleaning recipe. First passing criteria is visual inspection by operator , secondly is sampling inspection of the silicon layer under microscope for the completely removed diffusion layer. Third qualification test will be boron and oxide layer thickness removal measurement.

3.5.2.1 Visual Inspection

Once the wafer unloads from the cleaning module, the wafer will be 100% inspected visually by the Operator by following the criteria in Figure 3.6. Complete oxide removal will have no diffusion layer on the wafer, while incomplete oxide removal will have a bluish colour, which shows the oxide layer remains on the wafer surface. Any abnormal wafer that cannot remove the diffusion layer will be scrapped.

(a) (b)

Figure 3.6: (a) Complete Oxide Removal and (b) Incomplete Oxide Removal

3.5.2.2 Microscopic Image

Ten pieces of the wafer will be sampled for microscopic image, and 5 points per wafer will be inspected under a microscope. Wafer will be scribed with Upper left, Upper

right, Center, Lower Left and Lower right, as shown in Figure 3.7. This step aims to determine the capability of diffusion layer removal at each different site of the wafer surface.

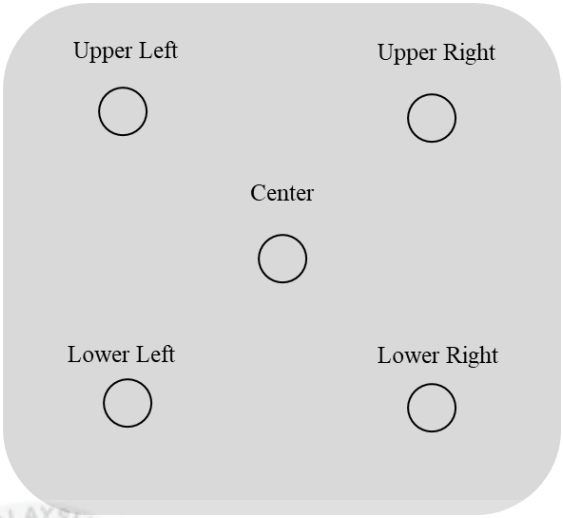


Figure 3.7: Sampling Point Inspection

3.5.2.3 Boron and Oxide Removal Thickness Measurement

Sampling 5 pieces of wafer measurement of the boron and oxide removal thickness will be conducted during the experimental run using Woollam Ellipsometer shown in Figure 3.8. Oxide Thickness will be measured prior to post loading to the WET Chemical process, and delta thickness will be measured accordingly. The measurement point will be following Figure 3.6.

Figure 3.8: Woolam Ellipsometer

3.6 Qualification of Re-Claim Cleaning Recipe using Reliability Testing

The defined re-claim recipe must be qualified before it is approved for production usage. A small run quantity of 100 pieces of the wafer using the defined re-claim cleaning recipe will undergo several tests to ensure the re-claimed wafer can comply with reliable performance and specification. Two necessary tests will be conducted, which are Autoclave HAST chamber (ACL) and Reverse Biased-Dielectric breakdown (RBTDE) testing.

3.6.1 Reliability Testing : Autoclave HAST Chamber (ACL)

The highly accelerated temperature and humidity stress test (HAST) is an accelerated method of testing electronic component reliability that uses temperature and humidity as environmental variables. The pressure cooker test (PCT) or unsaturated pressure cooker test (USPCT) is another name. It aims to find the effectiveness of a test sample's humidity resistance by increasing the water vapour pressure in a test chamber to an extremely high level above the partial water vapour pressure inside the test sample. The infiltration of moisture into the sample is speeded up by using this procedure (ESPEC, 2021).

This testing will be conducted using High Accelerated Stress Test System (HAST Chamber), as shown in Figure 3.9. This chamber operated with a temperature range of

105.0℃ to 142.9℃, humidity range of 75 to 100%rh, and pressure range of 0.020MPa to 0.196MPa (ESPEC, 2021).

Figure 3.9: Autoclave (HAST) Chamber (ESPEC, 2021)

Figure 3.10 illustrates the I-V and P-V curves used to evaluate the performance characteristics of PV modules, where "I" stands for current, "V" for voltage, and "P" for power. Tracing the I-V or P-V curve is the basic principle for evaluating PV efficiency that determines the maximum power point, fill factor, open-circuit voltage, and short circuit current (Mathew et al., 2018).

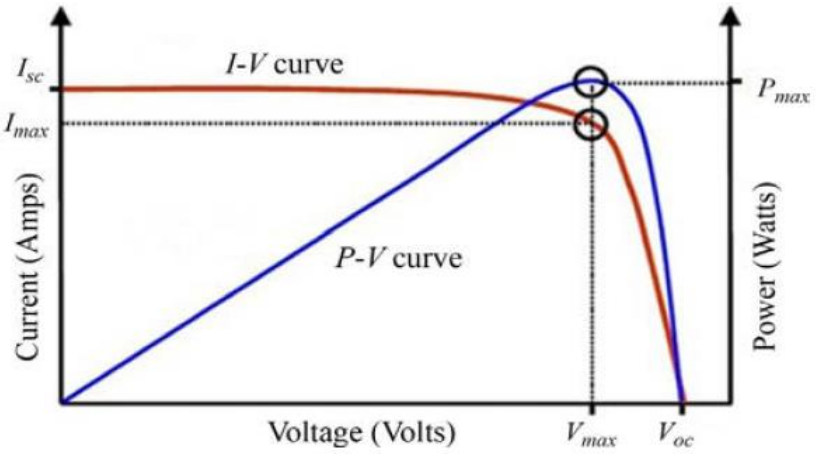


Figure 3.10: *I-V* and *P-V* Curves (ESPEC, 2021)

Maximum current, or Isc, is produced by a solar PV cell when it is operated under standard test settings (STC), similar to actual operating circumstances. Under STC or actual operating circumstances, Open Voltage Circuit (Voc) is the voltage recorded with open PV cell terminals. In most cases, the voltage reading taken under these circumstances will be greater than the highest voltage reached. Power Conversion Efficiency (EFF) is the ratio of power output to the power input. It is a stand-in for the overall efficiency of PV cells. The quality of the PV cell is measured by Fill Factor (FF). Power Input is the product of the area of the PV module, and the incident solar radiation gives the quantity of solar energy that can be produced. At the same time, Power Output is the sum of the highest possible current and voltage values. A more common word for the final power output. Quality of the PV cell measured from Fill Factor (FF) value. To simplify, it is expressed as the power output divided by the open-circuit voltage and current (Mathew et al., 2018). Generated formula of the electrical parameter and its relationship expressed as below :

Power Input (P_{in}) :

$$P_{in} = Area\ x\ I \tag{3.3}$$

Power Output (P_{out}) :

$$P_{out} = V_{max}\ x\ I_{max} \tag{3.4}$$

Power Conversion Efficiency (EFF):

$$EFF = \left[\frac{P_{out}}{Area\ x\ I}\right] x\ 100 \tag{3.5}$$

Fill factor (FF) :

$$FF = \frac{P_{out}}{(V_{oc} x I_{sc})} \tag{3.6}$$

Reliability testing flow for ACL is shown in Figure 3.11, starting with cell sampling. In this stage, the wafer will be collected from the yielding bin and continued with visual inspection to ensure no additional defects are observed on the wafer. Next, the wafer will undergo Pre Test using Cell Tester to collect data for Voc, Isc, FF, Maximum Power (Pmax) and Power Conversion Efficiency. Once pre- Test data is completed, the reliability sample will be loaded into Chamber for 168hours. Similar data collection for Post Test will be conducted, and the degradation result will be calculated based on the delta value of Pre Test and Post Test, which consist of Open Circuit Voltage (Voc), Short circuit current (Isc), FF(Fill factor) and Power conversion Efficiency (EFF).

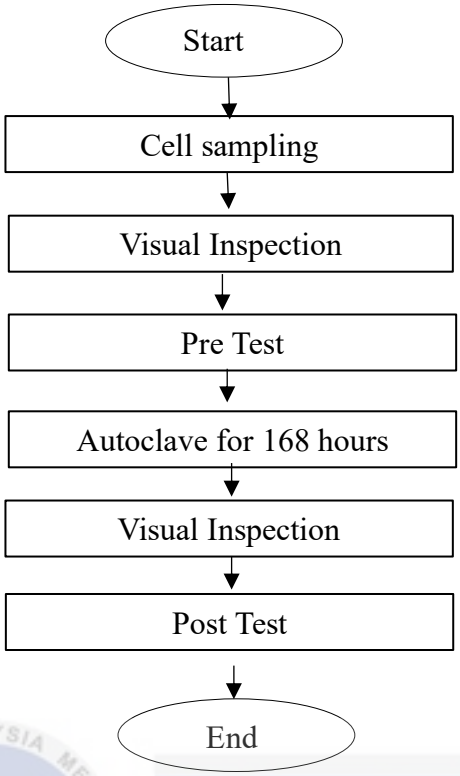


Figure 3.11: ACL Test Sample Submission Flow

For a passing ACL test, the result must be within the maximum admissible degradation limit of -5%. Besides, the experiment split result must be statistically comparable to the control splits on dPmax with 95% confidence.

3.6.2 Reliability Testing : Reverse Biased Testing Dielectric (RBTDE)

The reversed biased testing purpose or thermal cycling test is to verify the PN junction under reverse biased conditions after running using the re-claim cleaning recipe. This testing will be conducted using Thermal Chamber (ZPS-44-10-SCT\WCT as per image in Figure 3.12) and operated using 100.0°C temperature for 120hour.

Figure 3.12: Reverse Biased Test Chamber (cszindustrial, 2021)

For this testing, under a condition when a PN junction is reversed biased, only a little amount of current can pass through it. This current is caused by the movement of minority charge carriers and is nearly voltage independent. The current across the PN junction increases abruptly if the reverse bias is set too high, and the voltage at which this occurs is known as the breakdown voltage. The crystal structure will, at the same time, breaks down at this breakdown voltage. When an excess reverse bias is removed, this crystal structure recovers to its original condition, assuming the crystal has not been permanently destroyed by overheating (cszindustrial, 2021).

RBTDE testing, or PV Thermal Cycling Test, is a type of environmental testing that uses cyclical, high-and-low temperature exposure to replicate thermal stress on the solar panel (Cheacharoen et al., 2018). The cell is subjected to thermal cycling, repeatedly subjecting it to a range of temperatures between two predetermined extremes. The thermal fatigue test is an environmental stress test designed to assess a product's or component's durability and detect manufacturing flaws at an early stage. It is a standard qualification test for PV modules (Zhang et al., 2019).

The thermal cycling test, also known as the temperature cycle test, subjects a specimen to repeated thermal and thermal-mechanical stress. Mismatches in the coefficient of thermal expansion (CTE) of materials are one common cause of failure, and thermal cycle studies can help pinpoint the specific processes at play. The capacity of a device (or its components) to withstand very high and very low temperatures is measured through thermal cycling testing. The specimen's ability to tolerate repeated exposure to high temperatures is also evaluated (Zulkifli et al., 2011).

For this reliability testing, the sample has to undergo nine steps before releasing the report to the end user shown in Figure 3.13. The first step will be cell sampling, which is collected from the selected yielding bin before proceeding as a sample for this testing. Once the completed visual inspection, the wafer will need to undergo Pre Test for data collection to check and ensure no other non related to the study is included as sampling data. The wafer then will be assembled into a coupon as shown in Figure 3.14 and laminated before loading into the chamber. Pre EL, Pre Flash and Pre IR, as per Figures 3.15 and 3.16, will be conducted after initial loading into the chamber. Once unloaded from the chamber, Post EL and Post IR data will be conducted and compared with Prior EL and Prior IR.

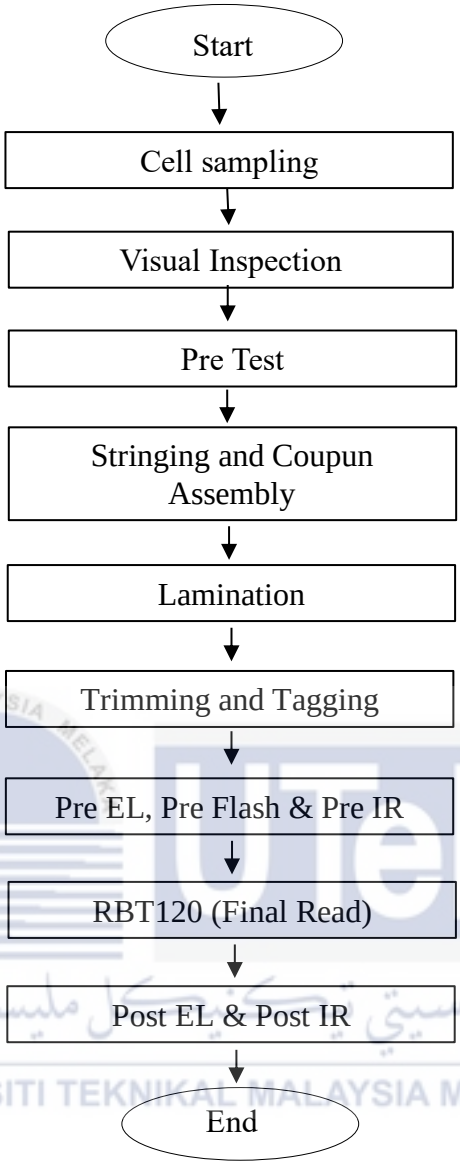


Figure 3.13: RBTDE Sample Submission Flow

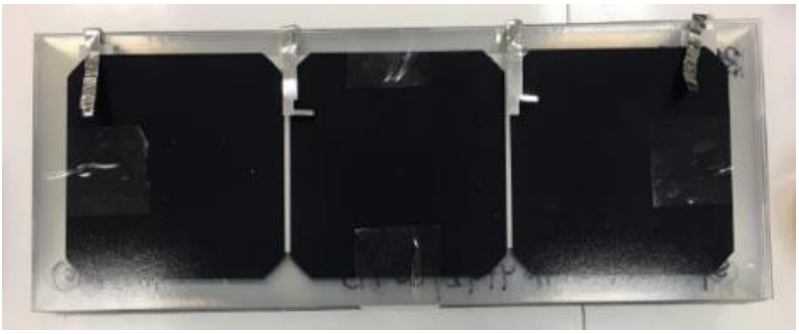


Figure 3.14: Reverse Biased Coupon

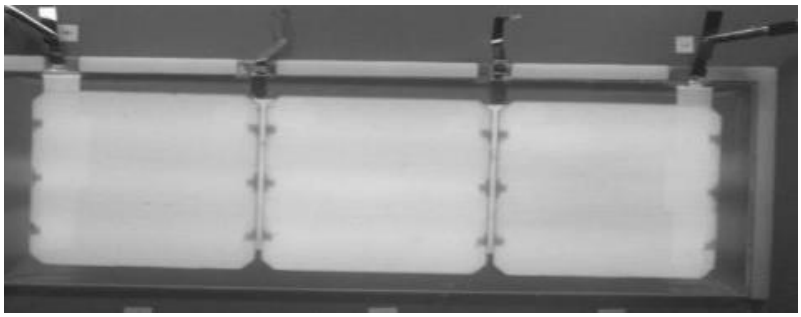


Figure 3.15: Sampling Image of Coupon EL

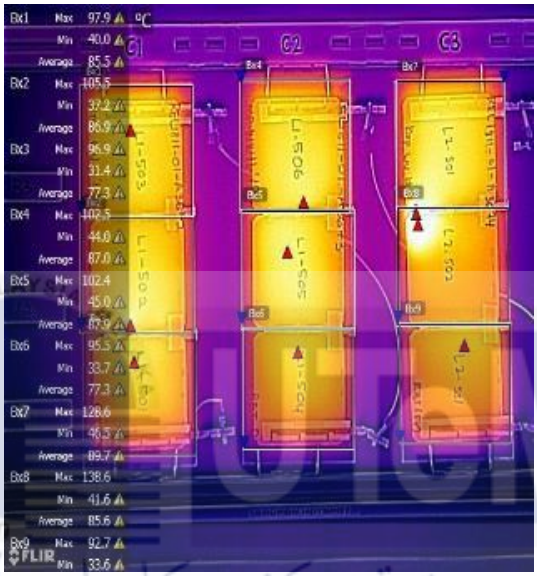


Figure 3.16: Sampling Image of Coupon IR

For a passing RBTDE test, the result must be within Level 2 Hotspot (< 160 C) at 0 and 120 hours. Hotspot level criteria can be seen in Table 3.2. Besides, the experiment split result must be statistically comparable to maximum temperature before it is approved as a passing result.

Table 3.2: Hotspot Level Criteria

Hotspot Level	Max Temp, C	Disposition
Level 1	< 120	Pass
Level 2	120 < x < 160	Pass
Level 3	160 < x < 260	Fail
Level 4	>260	Fail

3.7 Validation of Re-Claim Cleaning Recipe

The experimental flow of the selected cleaning recipe is shown in Figure 3.17, where this flow starts with turning ON the selected cleaning recipe for re-claim. After that, the defective wafer will be loaded into the WET cleaning tool. Wafer will be scrapped if there is incomplete oxide layer removal, while the good wafer that is completely removed will proceed to Final Visual Inspection (FVI) and Cell Tester. Data from the Cell Tester will be analyzed using JMP Statistical software to validate the performance of the experimental data.

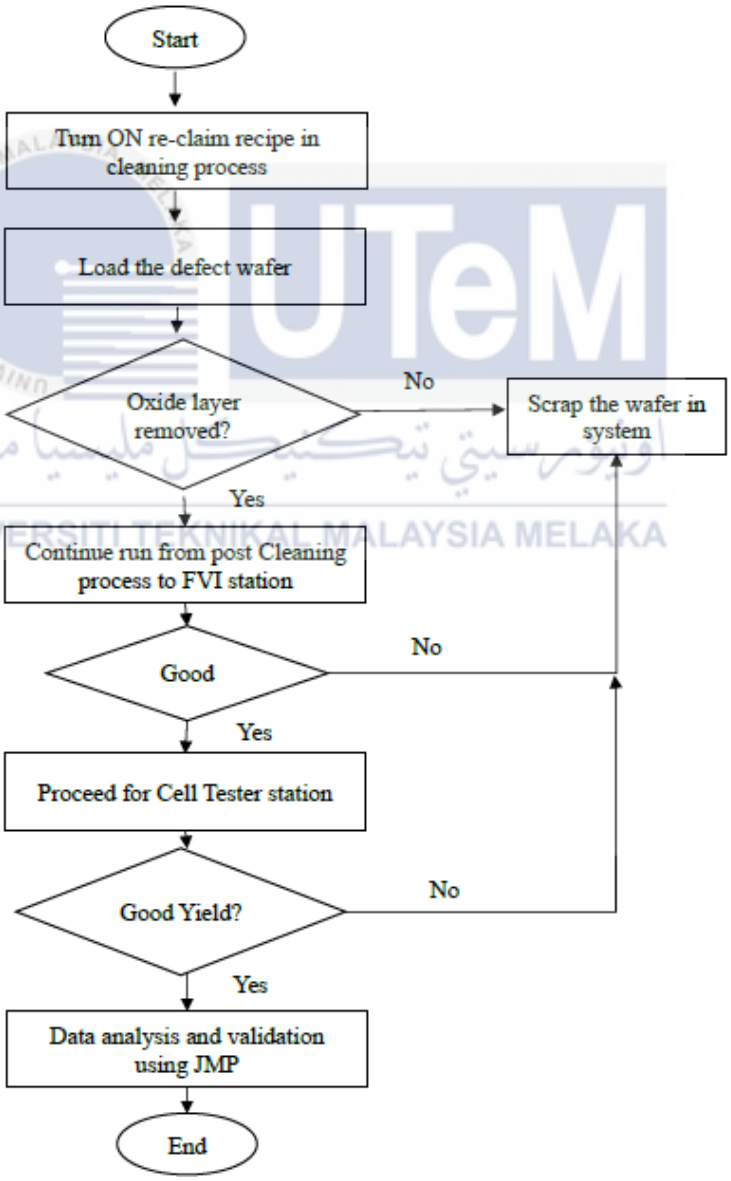


Figure 3.17: Experimental Run Flow using Re-Claim Recipe

3.7.1 Experimental Run

Two types of experimental runs will be conducted throughout this study. The first run is on a smaller scale quantity of 100 pieces for reliability testing sample submission, while the second run is on a higher volume run of 1000 pieces to test the re-claim cleaning recipe after passing the reliability testing. The sampling quantity for this experiment is shown in Table 3.3.

Table 3.3: Table of slit run

Stage	Lot Quantity (pieces)	
	Experimental run	Control run
Run 1	100	100
Run 2	1000	1000

The material in this experimental run is divided into an experimental lot and a control lot. The experimental lot is collected from a scrap wafer in a diffusion process that has undergone a re-claim cleaning process, while the control lot is from a good production wafer.

The wafer will load at the cleaning process using the selected re-claim recipe in the experimental run. Once the wafer is unloaded from the cleaning process, a visual inspection will ensure the diffusion layer is fully removed and clean without defects. The defect wafer will be rejected if the layer is not entirely removed. The wafer will continue loading from post Cleaning until Final Visual Inspection (FVI) and the final process step, the Cell Tester.

3.7.2 Data Collection for Power Conversion Efficiency, Electrical Parameter and Cosmetic Yield

At the Final Visual Inspection station, the wafer will be evaluated according to cosmetic condition and sorted according to 4 categories from highest to lowest grade, which is grade A, B, C and D. Good Cosmetic Yield is considered from a combined yield of grade

A & B. Wafer that is under grade A, B and C will continue to the following process which is Cell Testing while grade D will be scrap. Cosmetic Yield is a calculation expressed in formula 3.8 which the total quantity of Bin A and B is divided over the total quantity of all cosmetic Bin A, B, C and D. Examples of various wafer surface conditions are shown in Figure 3.18, where we can see the different colour of the wafer surface for lighter blue to darker blue that defines lowest to the highest grade of wafer surface cosmetic criteria.

Figure 3.18: Cosmetic Yield Categorized by Different Surface Color and Condition of Wafer

At the Cell Testing station, the wafer will be inspected under the Cell Testing machine. Automation (robot) will load the wafer onto a "flash table" and connects the positive and negative leads to measuring equipment as it exits the production line. After then, the panel is "flashed" with calibrated sunlight recipe that is similar to actual sunlight characteristics. 2 types of data will be collected from Cell Testing, which is Power Conversion Efficiency (EFF) yield measured from the power generated from each wafer while Electrical yield measured and sorted according to yielding (good bin) and non yielding (reject bin). This study's mean value of Power Conversion Efficiency cut-off is set at 21.8%.

Cells that do not meet 21.8% Power conversion Efficiency (EFF) will be categorized and rejected into non-yielding bin in the Cell Testing process. Calculating electrical yield is based on the quantity of yielding cells over the total cell produced, which is a combination of yielding and non yielding quantity.

$$\text{Electrical Yield} = \left[\frac{Yielding\ quantity}{Yielding\ quantity\ +\ Non-yielding\ quantity}\right] x\ 100 \quad (3.7)$$

$$Cosmetic\ \text{Yield} = \left[\frac{Bin\ A\ +\ Bin\ A}{Bin\ A\ +Bin\ B\ +Bin\ C\ +\ Bin\ D}\right] x\ 100 \quad (3.8)$$

All data collected from Cosmetic Yield, Power Conversion Efficiency yield, and Electrical Yield will be analyze using statistical analysis, JMP statistical software.

3.8 Data Anaylisis and Validation Using JMP Statistical Software

This study will be using JMP statistical software and the process flow depicted in Figure 3.19. The goal will focus on two groups, control and experiment, to estimate using the group means and check if they differ significantly.

The first step is to compile the experimental and control data to be uploaded into the JMP. The following step is to plot the group means in a graph and analyze them. This section includes analyzes that estimate group means and tests to see if they differ. The group means are the centre lines of the mean diamonds. The top and bottom of the diamonds represent the means 95 % confidence intervals. The probability that this confidence interval contains the true group mean is 0.95 (Sall et al., 2017).

Confidence intervals show whether a mean is significantly different from some hypothesized values. This study will be based on a 95% confidence interval in which the probability value (p-value) has to be more than 0.05 to determine that the experimental is insignificant difference from control or standard data (Sall et al., 2017).

In this study, a comparison analysis between experimental and control data will be conducted using the t-Test, Wilcoxon Test and Mosaic Plot. The t-test was introduced to determine whether a mean differed significantly from a hypothesized value. The situation now is to see if the difference between the two means is significantly different from the hypothesized value of zero. The t-ratio is calculated by first calculating the difference between the estimate and the hypothesized value and then dividing that amount by the standard error. (Sall et al., 2017).

Wilcoxon test in this study uses the nonparametric method that only uses the rank order of the data and disregards the spacing information between the data points. Nonparametric tests do not presume that the data follow a normal distribution. This can prevent the test from being invalidated by data that contains outliers and protects it from distributions with very non normal distribution shapes (Sall et al., 2017).

A mosaic plot is also used in this study where it is a group of split bar graphs arranged next to one another, which may be used to examine how different sample's response probabilities are divided up. First, the horizontal axis is segmented in accordance with the sample proportions. The predicted response probabilities are then used to further subdivide each of these cells vertically. Each rectangle's area is the corresponding cell's frequency count (Sall et al., 2017). A detailed description of data is then shown as a cross tabulation or cross tab (also known as a two-way contingency table). The probability and numbers in the predicted cells of the table are derived by multiplying the marginal probabilities and counts.

The chi-square test is employed for the contingency table, which is equivalent to the test for independence of multiple categorical responses.

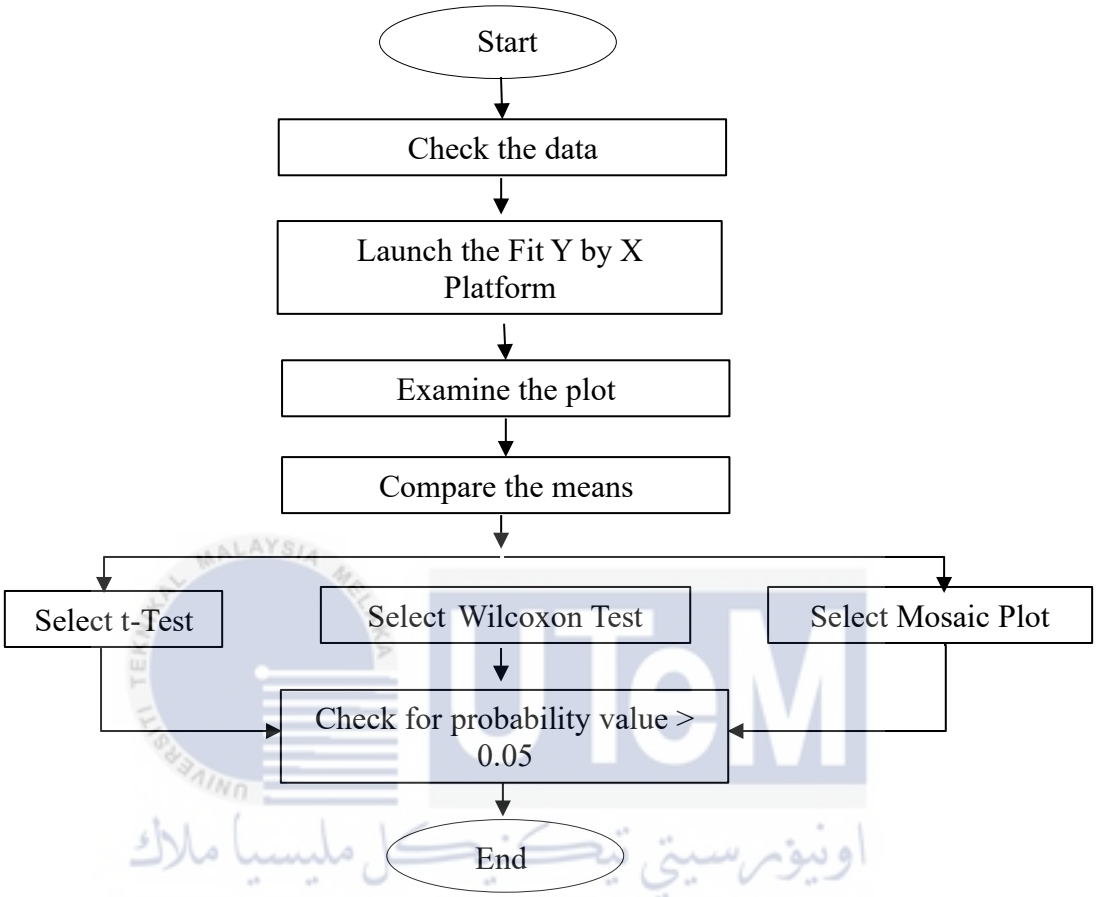


Figure 3.19: JMP Step Flow

This study will conduct comparison data for experimental and control lot to check the impact of Power Conversion Efficiency, Electrical and Cosmetic yield through JMP statistical software. The plotted t-Test, Wilcoxon test and Mosaic plot will help to define whether the result of an experimental run of using the re-claim cleaning recipe is comparable to or better performance with the control lot, which is, in this case, the existing product in the production line.

CHAPTER 4

RESULT AND DISCUSSION

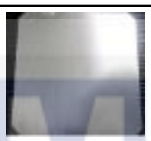
Chapter 4 presents the analysis and result of the qualifying cleaning process in removing the diffusion layer for the rework process. The cleaning process flow will help salvage the defect wafer from being scrap, thus improving yield loss and operational cost. By using Extreme Value Theory (EVT) concept, three recipe stage from the range of minimum , median and maximum value of $HF0_3$ chemical dosing and bath temperature tested for selection of the best cleaning recipe. Based on data collection and inspection of the experimental sample compared with the control of the research, this result will be used to justify the implementation of a clean pre process in the actual production of N-type photovoltaic solar cells. The cleaning recipe qualified through passing results of reliability testing before going for a higher volume run of the experimental wafer. Validation of higher volume results will confirm that the actual performance of the wafer is similar to control good production wafer after being cleaned using a cleaning recipe.

4.1 Result of Visual inspection of Wafer After Cleaning

During the pre- clean recipe evaluation, a visual inspection is performed after each experimental recipe defined for the HFO_3 module. In this activity, five pieces of the wafer in each recipe were tested and 100% verified using visual inspection. In any case of the wafer with an abnormal condition such as stain due to incomplete removal of the diffusion layer, the recipe will be considered as fail and need to be rejected. Based on the visual inspection image in Table 4.1, all three recipes defined were able to remove the diffusion layer for all five pieces of wafer run in each experimental recipe. This is in the same justification defined

by Osterkamp et al. (2003) that HFO_3 cleaning is an effective method for extracting certain metallic species without allowing the plates to return to the solution. Hydrophobic, H-passivated surfaces, such as those produced by HFO_3 last processing, are preferable because they improve film adhesion and reduce electrical contact resistance. In addition, the hydrophobic surface makes drying the wafers efficiently. As soon as the wafers are removed from the HFO_3 module, they are completely dry with no stains or watermarks (Osterkamp et al., 2003).

Table 4.1: Visual Inspection Result

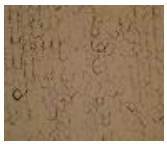
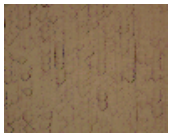
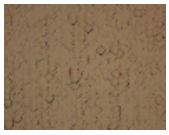
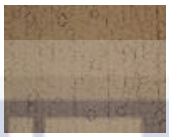
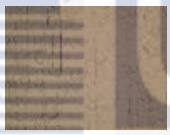
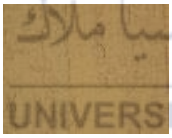
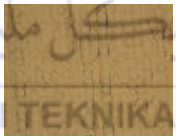
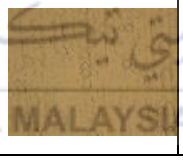
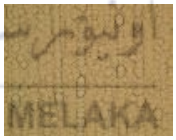
Recipe	Wafer 1	Wafer 2	Wafer 3	Wafer 4	Wafer 5
Recipe 1 : 150ml + 60°C					
	Result : PASS	Result : PASS	Result : PASS	Result : PASS	Result : PASS
Recipe 2 : 200ml + 65°C					
	Result : PASS	Result : PASS	Result : PASS	Result : PASS	Result : PASS
Recipe 3 : 250ml + 70°C					
	Result : PASS	Result : PASS	Result : PASS	Result : PASS	Result : PASS

4.2 Result of Optical Microscopic Inspection on Wafer Surface

Other criteria to be considered to evaluate the defined experimental recipe is by inspecting the cleaned wafer using optical microscopic. One wafer is selected in each recipe and inspected at 5 points on the wafer (Upper Right, Upper Left, Centre, Lower Right, Lower Left). Based on the microscopic inspection shown in Table 4.2, all three recipes observed cleaned wafers without a leftover diffusion layer. The microscopic images were

also compared with the non conformance wafer, and none of the wafers showed similar wafer conditions with non conformance.

Table 4.2: Microscopic Inspection Result

Recipe	Upper Right (UR)	Upper Left (UL)	Centre (C)	Lower Right (LR)	Lower Left (LL)
Recipe 1 : 150ml + 60°C					
Recipe 2 : 200ml + 65°C					
Recipe 3 : 250ml + 70°C					
Control					
Example of Non Conformance Wafer					

4.3 Result of Oxide Thickness Measurement

The third criteria for selecting the best pre clean recipe are measuring the oxide thickness wafer after diffusion. Once the wafer is unloaded from the cleaning bath, it will be directly loaded into the diffusion machine for the diffusion process. A total of 3 wafers from each control and experimental recipe were measured at 5 points (Upper Right, Upper Left, Centre, Lower Right, Lower Left), and oxide thickness measurement was conducted once the wafer completed diffusion processing. The recipe will be rejected if there is out of specification thickness data from the upper limit. The out of specification at the upper limit

defined that there is a remaining diffusion layer from pre clean activity. The oxide thickness measurement data shown in Table 4.3 observed that the oxide thickness is within the specification limit. The value of the oxide thickness was then tabulated in JMP statistical software for comparison of the experimental and control measurement data.

Table 4.3: Oxide Thickness Measurement Result

Split Run	Wafer Number	Wafer site	Diffusion Thickness		
			150ml + 60°C	200ml + 65°C	250ml + 70°C
Control	Wafer 1	Upper Right	381.52	381.52	381.52
Control		Upper Left	398.38	398.38	398.38
Control		Center	407.77	407.77	407.77
Control		Lower Right	395.25	395.25	395.25
Control		Lower Left	393.65	393.65	393.65
Control	Wafer 2	Upper Right	399.41	399.41	399.41
Control		Upper Left	392.43	392.43	392.43
Control		Center	390.01	390.01	390.01
Control		Lower Right	392.24	392.24	392.24
Control		Lower Left	411.21	411.21	411.21
Control	Wafer 3	Upper Right	388.74	388.74	388.74
Control		Upper Left	395.95	395.95	395.95
Control		Center	399.21	399.21	399.21
Control		Lower Right	395.50	395.50	395.50
Control		Lower Left	393.30	393.30	393.30
Experiment	Wafer 1	Upper Right	398.99	410.55	387.52
Experiment		Upper Left	381.01	385.96	388.38
Experiment		Center	401.18	399.92	407.77
Experiment		Lower Right	415.72	405.35	385.25
Experiment		Lower Left	398.66	399.43	393.65
Experiment	Wafer 2	Upper Right	386.72	409.20	399.41
Experiment		Upper Left	382.30	393.36	392.43
Experiment		Center	405.69	386.49	390.01
Experiment		Lower Right	406.06	391.66	392.24
Experiment		Lower Left	415.44	402.26	411.21
Experiment	Wafer 3	Upper Right	405.76	401.73	398.74
Experiment		Upper Left	415.72	386.38	395.95
Experiment		Center	387.73	406.72	399.21
Experiment		Lower Right	412.33	381.01	395.50
Experiment		Lower Left	406.47	396.55	403.30

Three experimental recipe measurement data were plotted in JMP and further analyzed using T-test to illustrate the magnitude of difference between the experimental and control group of data. The likelihood of difference is then evaluated by probability value or p-value. The probability value or p-value is then used to determine the likelihood of a difference. The p-value in this study will define a severe or even more significant difference between experimental and control data. If the p-value is 0.05%, it means 5% of the experimental data is comparable to the control data. Comparison p-value of three different pre clean recipes compiled in Table 4.4. Based on the plotted T-test p-value, Figure 4.3 showed that Recipe 3 (250ml HFO_3 dosing and 70^oC HFO_3 temperature) is the highest rank at 0.4411, which defined the closest value to the control data, followed by Recipe 2 (200ml HFO_3 dosing and 70^oC HFO_3 temperature) p-value at 0.3166 plotted in Figure 4.2 and lowest p-value at 0.0648 showed in Figure 4.1 from Recipe 1 with lowest HFO_3 dosing at 150ml and 60^oC HFO_3 temperature). In this study, Recipe 3 is selected as pre clean recipe due to the closest p-value to the control data. Among three recipe conducted in the experiment, Recipe 3 using highest voume of HFO_3 chemical dosing and highest $HF0_3$ bath temperature. Besides that , the higher volume of HFO_3 chemical dosing and higher HFO_3 bath temperature will have more aggresive cleaning which explained on why Recipe 3 resulted closest p-value to the production control wafer performance. Reliability testing sample preparation will be using Recipe 3 as pre clean recipe for further confirmation on the wafer reliability performance to meet the product quality after undergo oxide layer removal.

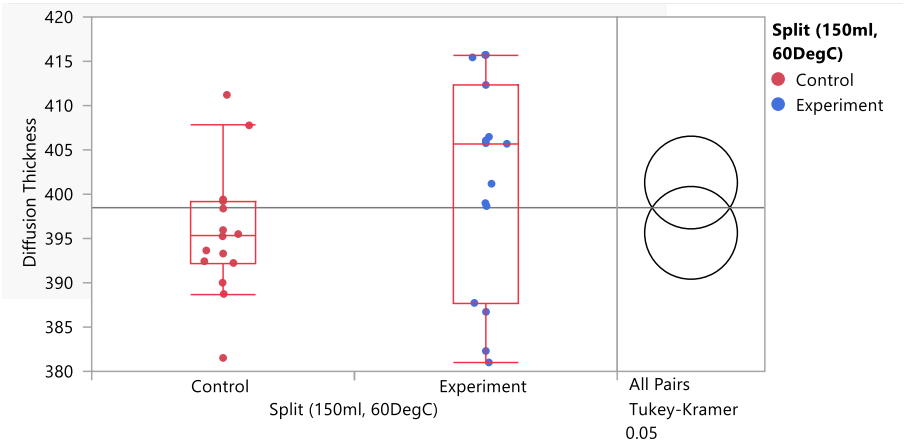


Figure 4.1: Oxide Thickness Comparison for Recipe 1 (150ml, 60°c)

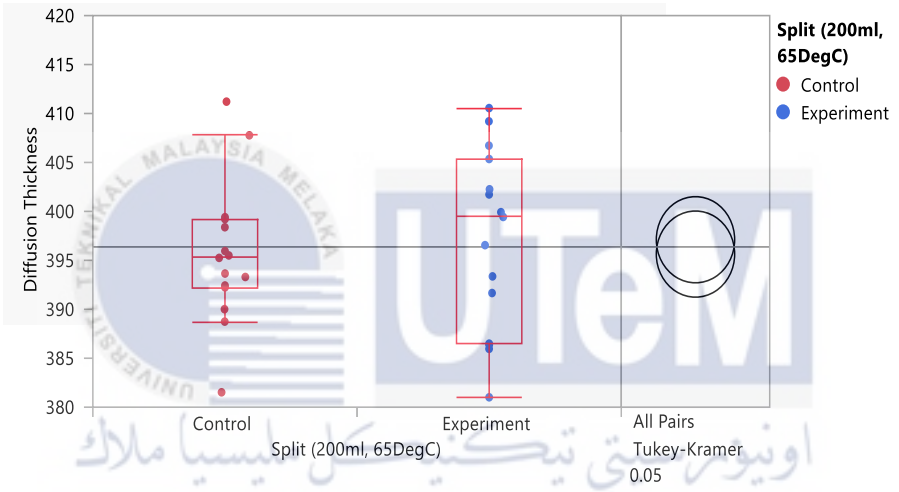


Figure 4.2: Oxide Thickness Comparison for Recipe 2 (200ml, 65°c)

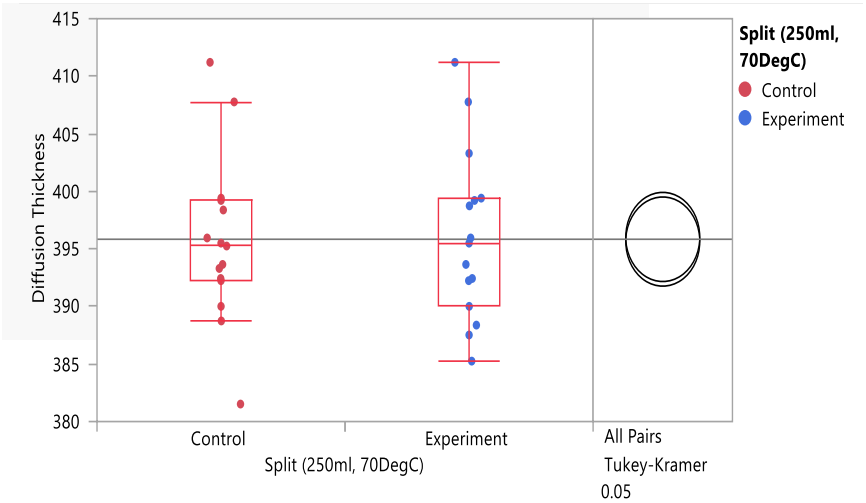


Figure 4.3: Oxide Thickness Comparison for Recipe 3 (250ml, 70°C)

Table 4.4: Oxide Thickness Measurement Result

Experimental recipe	p-value	Statistical Analysis	p-value Rank
Recipe 1 : 150ml, 60ºC	0.0648	insignificant difference to control data due to p-value > 0.05	1 (lowest)
Recipe 2 : 200ml, 65ºC	0.3166	insignificant difference to control data due to p-value > 0.05	2 (middle)
Recipe 3 : 250ml, 70ºC	0.4411	insignificant difference to control data due to p-value > 0.05	3 (highest)

4.4 Result of Reverse Biased Test Dielectric (RBTDE)

The experimental wafer that undergoes rework using cleaning Recipe 3 is then collected at the cell tester. The wafer is then submitted as a reliability test sample for the thermal cycling test, and the maximum temperature is measured under two conditions, 0 hour and 120hour. Twenty pieces of the control wafer and experimental data of the maximum temperature are recorded in Table 4.5 for 0 hour and 120hour. Maximum temperature for both experimental and control compared with the hotspot level from Table 3.2. The test data will be rejected if it reaches levels 3 and 4, which is more than 160ºC. Based on the recorded data Time : 0 hour, the maximum temperature recorded for Experimental data is 136.8ºC, while control data recorded maximum temperature at 119.6ºC. While for Time: 120 hours, the recorded maximum temperature for experimental data is 141.9oC and 119.9ºC for control data. It is observed that both the pre test (Time : 0 hour) and the post test (Time: 120hours) for experimental data are within level 2 hotspot criteria and accepted as a passing result for this test. The result was within the maximum temperature range defined in Table 3.2, which is inline with Wohlgemuth et al. (2000) that the result can be accepted if no badly damaged cell is observed after being subjected to long-term heat cycling.

Table 4.5: Max Temperature Data for Pre Time : 0 hour & 120hours

Split Run	Wafer Number	Max Temperature , °C	
		Pre Test (Time : 0 hour)	Post Test (Time : 120 hours)
Experiment	Wafer 1	106.30	111.50
Experiment	Wafer 2	105.50	114.40
Experiment	Wafer 3	103.70	114.80
Experiment	Wafer 4	106.70	111.30
Experiment	Wafer 5	106.40	108.90
Experiment	Wafer 6	103.00	110.90
Experiment	Wafer 7	115.40	130.10
Experiment	Wafer 8	104.00	106.00
Experiment	Wafer 9	98.30	101.80
Experiment	Wafer 10	108.20	111.10
Experiment	Wafer 11	107.90	108.30
Experiment	Wafer 12	103.40	101.90
Experiment	Wafer 13	116.40	114.70
Experiment	Wafer 14	112.90	110.20
Experiment	Wafer 15	106.70	109.00
Experiment	Wafer 16	136.80	137.40
Experiment	Wafer 17	112.20	108.60
Experiment	Wafer 18	111.40	112.30
Experiment	Wafer 19	105.40	109.60
Experiment	Wafer 20	108.40	114.00
Control	Wafer 1	108.10	113.10
Control	Wafer 2	108.10	110.90
Control	Wafer 3	101.70	103.60
Control	Wafer 4	106.60	110.20
Control	Wafer 5	106.90	110.90
Control	Wafer 6	102.60	106.80
Control	Wafer 7	112.10	119.30
Control	Wafer 8	110.50	110.40
Control	Wafer 9	100.00	102.40
Control	Wafer 10	104.50	106.10
Control	Wafer 11	108.80	108.80
Control	Wafer 12	100.90	99.10
Control	Wafer 13	107.70	114.40
Control	Wafer 14	106.60	107.80
Control	Wafer 15	100.30	102.90
Control	Wafer 16	105.30	106.40
Control	Wafer 17	109.80	109.40
Control	Wafer 18	103.30	103.30
Control	Wafer 19	107.00	110.50
Control	Wafer 20	110.20	110.10

In comparison of the probability value between experimental and control data, it is observed that experimental data is insignificant different from the control data with a p-value of 0.6491 in Table 4.6 based on the JMP Wilcoxon test analysis plotted in Figure 4.4 for Time : 0 hour. This analysis suggested that there is no significant impact on the wafer reliability of the experimental data on using the cleaning recipe 3.

For Time: 120 hours , plotted JMP using Wilcoxon analysis in Figure 4.5 also showing similar condition to Time : 0 hour as observing p-value of 0.4695 in Table 4.6 identified that the experimental data is insignificant different to the maximum temperature of control data. This analysis supported that there is no significant impact on the wafer reliability under the extreme temperature of reliability test of 120hour duration on the cleaning recipe 3 experimental results.

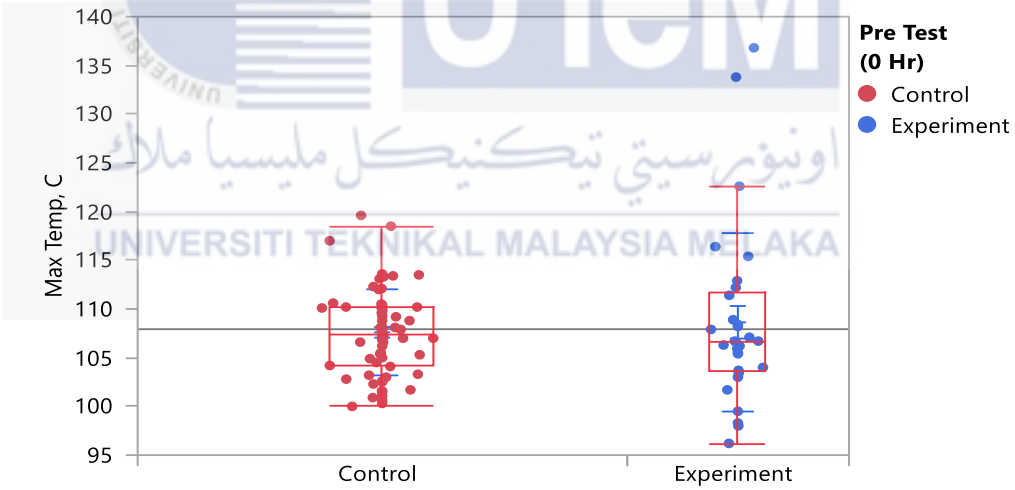


Figure 4.4: Pre Test data at 0 hour

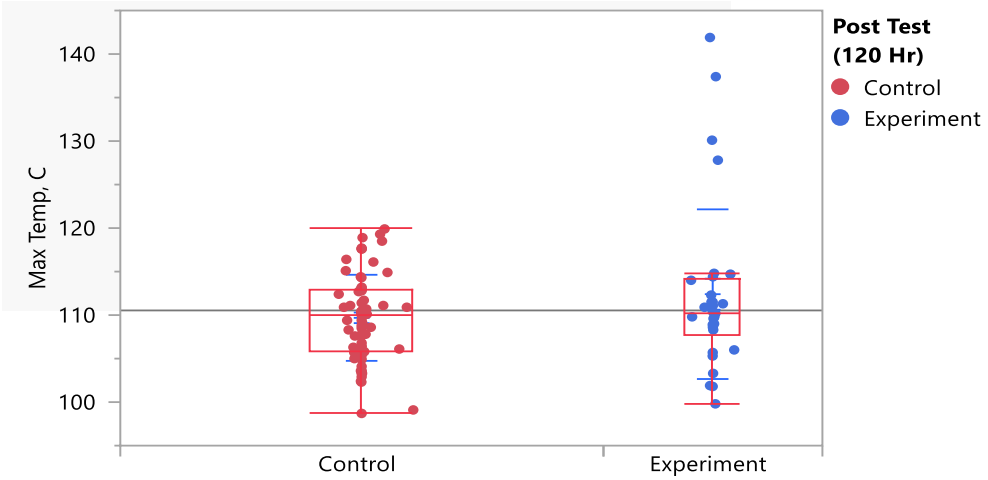


Figure 4.5: Post Test data at 120 hours

Table 4.6: RBTDE Test Result

Test duration	Material	Mean value	Standerd Deviation value	p-value	Statistical Analysis
Pre Test	Control	107.60	4.4169	0.6491	Experiment data showed insignificant difference to Control data due to p-value > 0.05
	Experiment	108.63	9.1578		
Post Test	Control	109.69	4.9462	0.4595	Experiment data showed insignificant difference to Control data due to p-value > 0.05
	Experiment	112.43	9.7482		

4.5 Result of Autoclave HAST Chamber (ACL) Test

The experimental wafer that is collected from the cell tester is submitted for Autoclave HAST chamber (ACL) testing under severe temperature (121^{o}C) and relative humidity (100%) conditions for 168 hours duration. Delta value of pre and post data of Voltage Open Circuit (Voc), Short circuit current (Isc), Fill factor (FF), Power Conversion Efficiency (EFF) and Maximum Power (Pmax) recorded in Table 4.7 for both experimental and control data. Maximum degradation for experimental Voc was recorded at 0.485% compared to control data at 0.785%. Maximum degradation for experimental Isc was

recorded at 0.258% compared to control data at 0.415%. Maximum degradation for experimental FF was recorded at 0.588% compared to control data at 0.541%. Maximum degradation for experimental EFF was recorded at 0.999% compared to control data at 1.040%. The maximum degradation of Pmax of the experimental wafer is -0.999%, while -1.040% for control data. In summary, Voc, Isc, FF, EFF, and Pmax data concluded that the experimental wafer is passing Autoclave HAST chamber (ACL) reliability testing as the results show within the maximum admissible degradation limit of -5%.

Table 4.7: Delta ata Electrical Parameter and Maximum Power Data for Pre Time : 0 hour & 120hours

Split Run	**Wafer No**	**dVoc**	**dIsc**	**dFF**	**dEFF**	**dPmax**
Experiment	Wafer 1	-0.484%	-0.258%	0.074%	-0.667%	-0.667%
Experiment	Wafer 2	-0.485%	-0.195%	-0.322%	-0.999%	-0.999%
Experiment	Wafer 3	-0.336%	-0.121%	-0.541%	-0.995%	-0.995%
Experiment	Wafer 4	-0.314%	-0.231%	0.454%	-0.093%	-0.093%
Experiment	Wafer 5	-0.329%	-0.123%	-0.211%	-0.662%	-0.662%
Experiment	Wafer 6	-0.341%	-0.179%	-0.480%	-0.997%	-0.997%
Experiment	Wafer 7	-0.305%	-0.069%	-0.312%	-0.684%	-0.684%
Experiment	Wafer 8	-0.352%	-0.243%	0.091%	-0.504%	-0.504%
Experiment	Wafer 9	-0.195%	-0.210%	-0.145%	-0.549%	-0.549%
Experiment	Wafer 10	-0.401%	-0.198%	-0.116%	-0.713%	-0.713%
Experiment	Wafer 11	-0.416%	-0.074%	0.447%	-0.044%	-0.044%
Experiment	Wafer 12	-0.404%	-0.114%	-0.061%	-0.578%	-0.578%
Control	Wafer 1	-0.475%	-0.167%	0.018%	-0.624%	-0.624%
Control	Wafer 2	-0.147%	-0.237%	-0.121%	-0.503%	-0.503%
Control	Wafer 3	-0.203%	-0.155%	-0.457%	-0.813%	-0.813%
Control	Wafer 4	-0.201%	-0.123%	0.155%	-0.168%	-0.169%
Control	Wafer 5	-0.482%	-0.231%	-0.098%	-0.809%	-0.809%
Control	Wafer 6	-0.467%	-0.200%	0.099%	-0.567%	-0.567%
Control	Wafer 7	-0.365%	-0.218%	-0.155%	-0.737%	-0.737%
Control	Wafer 8	-0.292%	-0.139%	-0.281%	-0.709%	-0.709%
Control	Wafer 9	-0.785%	-0.221%	0.647%	-0.364%	-0.364%
Control	Wafer 10	-0.272%	-0.114%	-0.290%	-0.674%	-0.674%
Control	Wafer 11	-0.106%	-0.288%	-0.359%	-0.751%	-0.751%
Control	Wafer 12	-0.003%	-0.415%	-0.588%	-1.004%	-1.004%

In the comparison of the probability value between experimental and control data, it is observed that experimental data is insignificant different to the control data, with a p-value of 0.6150 in Table 4.8 based on the dPmax Wilcoxon test analysis plotted in Figure 4.6. This analysis suggested that there is no significant impact on the wafer reliability under Autoclave HAST chamber (ACL) testing of the experimental data using the cleaning recipe 3 compared to the control data.

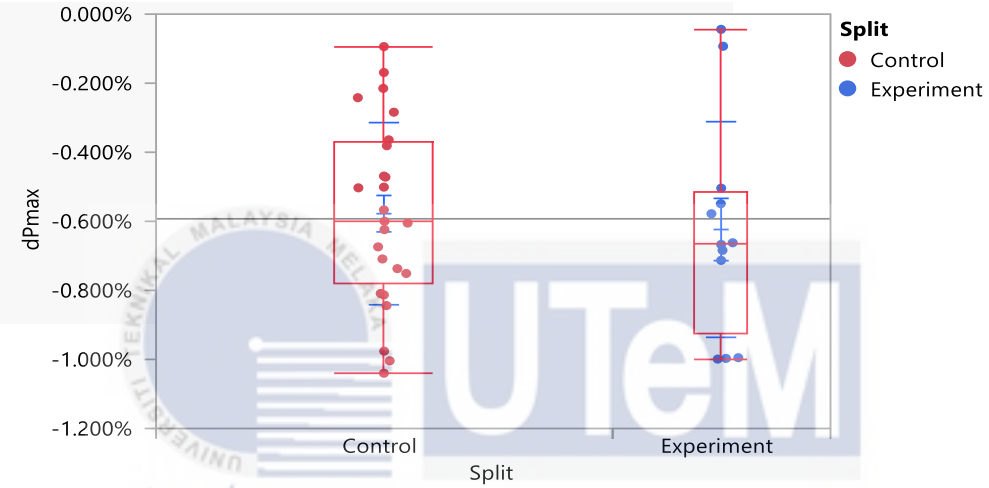


Figure 4.6: dPmax analysis from ACL Test

Table 4.8: ACL Test Result

Material	Mean value	Standerd Deviation value	p-value	Statistical Analysis
Control	-0.005779	0.002637	0.6150	Experiment data showed insignificant difference to Control data due to p-value > 0.05
Experiment	-0.006238	0.003122		

4.6 Validation Result of Selected Cleaning Recipe

100 pieces of data were collected for both experiment and control data, and the Power Conversion Efficiency, Electrical yield and Cosmetic yield data were compiled in Table 4.9.

Data population and distribution between experimental being compared with control data to ensure it is within p-value > 0.05 under 95% confidence interval.

Table 4.9: Power Conversion Efficiency , Electrical Yield and Cosmetic Data Comparison

Experiment				Control			
Wafer Number	**Efficiency**	**Electrical Yield**	**Cosmetic Yield**	**Wafer Number**	**Efficiency**	**Electrical Yield**	**Cosmetic Yield**
Wafer 1	23.01	Yielding	Bin A	Wafer 1	22.84	Yielding	Bin A
Wafer 2	23.08	Yielding	Bin B	Wafer 2	23.27	Yielding	Bin A
Wafer 3	22.94	Yielding	Bin A	Wafer 3	22.94	Yielding	Bin A
Wafer 4	23.02	Yielding	Bin B	Wafer 4	23.12	Yielding	Bin A
Wafer 5	22.89	Yielding	Bin A	Wafer 5	23.26	Yielding	Bin D
Wafer 6	22.81	Yielding	Bin A	Wafer 6	22.99	Yielding	Bin C
Wafer 7	22.95	Yielding	Bin B	Wafer 7	22.81	Yielding	Bin B
Wafer 8	22.91	Yielding	Bin D	Wafer 8	23.29	Yielding	Bin B
Wafer 9	22.93	Yielding	Bin A	Wafer 9	23.18	Yielding	Bin C
Wafer 10	23.05	Yielding	Bin B	Wafer 10	23.13	Yielding	Bin B
Wafer 11	23.06	Yielding	Bin A	Wafer 11	22.79	Yielding	Bin B
Wafer 12	23.14	Yielding	Bin A	Wafer 12	22.48	Yielding	Bin A
Wafer 13	22.97	Yielding	Bin A	Wafer 13	22.59	Yielding	Bin A
Wafer 14	23.04	Yielding	Bin A	Wafer 14	22.67	Yielding	Bin B
Wafer 15	23.07	Yielding	Bin B	Wafer 15	22.65	Yielding	Bin B
Wafer 16	23.02	Yielding	Bin A	Wafer 16	22.80	Yielding	Bin C
Wafer 17	23.14	Yielding	Bin B	Wafer 17	22.86	Yielding	Bin B
Wafer 18	23.09	Yielding	Bin B	Wafer 18	22.80	Yielding	Bin B
Wafer 19	22.99	Yielding	Bin B	Wafer 19	22.63	Yielding	Bin B
Wafer 20	23.12	Yielding	Bin B	Wafer 20	22.80	Yielding	Bin C
Wafer 21	23.09	Yielding	Bin B	Wafer 21	22.83	Yielding	Bin A
Wafer 22	23.05	Yielding	Bin B	Wafer 22	22.54	Yielding	Bin A
Wafer 23	23.05	Yielding	Bin B	Wafer 23	22.79	Yielding	Bin A
Wafer 24	23.10	Yielding	Bin B	Wafer 24	22.81	Yielding	Bin B
Wafer 25	23.05	Yielding	Bin B	Wafer 25	22.76	Yielding	Bin B
Wafer 26	22.89	Yielding	Bin B	Wafer 26	22.79	Yielding	Bin B
Wafer 27	23.06	Yielding	Bin B	Wafer 27	22.57	Yielding	Bin A
Wafer 28	23.09	Yielding	Bin B	Wafer 28	23.04	Yielding	Bin B
Wafer 29	23.01	Yielding	Bin B	Wafer 29	22.78	Yielding	Bin B
Wafer 30	23.00	Yielding	Bin B	Wafer 30	22.56	Yielding	Bin B

4.7 Result of Power Conversion Efficiency Analysis for Small Quantity Run

The 100 pieces of experimental and control data of the Power Conversion Efficiency performance were plotted in JMP and analyze using the Wilcoxon comparison test. Comparison data between an experimental and control group of data shown in Figure 4.7 showed that the population distribution of the experiment sample of cell Power Conversion Efficiency is significant different to the control sample with a p-value of < 0.0001. However, the mean statistical data for experimental is higher, at 22.98%, compared to the control mean value of 22.84% shown in Table 4.10. Higher Power Conversion Efficiency is recommended in the solar cell as it will produce a higher Watt (W) value. This comparison analysis suggested that the experimental data is accepted as it produces a better mean Power Conversion Efficiency value even though the p-value is a significant difference to control data. According to Park et al. (1993), integrating such "critical cleaning" becomes important for better efficient solar cells as contamination and impurities are removed that impact the charge carrier's lifetime and increase the efficiency. In this study, the wafer undergoes cleaning twice under the HFO_3 process, which is explained by the increase in efficiency compared to standard production wafer as the contamination is completely and efficiently removed from the wafer surface.

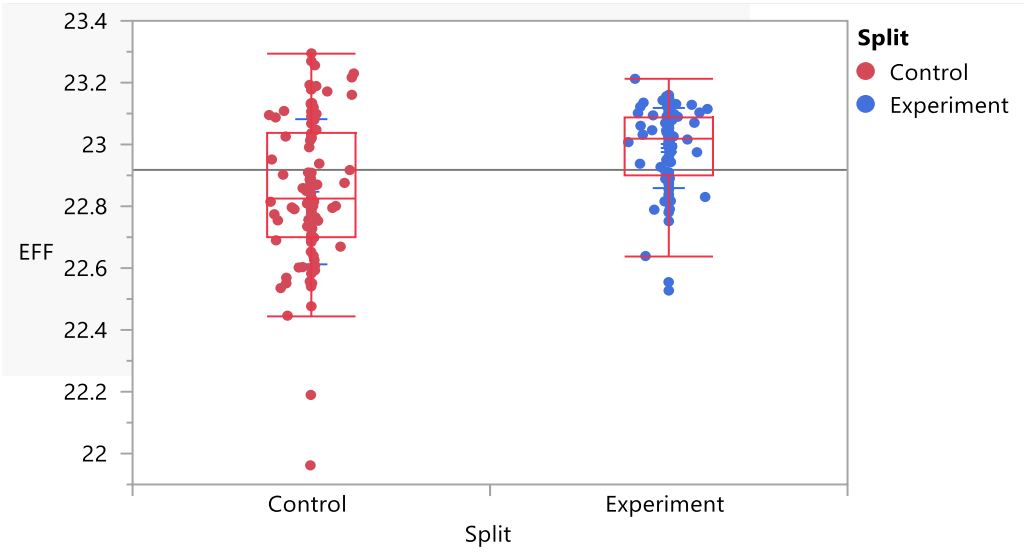


Figure 4.7: JMP Analysis for Power Conversion Efficiency

Table 4.10: Power Conversion Efficiency (EFF) result

Material	Mean value	Standerd Deviation value	p-value	Statistical Analysis
Control	22.84	0.2348	<0.0001*	Experiment data showed significant difference to Control data due to p-value > 0.05
Experiment	22.98	0.1296		

4.8 Result of Electrical Yield Analysis for Small Quantity Run

The Electrical Yield of experimental and control is also being monitored and compared in this study to see the impact of Electrical Yield. The wafer is tested in a cell tester and sorted according to yielding and non-yielding bin. The yielding bin is defined by the electrical limit value set up in the cell tester. Those wafers that are unable to meet the electrical limit value will be rejected and fall into non-yielding bin. Compiled data of the 100 pieces of experimental and control wafers are shown in Table 4.9. The Electrical Yield data is then plotted in JMP, and the distribution frequency is shown by using the contingency table in Figure 4.8. Chi-square data shows that the p-value is insignificant difference between

the two groups experimental and control data with p-value of 0.6495 shown in Table 4.11. This analysis suggested that the experimental data is statistically comparable and has no impact on the Electrical Yield performance. The result of Electrical Yield is inline with Power Conversion Efficiency value as the yielding bin is better performance for experimental compared to standard production wafer that only undergo one time cleaning, which also clarified by Zhang et al. (2021).

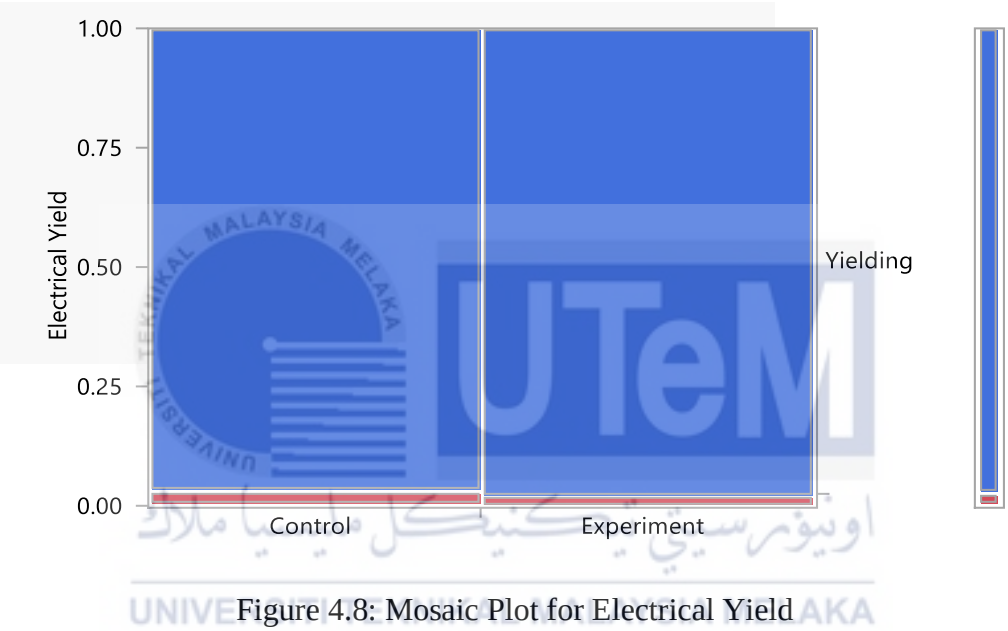


Figure 4.8: Mosaic Plot for Electrical Yield

Table 4.11: Electrical Yield result

Material	Non-yielding	Yielding	p-value	Statistical Analysis
Control	1.50	48.50	0.6495	Experiment data showed significant difference to Control data due to p-value > 0.05
Experiment	1.00	49.00		

4.9 Result of Cosmetic Yield Analysis for Small Quantity Run

Cosmetic Yield is one important monitoring result to determine if the cleaning recipe meets the product requirement. Incomplete diffusion layer removal will contaminate and

cause a stain mark on the wafer surface. In this study, 100 pieces of the experimental wafer were inspected and categorised under different cosmetic categories based on the wafer surface appearance. Figure 4.9 shows the Mosaic plot that identifies wafer population distribution differences between experimental and control data on cosmetic binning. The analysis also suggested that there is no significant difference between the two data groups as the p-value is at 0.8709 with a probability value of more than 0.05 as per Table 4.12.

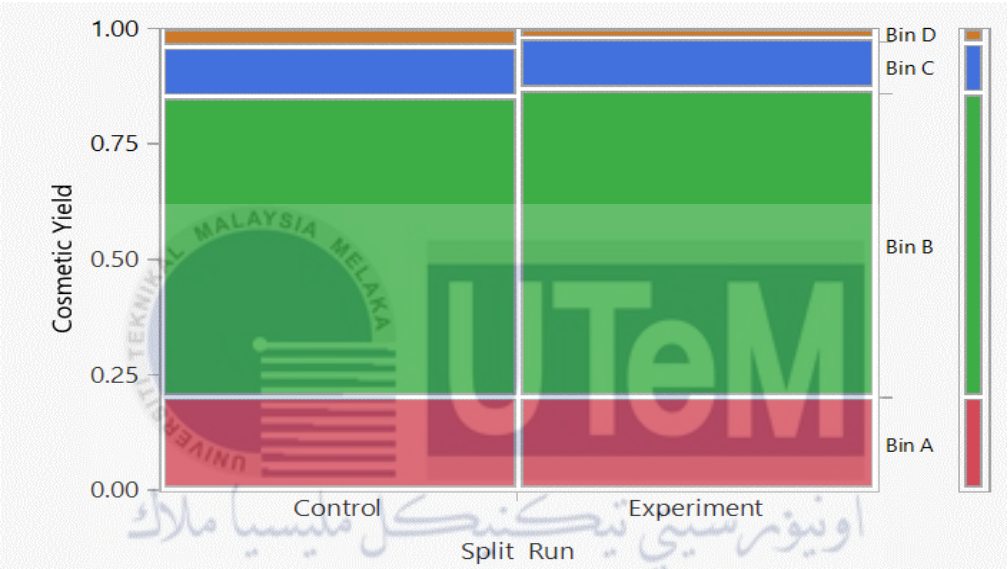


Figure 4.9: Mosaic Plot for Cosmetic Yield

Table 4.12: Cosmetic Yield result

Material	Cosmetic Yield				p-value	Statistical Analysis
	Bin A	Bin B	Bin C	Bin D		
Control	10.00	32.50	5.50	2.00	0.8709	Experiment data showed significant difference to Control data due to p-value > 0.05
Experiment	10.00	33.50	5.50	1.00		

4.10 Result of Visual Inspection for High Volume Quantity Run

In a higher volume quantity run, a visual inspection was conducted post rework cleaning recipe to verify oxide removal effectiveness. In this activity, a total of 60 pieces of

the wafer were inspected visually and selected from slot 1, slot 25 and slot 50 of 20 cassettes. Based on the visual inspection image in Table 4.13, the selected experimental cleaning recipe removed the diffusion layer, even running at a higher volume run.

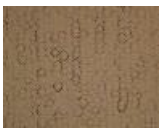
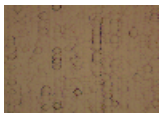
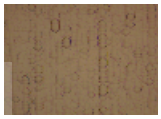
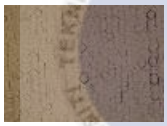
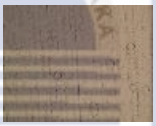
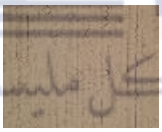
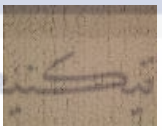
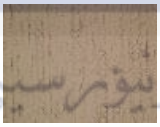
Table 4.13: Sampling Visual Inspection data

Cassette Number	Wafer appearance			Cassette Number	Wafer appearance		
	Slot 1	Slot 25	Slot 50		Slot 1	Slot 25	Slot 50
Cassette 1	0	0	0	**Cassette 11**	0	0	0
Cassette 2	0	0	0	**Cassette 12**	0	0	0
Cassette 3	0	0	0	**Cassette 13**	0	0	0
Cassette 4	0	0	0	**Cassette 14**	0	0	0
Cassette 5	0	0	0	**Cassette 15**	0	0	0
Cassette 6	0	0	0	**Cassette 16**	0	0	0
Cassette 7	0	0	0	**Cassette 17**	0	0	0
Cassette 8	0	0	0	**Cassette 18**	0	0	0
Cassette 9	0	0	0	**Cassette 19**	0	0	0
Cassette 10	0	0	0	**Cassette 20**	0	0	0

4.11 Result of Microscopic Inspection ((High Volume Quantity Run)

A sampling of 10 pieces of the wafer was selected and inspected at 5 points on the wafer (Upper Right, Upper Left, Centre, Lower Right, Lower Left). Based on the microscopic inspection shown in Table 4.14, the selected experimental recipe observed a cleaned wafer without a leftover diffusion layer. This shows that the cleaning recipe is also fit to run under a high volume run as no abnormality was captured on the wafer surface through microscopic inspection.

Table 4.14: Sampling Microscopic Inspection Images

Wafer no	Upper Right (UR)	Upper Left (UL)	Centre (C)	Lower Right (LR)	Lower Left (LL)
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					

4.12 Result of Power Conversion Efficiency Analysis for High Quantity Run

A total of 1000 pieces of experimental and control data on the Power Conversion Efficiency performance was compiled in Table 4.15, plotted in JMP, and analyzed using the Wilcoxon comparison test. Comparison data between an experimental and control group of data shown in Figure 4.10 showed that the population distribution of the experiment sample of cell Power Conversion Efficiency is significant different to the control sample with a p-value of < 0.0001 as per value shown in Table 4.16. The higher volume quntity runs replicated the smaller run quantity of 100 pieces which observed mean statistical experimental is higher at 22.94% compared to the control mean value at 22.88%. This comparison analysis also suggested that the experimental data is accepted as it produces a better mean Power Conversion Efficiency value even though the p-value is a significant difference to control data.

Table 4. 15: Power Conversion Efficiency Data for High Volume Quantity Run

Experiment				Control			
Wafer Number	**Efficiency**	**Wafer Number**	**Efficiency**	**Wafer Number**	**Efficiency**	**Wafer Number**	**Efficiency**
1	23.05	51	22.81	1	22.97	51	23.07
2	22.94	52	22.83	2	23.26	52	22.69
3	22.97	53	22.82	3	23.04	53	22.78
4	22.97	54	22.78	4	23.21	54	23.03
5	22.99	55	23.09	5	22.88	55	23.03
6	22.77	56	22.98	6	22.92	56	22.82
7	22.86	57	22.88	7	23.00	57	22.89
8	22.95	58	22.79	8	23.02	58	23.19
9	22.96	59	22.77	9	22.87	59	22.93
10	22.83	60	22.83	10	22.87	60	23.01
11	23.08	61	22.97	11	22.43	61	22.95
12	23.06	62	22.63	12	22.94	62	22.92
13	23.02	63	23.04	13	22.97	63	23.04
14	22.94	64	22.94	14	22.83	64	23.06
15	23.07	65	22.97	15	22.67	65	23.05
16	22.94	66	22.95	16	22.75	66	23.04

17	22.79	67	23.13	17	22.53	67	23.18
18	22.94	68	22.75	18	22.93	68	22.56
19	23.03	69	22.60	19	22.77	69	22.87
20	22.99	70	22.93	20	22.83	70	23.01
21	23.01	71	22.80	21	22.82	71	23.09
22	23.06	72	23.00	22	22.94	72	22.81
23	23.00	73	23.07	23	22.74	73	22.90
24	23.09	74	22.63	24	22.55	74	23.10
25	22.16	75	22.95	25	22.08	75	22.59
26	23.01	76	23.01	26	22.33	76	22.63
27	22.94	77	23.05	27	22.63	77	22.90
28	22.98	78	22.62	28	22.78	78	22.80
29	22.94	79	22.95	29	22.30	79	22.86
30	22.99	80	22.94	30	22.51	80	22.91
31	22.97	81	22.87	31	22.37	81	22.73
32	22.95	82	22.79	32	22.77	82	23.13
33	23.01	83	22.91	33	22.77	83	22.77
34	22.93	84	22.79	34	22.51	84	23.00
35	22.41	85	22.87	35	22.78	85	22.72
36	22.85	86	22.94	36	22.79	86	22.85
37	22.85	87	22.93	37	22.82	87	22.65
38	22.98	88	22.84	38	22.73	88	22.97
39	22.90	89	22.82	39	22.89	89	22.60
40	23.05	90	22.83	40	22.95	90	22.88
41	23.12	91	22.90	41	22.70	91	22.89
42	22.89	92	22.91	42	22.58	92	22.98
43	22.89	93	22.92	43	22.69	93	22.69
44	21.95	94	22.87	44	22.70	94	23.03
45	22.94	95	22.75	45	22.86	95	23.09
46	22.11	96	22.96	46	22.85	96	23.14
47	22.99	97	22.95	47	22.91	97	23.12
48	22.95	98	22.91	48	22.83	98	22.49
49	22.93	99	22.86	49	22.81	99	22.86
50	22.98	100	23.05	50	22.74	100	23.05

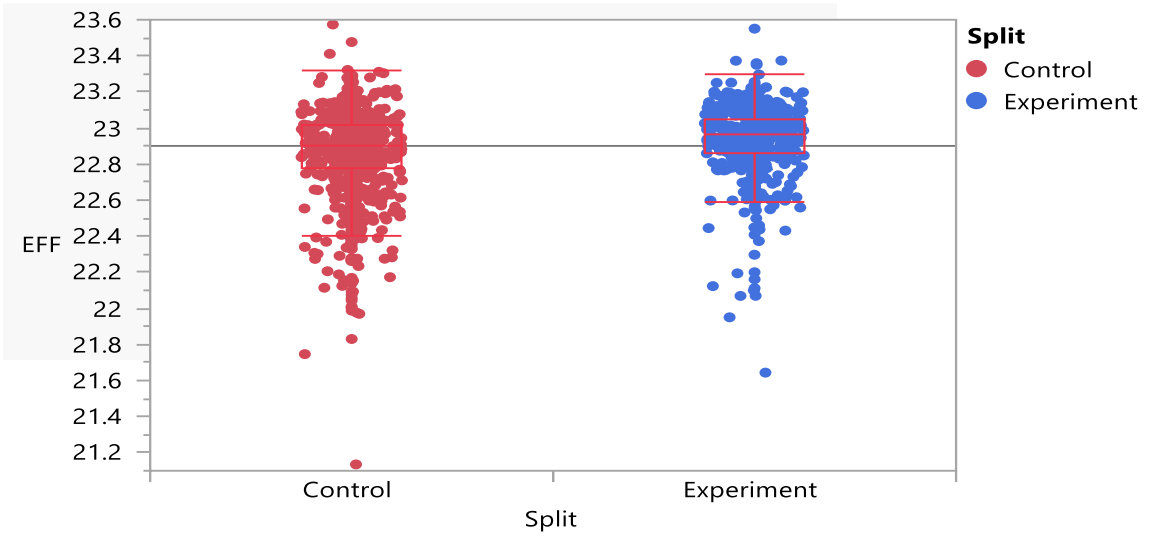


Figure 4.10: JMP Validation for Efficiency

Table 4.16: Power Conversion Efficiency (EFF) result

Material	Mean value	Standerd Deviation value	p-value	Statistical Analysis
Control	22.86	0.2387	<0.0001*	Experiment data showed significant difference to Control data due to p-value < 0.05
Experiment	22.94	0.1710		

4.13 Result of Electrical Yield Analysis for High Quantity Run

For higher volume run, a similar method of smaller quantity experimental run where wafer collected after running cell tester and sorted according to yielding and non-yielding bin. Compiled data of the 1000 pieces of experimental and control wafers are shown in Table 4.17. The electrical yield data is then plotted in JMP, and the distribution frequency is shown using the contingency table in Figure 4.11. Chi-square data showed that the p-value is insignificant difference with a p-value of 0.8177 in Table 4.18 between the experimental and control data groups. This analysis shows that validation run for a higher volume of experimental data is statistically comparable and has no impact on the electrical yield performance.

Table 4.17: Electrical Yield Data for High Volume Run

Experiment				Control			
Wafer Number	**Electrical Yield**	**Wafer Number**	**Electrical Yield**	**Wafer Number**	**Electrical Yield**	**Wafer Number**	**Electrical Yield**
1	Yielding	51	Yielding	1	Yielding	51	Yielding
2	Yielding	52	Yielding	2	Yielding	52	Yielding
3	Yielding	53	Yielding	3	Yielding	53	Yielding
4	Yielding	54	Yielding	4	Yielding	54	Yielding
5	Yielding	55	Yielding	5	Yielding	55	Yielding
6	Yielding	56	Yielding	6	Yielding	56	Yielding
7	Yielding	57	Yielding	7	Yielding	57	Yielding
8	Yielding	58	Yielding	8	Yielding	58	Yielding
9	Yielding	59	Yielding	9	Yielding	59	Yielding
10	Yielding	60	Yielding	10	Yielding	60	Yielding
11	Yielding	61	Yielding	11	Yielding	61	Yielding
12	Yielding	62	Yielding	12	Yielding	62	Yielding
13	Yielding	63	Yielding	13	Yielding	63	Yielding
14	Yielding	64	Yielding	14	Yielding	64	Yielding
15	Yielding	65	Yielding	15	Yielding	65	Yielding
16	Yielding	66	Yielding	16	Yielding	66	Yielding
17	Yielding	67	Yielding	17	Yielding	67	Yielding
18	Yielding	68	Yielding	18	Yielding	68	Yielding
19	Yielding	69	Yielding	19	Yielding	69	Yielding
20	Yielding	70	Yielding	20	Yielding	70	Yielding
21	Yielding	71	Yielding	21	Yielding	71	Yielding
22	Yielding	72	Yielding	22	Yielding	72	Yielding
23	Yielding	73	Yielding	23	Yielding	73	Yielding
24	Yielding	74	Yielding	24	Yielding	74	Yielding
25	Non-yielding	75	Yielding	25	Yielding	75	Yielding
26	Yielding	76	Yielding	26	Yielding	76	Yielding
27	Yielding	77	Yielding	27	Yielding	77	Yielding
28	Yielding	78	Yielding	28	Yielding	78	Yielding
29	Yielding	79	Yielding	29	Yielding	79	Yielding
30	Yielding	80	Yielding	30	Yielding	80	Yielding
31	Yielding	81	Yielding	31	Yielding	81	Yielding
32	Yielding	82	Yielding	32	Yielding	82	Yielding
33	Yielding	83	Yielding	33	Yielding	83	Yielding
34	Yielding	84	Yielding	34	Yielding	84	Yielding
35	Yielding	85	Yielding	35	Yielding	85	Yielding
36	Yielding	86	Yielding	36	Yielding	86	Yielding
37	Yielding	87	Yielding	37	Yielding	87	Yielding
38	Yielding	88	Yielding	38	Yielding	88	Yielding
39	Yielding	89	Yielding	39	Yielding	89	Yielding

40	Yielding	90	Yielding	40	Yielding	90	Yielding
41	Yielding	91	Yielding	41	Yielding	91	Yielding
42	Yielding	92	Yielding	42	Yielding	92	Yielding
43	Yielding	93	Yielding	43	Yielding	93	Yielding
44	Non-yielding	94	Yielding	44	Yielding	94	Yielding
45	Yielding	95	Yielding	45	Yielding	95	Yielding
46	Non-yielding	96	Yielding	46	Yielding	96	Yielding
47	Yielding	97	Yielding	47	Yielding	97	Yielding
48	Yielding	98	Yielding	48	Yielding	98	Yielding
49	Yielding	99	Yielding	49	Yielding	99	Yielding
50	Yielding	100	Yielding	50	Yielding	100	Yielding

Figure 4.11: Mosaic Plot for Electrical Yield

Table 4.18: Electrical Yield result

Material	Non-yielding	Yielding	p-value	Statistical Analysis
Control	0.45	49.55	0.8177	Experiment data showed significant difference to Control data due to p-value > 0.05
Experiment	0.50	49.50		

4.14 Result of Cosmetic Yield Analysis for High Quantity Run

The wafer appearance of the high volume run experimental wafer is also inspected and compared with the production control good wafer. Figure 4.12 shows that the Mosaic plot of the experiment wafer has a higher population distribution of bin A (highest quality bin) compared to the control. The analysis in Table 4.19 also observed a significant difference between the two data groups as the p-value is at 0.0001. However, as the bin A distribution for experimental is higher than control, the cosmetic yield performance is accepted as it is considered statistically different with 13.85% higher cosmetic yield performance.

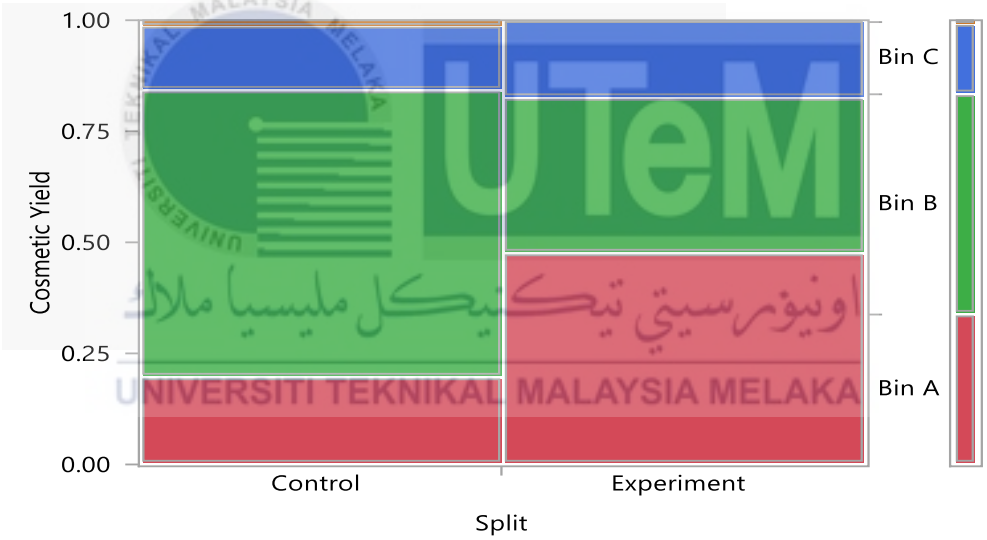


Figure 4.12: JMP Validation for Cosmetic Yield

Table 4.19: Cosmetic Yield result

Material	Electrical Yield				p-value	Statistical Analysis
	Bin A	Bin B	Bin C	Bin D		
Control	9.95	32.25	7.25	0.55	<0.0001*	Experiment data showed significant difference to Control data due to p-value < 0.05
Experiment	23.80	17.50	8.70	0.00		

4.15 Summary

Experiments were conducted accordingly as per process flow. All objectives in this study were successful with no significant impact on the product quality. Comparison data between experimental and control data was also conducted starting from the selection of the rework cleaning recipe, reliability testing, smaller volume experimental run and validation of cleaning recipe through higher volume run. This study proposed an optimum cleaning recipe in diffusion layer removal with confirmation of the reliability performance similar to the excellent production wafer that did not undergo a rework process. The smaller and higher volume quantity run resulted in a statistically insignificant difference compared to the control data.

CHAPTER 5

CONCLUSION AND RECOMMENDATION

5.1 Conclusion

In this study, the flow of selecting the best cleaning recipe for removing the diffusion layer has been conducted by evaluating it through reliability testing and two experimental runs. The main goal of this study is to obtain the best cleaning recipe that can rework the defective wafer and ship it to the customer without affecting the product quality. At the same time, doing a rework of the rejected wafer using the cleaning recipe will lower the scrap yield loss and improve the operational cost of building the cells. This study completed all requirements in qualifying the cleaning recipe, and the recipe was validated successfully without significant impact compared to standard product quality.

The first objective of this study is to select the best cleaning recipe for removing the diffusion layer of the rejected wafer. Three different experiment recipes of HFO_3 module dosing volume and temperature combination change have been evaluated by three different activities, which are visual inspection, optical microscopic inspection, and oxide thickness measurement. Every wafer in each split run has been inspected post cleaning recipe, and the water is spotless with no abnormal stain observed on the wafer surface for every three split experiment recipes. A sampling check was conducted through microscopic inspection of all three experiment splits and came out with a good wafer surface with no contamination observed. The third activity is by doing oxide thickness measurement on the wafer. All three combination recipes have a statistically insignificant difference with control good production wafer and can be accepted as the cleaning recipe with a p-value of 0.0648, 0.3166, and 0.4411, respectively, for recipe 1, 2, and 3. However, in determining the best cleaning recipe,

a combination recipe of 250ml HFO_3 volume dosing and 70°C was selected due to its highest p-value, which showed the closest value to control data measurement compared to the other two HFO_3 combination recipes.

In the second objective, two types of reliability testing, reverse biased test dielectric (RBTDE) and Autoclave HAST chamber (ACL), are conducted on the experimental wafer that has undergone a selected cleaning process in objective 1. The result for RBTDE using JMP Wilcoxon comparison analysis was insignificant compared with the control run with a p-value of 0.6494 and 0.4696 for Pre Testing (Time: 0 hour) and Post Testing (Time: 120 hours), respectively. Second reliability testing under Autoclave HAST chamber (ACL) showed a similar response with an RBTDE result with a p-value of 0.6150, which shows an insignificant difference from the control run data. Based on the passing result of reliability testing, it was determined that the selected cleaning recipe was accepted and qualified as there was no impact on the product quality observed.

The third objective is to validate experimental data on Cell Power Conversion Efficiency, Electrical Yield and Cosmetic Yield and compare them with the control production wafer data. The completed product or cell from the rework cleaning recipe has to be comparable and not significantly different from control data to ensure no impact on the product quality. The result plotted using JMP analysis showed that the cell Power Conversion Efficiency is significantly different but better, with a higher mean value at 22.98% compared to the control value at 22.84%. Electrical yield resulted insignificant difference compared to control with a p-value of 0.6485, while cosmetic yield also observed no significant difference of p-value at 0.8709. All results from Cell Power Conversion Efficiency, Electrical Yield and Cosmetic Yield resulted in a positive and successful third objective. This study also conducted validation cleaning recipe in a higher volume quantity run of 1000pieces. Visual inspection and microscopic analysis were conducted and validated

that the diffusion layer on the experimental wafer could be removed completely. The result of Cell Power Conversion Efficiency, Electrical Yield and Cosmetic Yield compared to the standard production wafer to ensure it is comparable or better. Comparison analysis between experimental and control standard production wafer of 1000 pieces respectively for each split run of higher volume run observed 95% confidence interval resulted p-value of <0.0001, but higher mean value showed better Cell Power Conversion Efficiency for experimental data. A similar condition to Cosmetic Yield showed a p-value of < 0.0001, but a higher percentage of bin A supported that the experimental data is better than control data. Electrical Yield also observed a p-value of 0.8177, which defined the experimental data as insignificant and different from the control. Validation data on higher volume quantity run can meet normal production wafer level, which strongly supports that the selected cleaning recipe is safe to run without impacting the product quality. This study's success will help create another alternative for further cost reduction study from scrap yield loss.

5.2 Recommendation

Suggestion for future work is to apply the same concept of re-claim activity to other diffusion process steps in solar cell manufacturing. Rework or re-claim activity should be further explored for other process steps as the current study only focuses on defective wafer reject in the second process step. There is another two diffusions process step from total solar cell process flow, and the application of re-claim cleaning could also be successful in this process. Besides that, the same concept of re-claim cleaning could be evaluated and applied to the P-type silicon type, which could benefit solar cell makers that manufacture N-type and P-type silicon cells simultaneously. The other recommendation that could be made from this study is to expand and conduct a design of experiment (DOE) on the HFO_3 parameter range to benefit and improve electrical parameters, as observed good results from this study.

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APPENDICES

APPENDIX A : Table of Result for Reliability Test RBTDE

Split Run	Wafer Number	Max Temperature , °C	
		Pre Test (Time : 0 hour)	Post Test (Time : 120 hours)
Experiment	Wafer 1	106.30	111.50
Experiment	Wafer 3	103.70	114.80
Experiment	Wafer 4	106.70	111.30
Experiment	Wafer 5	106.40	108.90
Experiment	Wafer 6	103.00	110.90
Experiment	Wafer 8	104.00	106.00
Experiment	Wafer 9	98.30	101.80
Experiment	Wafer 11	107.90	108.30
Experiment	Wafer 12	103.40	101.90
Experiment	Wafer 13	116.40	114.70
Experiment	Wafer 14	112.90	110.20
Experiment	Wafer 18	111.40	112.30
Experiment	Wafer 19	105.40	109.60
Experiment	Wafer 20	108.40	114.00
Experiment	Wafer 21	101.70	105.70
Experiment	Wafer 23	108.90	109.80
Experiment	Wafer 24	98.00	99.80
Experiment	Wafer 25	105.90	109.80
Experiment	Wafer 26	133.80	141.90
Experiment	Wafer 28	106.20	110.40
Experiment	Wafer 29	107.10	111.50
Experiment	Wafer 30	96.20	103.30
Control	Wafer 1	108.10	113.10
Control	Wafer 2	108.10	110.90
Control	Wafer 3	101.70	103.60
Control	Wafer 4	106.60	110.20
Control	Wafer 5	106.90	110.90
Control	Wafer 6	102.60	106.80
Control	Wafer 8	110.50	110.40
Control	Wafer 9	100.00	102.40
Control	Wafer 11	108.80	108.80
Control	Wafer 12	100.90	99.10
Control	Wafer 14	106.60	107.80
Control	Wafer 15	100.30	102.90
Control	Wafer 16	105.30	106.40
Control	Wafer 17	109.80	109.40
Control	Wafer 18	103.30	103.30

Control	Wafer 19	107.00	110.50
Control	Wafer 21	103.20	103.60
Control	Wafer 22	118.50	117.70
Control	Wafer 23	107.00	109.00
Control	Wafer 24	102.30	105.10
Control	Wafer 25	112.00	113.20
Control	Wafer 29	113.30	111.40
Control	Wafer 30	102.50	102.30
Control	Wafer 31	110.10	109.40
Control	Wafer 32	109.30	108.30
Control	Wafer 33	104.10	105.80
Control	Wafer 34	110.10	108.60
Control	Wafer 35	110.60	110.70
Control	Wafer 36	104.20	104.90
Control	Wafer 37	108.80	110.40
Control	Wafer 38	119.60	119.90
Control	Wafer 39	112.00	98.70
Control	Wafer 40	108.10	111.10
Control	Wafer 41	113.50	115.10
Control	Wafer 42	101.50	103.30
Control	Wafer 43	112.30	112.80
Control	Wafer 44	108.10	108.50
Control	Wafer 45	101.10	107.60
Control	Wafer 46	110.40	112.90
Control	Wafer 47	107.20	110.10
Control	Wafer 48	101.60	105.00
Control	Wafer 49	107.20	112.40
Control	Wafer 50	109.60	116.10
Control	Wafer 51	105.50	111.10
Control	Wafer 52	106.90	117.60
Control	Wafer 53	105.00	107.80
Control	Wafer 54	102.80	105.80
Control	Wafer 55	107.20	112.70
Control	Wafer 56	106.20	111.70
Control	Wafer 57	100.60	106.30
Control	Wafer 58	113.10	118.50
Control	Wafer 59	110.20	116.40
Control	Wafer 60	103.00	105.40
Control	Wafer 61	104.90	114.30
Control	Wafer 62	107.90	112.60
Control	Wafer 63	110.50	107.60
Control	Wafer 64	113.60	110.00
Control	Wafer 65	109.20	104.10
Control	Wafer 66	117.00	118.90

APPENDIX B : Table of Result for Reliability Test ACL Test

Split Run	Wafer no	dVoc	dIsc	dFF	dEFF	dPmax
Experiment	1	-0.484%	-0.258%	0.074%	-0.667%	-0.667%
Experiment	2	-0.485%	-0.195%	-0.322%	-0.999%	-0.999%
Experiment	3	-0.336%	-0.121%	-0.541%	-0.995%	-0.995%
Experiment	4	-0.314%	-0.231%	0.454%	-0.093%	-0.093%
Experiment	5	-0.329%	-0.123%	-0.211%	-0.662%	-0.662%
Experiment	6	-0.341%	-0.179%	-0.480%	-0.997%	-0.997%
Experiment	7	-0.305%	-0.069%	-0.312%	-0.684%	-0.684%
Experiment	8	-0.352%	-0.243%	0.091%	-0.504%	-0.504%
Experiment	9	-0.195%	-0.210%	-0.145%	-0.549%	-0.549%
Experiment	10	-0.401%	-0.198%	-0.116%	-0.713%	-0.713%
Experiment	11	-0.416%	-0.074%	0.447%	-0.044%	-0.044%
Experiment	12	-0.404%	-0.114%	-0.061%	-0.578%	-0.578%
Control	1	-0.475%	-0.167%	0.018%	-0.624%	-0.624%
Control	2	-0.147%	-0.237%	-0.121%	-0.503%	-0.503%
Control	3	-0.203%	-0.155%	-0.457%	-0.813%	-0.813%
Control	4	-0.201%	-0.123%	0.155%	-0.168%	-0.169%
Control	5	-0.482%	-0.231%	-0.098%	-0.809%	-0.809%
Control	6	-0.467%	-0.200%	0.099%	-0.567%	-0.567%
Control	7	-0.365%	-0.218%	-0.155%	-0.737%	-0.737%
Control	8	-0.292%	-0.139%	-0.281%	-0.709%	-0.709%
Control	9	-0.785%	-0.221%	0.647%	-0.364%	-0.364%
Control	10	-0.272%	-0.114%	-0.290%	-0.674%	-0.674%
Control	11	-0.106%	-0.288%	-0.359%	-0.751%	-0.751%
Control	12	-0.003%	-0.415%	-0.588%	-1.004%	-1.004%
Control	13	-0.349%	-0.291%	-0.339%	-0.976%	-0.976%
Control	14	-0.455%	-0.246%	0.488%	-0.215%	-0.215%
Control	15	-0.416%	-0.071%	0.246%	-0.242%	-0.242%
Control	16	-0.505%	-0.158%	0.063%	-0.600%	-0.600%
Control	17	-0.419%	-0.158%	0.195%	-0.381%	-0.381%
Control	18	-0.471%	-0.173%	0.362%	-0.284%	-0.284%
Control	19	-0.588%	-0.262%	0.761%	-0.094%	-0.094%
Control	20	-0.263%	-0.214%	-0.024%	-0.501%	-0.501%
Control	21	-0.379%	-0.247%	-0.417%	-1.040%	-1.040%
Control	22	-0.556%	-0.136%	0.221%	-0.472%	-0.472%
Control	23	-0.393%	-0.141%	-0.312%	-0.844%	-0.844%
Control	24	-0.327%	-0.211%	-0.068%	-0.605%	-0.605%
Control	25	-0.646%	-0.305%	0.485%	-0.469%	-0.469%

APPENDIX C : Table of Result for Experimental Run (Quantity : 100pieces)

Split Run	Wafer Number	EFF	Electrical Yield	Cosmetic Yield
Experiment	Wafer 1	23.01	Yielding	Bin A
Experiment	Wafer 2	23.08	Yielding	Bin B
Experiment	Wafer 3	22.94	Yielding	Bin A
Experiment	Wafer 4	23.02	Yielding	Bin B
Experiment	Wafer 5	22.89	Yielding	Bin A
Experiment	Wafer 6	22.81	Yielding	Bin A
Experiment	Wafer 7	22.95	Yielding	Bin B
Experiment	Wafer 8	22.91	Yielding	Bin D
Experiment	Wafer 9	22.93	Yielding	Bin A
Experiment	Wafer 10	23.05	Yielding	Bin B
Experiment	Wafer 11	23.06	Yielding	Bin A
Experiment	Wafer 12	23.14	Yielding	Bin A
Experiment	Wafer 13	22.97	Yielding	Bin A
Experiment	Wafer 14	23.04	Yielding	Bin A
Experiment	Wafer 15	23.07	Yielding	Bin B
Experiment	Wafer 16	23.02	Yielding	Bin A
Experiment	Wafer 17	23.14	Yielding	Bin B
Experiment	Wafer 18	23.09	Yielding	Bin B
Experiment	Wafer 19	22.99	Yielding	Bin B
Experiment	Wafer 20	23.12	Yielding	Bin B
Experiment	Wafer 21	23.09	Yielding	Bin B
Experiment	Wafer 22	23.05	Yielding	Bin B
Experiment	Wafer 23	23.05	Yielding	Bin B
Experiment	Wafer 24	23.10	Yielding	Bin B
Experiment	Wafer 25	23.05	Yielding	Bin B
Experiment	Wafer 26	22.89	Yielding	Bin B
Experiment	Wafer 27	23.06	Yielding	Bin B
Experiment	Wafer 28	23.09	Yielding	Bin B
Experiment	Wafer 29	23.01	Yielding	Bin B
Experiment	Wafer 30	23.00	Yielding	Bin B
Experiment	Wafer 31	21.95	Non-yielding	Bin B
Experiment	Wafer 32	23.04	Yielding	Bin B
Experiment	Wafer 33	23.11	Yielding	Bin B
Experiment	Wafer 34	23.09	Yielding	Bin A
Experiment	Wafer 35	23.16	Yielding	Bin B
Experiment	Wafer 36	22.87	Yielding	Bin B
Experiment	Wafer 37	22.83	Yielding	Bin B
Experiment	Wafer 38	23.00	Yielding	Bin B
Experiment	Wafer 39	23.10	Yielding	Bin A

Experiment	Wafer 40	23.03	Yielding	Bin B
Experiment	Wafer 41	22.88	Yielding	Bin B
Experiment	Wafer 42	23.21	Yielding	Bin D
Experiment	Wafer 43	23.11	Yielding	Bin A
Experiment	Wafer 44	23.13	Yielding	Bin B
Experiment	Wafer 45	23.04	Yielding	Bin B
Experiment	Wafer 46	23.13	Yielding	Bin A
Experiment	Wafer 47	23.01	Yielding	Bin B
Experiment	Wafer 48	23.04	Yielding	Bin A
Experiment	Wafer 49	23.02	Yielding	Bin B
Experiment	Wafer 50	23.07	Yielding	Bin C
Experiment	Wafer 51	22.89	Yielding	Bin B
Experiment	Wafer 52	22.64	Yielding	Bin A
Experiment	Wafer 53	22.85	Yielding	Bin B
Experiment	Wafer 54	23.06	Yielding	Bin A
Experiment	Wafer 55	23.02	Yielding	Bin B
Experiment	Wafer 56	23.04	Yielding	Bin B
Experiment	Wafer 57	22.98	Yielding	Bin A
Experiment	Wafer 58	22.95	Yielding	Bin B
Experiment	Wafer 59	22.90	Yielding	Bin C
Experiment	Wafer 60	22.84	Yielding	Bin B
Experiment	Wafer 61	23.10	Yielding	Bin A
Experiment	Wafer 62	22.89	Yielding	Bin B
Experiment	Wafer 63	23.13	Yielding	Bin A
Experiment	Wafer 64	23.16	Yielding	Bin B
Experiment	Wafer 65	22.79	Yielding	Bin C
Experiment	Wafer 66	22.99	Yielding	Bin B
Experiment	Wafer 67	22.90	Yielding	Bin B
Experiment	Wafer 68	22.75	Yielding	Bin C
Experiment	Wafer 69	22.81	Yielding	Bin B
Experiment	Wafer 70	22.94	Yielding	Bin C
Experiment	Wafer 71	22.95	Yielding	Bin B
Experiment	Wafer 72	23.15	Yielding	Bin C
Experiment	Wafer 73	23.09	Yielding	Bin B
Experiment	Wafer 74	23.10	Yielding	Bin B
Experiment	Wafer 75	22.99	Yielding	Bin B
Experiment	Wafer 76	23.12	Yielding	Bin B
Experiment	Wafer 77	22.03	Non-yielding	Bin C
Experiment	Wafer 78	22.96	Yielding	Bin B
Experiment	Wafer 79	23.04	Yielding	Bin B
Experiment	Wafer 80	23.01	Yielding	Bin B
Experiment	Wafer 81	23.03	Yielding	Bin B
Experiment	Wafer 82	22.91	Yielding	Bin B
Experiment	Wafer 83	23.11	Yielding	Bin C

Experiment	Wafer 84	23.08	Yielding	Bin B
Experiment	Wafer 85	23.14	Yielding	Bin B
Experiment	Wafer 86	22.82	Yielding	Bin B
Experiment	Wafer 87	23.12	Yielding	Bin C
Experiment	Wafer 88	22.86	Yielding	Bin B
Experiment	Wafer 89	22.89	Yielding	Bin B
Experiment	Wafer 90	23.07	Yielding	Bin C
Experiment	Wafer 91	23.15	Yielding	Bin B
Experiment	Wafer 92	22.94	Yielding	Bin B
Experiment	Wafer 93	22.99	Yielding	Bin B
Experiment	Wafer 94	23.03	Yielding	Bin B
Experiment	Wafer 95	23.05	Yielding	Bin C
Experiment	Wafer 96	22.83	Yielding	Bin B
Experiment	Wafer 97	22.78	Yielding	Bin B
Experiment	Wafer 98	22.81	Yielding	Bin B
Experiment	Wafer 99	22.82	Yielding	Bin B
Experiment	Wafer 100	22.79	Yielding	Bin B
Control	Wafer 1	22.84	Yielding	Bin A
Control	Wafer 2	23.27	Yielding	Bin A
Control	Wafer 3	22.94	Yielding	Bin A
Control	Wafer 4	23.12	Yielding	Bin A
Control	Wafer 5	23.26	Yielding	Bin D
Control	Wafer 6	22.99	Yielding	Bin C
Control	Wafer 7	22.81	Yielding	Bin B
Control	Wafer 8	23.29	Yielding	Bin B
Control	Wafer 9	23.18	Yielding	Bin C
Control	Wafer 10	23.13	Yielding	Bin B
Control	Wafer 11	22.79	Yielding	Bin B
Control	Wafer 12	22.48	Yielding	Bin A
Control	Wafer 13	22.59	Yielding	Bin A
Control	Wafer 14	22.67	Yielding	Bin B
Control	Wafer 15	22.65	Yielding	Bin B
Control	Wafer 16	22.80	Yielding	Bin C
Control	Wafer 17	22.86	Yielding	Bin B
Control	Wafer 18	22.80	Yielding	Bin B
Control	Wafer 19	22.63	Yielding	Bin B
Control	Wafer 20	22.80	Yielding	Bin C
Control	Wafer 21	22.83	Yielding	Bin A
Control	Wafer 22	22.54	Yielding	Bin A
Control	Wafer 23	22.79	Yielding	Bin A
Control	Wafer 24	22.81	Yielding	Bin B
Control	Wafer 25	22.76	Yielding	Bin B
Control	Wafer 26	22.79	Yielding	Bin B
Control	Wafer 27	22.57	Yielding	Bin A

Control	Wafer 28	23.04	Yielding	Bin B
Control	Wafer 29	22.78	Yielding	Bin B
Control	Wafer 30	22.56	Yielding	Bin B
Control	Wafer 31	22.64	Yielding	Bin B
Control	Wafer 32	22.55	Yielding	Bin B
Control	Wafer 33	22.70	Yielding	Bin B
Control	Wafer 34	22.68	Yielding	Bin D
Control	Wafer 35	22.60	Yielding	Bin B
Control	Wafer 36	22.68	Yielding	Bin B
Control	Wafer 37	22.60	Yielding	Bin B
Control	Wafer 38	22.82	Yielding	Bin B
Control	Wafer 39	22.69	Yielding	Bin B
Control	Wafer 40	22.19	Non-yielding	Bin B
Control	Wafer 41	22.55	Yielding	Bin B
Control	Wafer 42	22.73	Yielding	Bin B
Control	Wafer 43	23.03	Yielding	Bin B
Control	Wafer 44	22.89	Yielding	Bin C
Control	Wafer 45	22.76	Yielding	Bin B
Control	Wafer 46	22.86	Yielding	Bin B
Control	Wafer 47	22.73	Yielding	Bin B
Control	Wafer 48	22.70	Yielding	Bin C
Control	Wafer 49	22.60	Yielding	Bin D
Control	Wafer 50	22.69	Yielding	Bin B
Control	Wafer 51	22.88	Yielding	Bin B
Control	Wafer 52	22.82	Yielding	Bin C
Control	Wafer 53	22.89	Yielding	Bin B
Control	Wafer 54	22.75	Yielding	Bin B
Control	Wafer 55	23.08	Yielding	Bin B
Control	Wafer 56	23.02	Yielding	Bin C
Control	Wafer 57	22.75	Yielding	Bin B
Control	Wafer 58	22.58	Yielding	Bin B
Control	Wafer 59	22.87	Yielding	Bin B
Control	Wafer 60	22.61	Yielding	Bin C
Control	Wafer 61	23.01	Yielding	Bin A
Control	Wafer 62	22.90	Yielding	Bin B
Control	Wafer 63	22.83	Yielding	Bin A
Control	Wafer 64	22.82	Yielding	Bin B
Control	Wafer 65	22.76	Yielding	Bin C
Control	Wafer 66	22.73	Yielding	Bin B
Control	Wafer 67	23.03	Yielding	Bin A
Control	Wafer 68	22.92	Yielding	Bin B
Control	Wafer 69	23.09	Yielding	Bin A
Control	Wafer 70	23.22	Yielding	Bin B
Control	Wafer 71	22.87	Yielding	Bin B

Control	Wafer 72	22.73	Yielding	Bin B
Control	Wafer 73	21.45	Non-yielding	Bin C
Control	Wafer 74	22.71	Yielding	Bin B
Control	Wafer 75	22.54	Yielding	Bin A
Control	Wafer 76	22.85	Yielding	Bin B
Control	Wafer 77	22.88	Yielding	Bin B
Control	Wafer 78	19.16	Non-yielding	Bin D
Control	Wafer 79	22.78	Yielding	Bin B
Control	Wafer 80	22.75	Yielding	Bin B
Control	Wafer 81	23.09	Yielding	Bin B
Control	Wafer 82	22.77	Yielding	Bin A
Control	Wafer 83	23.11	Yielding	Bin B
Control	Wafer 84	23.02	Yielding	Bin B
Control	Wafer 85	23.11	Yielding	Bin A
Control	Wafer 86	23.13	Yielding	Bin A
Control	Wafer 87	23.23	Yielding	Bin B
Control	Wafer 88	23.16	Yielding	Bin B
Control	Wafer 89	23.10	Yielding	Bin A
Control	Wafer 90	23.18	Yielding	Bin B
Control	Wafer 91	22.95	Yielding	Bin B
Control	Wafer 92	23.17	Yielding	Bin B
Control	Wafer 93	23.07	Yielding	Bin B
Control	Wafer 94	23.10	Yielding	Bin B
Control	Wafer 95	22.91	Yielding	Bin A
Control	Wafer 96	23.13	Yielding	Bin B
Control	Wafer 97	23.19	Yielding	Bin B
Control	Wafer 98	23.19	Yielding	Bin B
Control	Wafer 99	23.05	Yielding	Bin B
Control	Wafer 100	22.91	Yielding	Bin B

APPENDIX D : Table of Result for Experimental Run (Quantity : 1000pieces)

Split	Wafer Number	Efficiency	Electrical Yield	Cosmetic Yield
Experiment	Wafer 1	23.05	Yielding	Bin A
Experiment	Wafer 2	22.94	Yielding	Bin A
Experiment	Wafer 3	22.97	Yielding	Bin A
Experiment	Wafer 4	22.97	Yielding	Bin A
Experiment	Wafer 5	22.99	Yielding	Bin A
Experiment	Wafer 6	22.77	Yielding	Bin A
Experiment	Wafer 7	22.86	Yielding	Bin A
Experiment	Wafer 8	22.95	Yielding	Bin A
Experiment	Wafer 9	22.96	Yielding	Bin A
Experiment	Wafer 10	22.83	Yielding	Bin A
Experiment	Wafer 11	23.08	Yielding	Bin A
Experiment	Wafer 12	23.06	Yielding	Bin A
Experiment	Wafer 13	23.02	Yielding	Bin A
Experiment	Wafer 14	22.94	Yielding	Bin A
Experiment	Wafer 15	23.07	Yielding	Bin A
Experiment	Wafer 16	22.94	Yielding	Bin A
Experiment	Wafer 17	22.79	Yielding	Bin A
Experiment	Wafer 18	22.94	Yielding	Bin A
Experiment	Wafer 19	23.03	Yielding	Bin A
Experiment	Wafer 20	22.99	Yielding	Bin A
Experiment	Wafer 21	23.01	Yielding	Bin A
Experiment	Wafer 22	23.06	Yielding	Bin A
Experiment	Wafer 23	23.00	Yielding	Bin A
Experiment	Wafer 24	23.09	Yielding	Bin A
Experiment	Wafer 25	22.16	Non-yielding	Bin A
Experiment	Wafer 26	23.01	Yielding	Bin A
Experiment	Wafer 27	22.94	Yielding	Bin A
Experiment	Wafer 28	22.98	Yielding	Bin A
Experiment	Wafer 29	22.94	Yielding	Bin A
Experiment	Wafer 30	22.99	Yielding	Bin A
Experiment	Wafer 31	22.97	Yielding	Bin A
Experiment	Wafer 32	22.95	Yielding	Bin A
Experiment	Wafer 33	23.01	Yielding	Bin A
Experiment	Wafer 34	22.93	Yielding	Bin A
Experiment	Wafer 35	22.41	Yielding	Bin A
Experiment	Wafer 36	22.85	Yielding	Bin A
Experiment	Wafer 37	22.85	Yielding	Bin A
Experiment	Wafer 38	22.98	Yielding	Bin A
Experiment	Wafer 39	22.90	Yielding	Bin A
Experiment	Wafer 40	23.05	Yielding	Bin A

Experiment	Wafer 41	23.12	Yielding	Bin A
Experiment	Wafer 42	22.89	Yielding	Bin A
Experiment	Wafer 43	22.89	Yielding	Bin A
Experiment	Wafer 44	21.95	Non-yielding	Bin A
Experiment	Wafer 45	22.94	Yielding	Bin A
Experiment	Wafer 46	22.11	Non-yielding	Bin A
Experiment	Wafer 47	22.99	Yielding	Bin A
Experiment	Wafer 48	22.95	Yielding	Bin A
Experiment	Wafer 49	22.93	Yielding	Bin A
Experiment	Wafer 50	22.98	Yielding	Bin A
Experiment	Wafer 51	22.81	Yielding	Bin A
Experiment	Wafer 52	22.83	Yielding	Bin A
Experiment	Wafer 53	22.82	Yielding	Bin A
Experiment	Wafer 54	22.78	Yielding	Bin A
Experiment	Wafer 55	23.09	Yielding	Bin A
Experiment	Wafer 56	22.98	Yielding	Bin A
Experiment	Wafer 57	22.88	Yielding	Bin A
Experiment	Wafer 58	22.79	Yielding	Bin A
Experiment	Wafer 59	22.77	Yielding	Bin A
Experiment	Wafer 60	22.83	Yielding	Bin A
Experiment	Wafer 61	22.97	Yielding	Bin A
Experiment	Wafer 62	22.63	Yielding	Bin A
Experiment	Wafer 63	23.04	Yielding	Bin A
Experiment	Wafer 64	22.94	Yielding	Bin A
Experiment	Wafer 65	22.97	Yielding	Bin A
Experiment	Wafer 66	22.95	Yielding	Bin A
Experiment	Wafer 67	23.13	Yielding	Bin A
Experiment	Wafer 68	22.75	Yielding	Bin A
Experiment	Wafer 69	22.60	Yielding	Bin A
Experiment	Wafer 70	22.93	Yielding	Bin A
Experiment	Wafer 71	22.80	Yielding	Bin A
Experiment	Wafer 72	23.00	Yielding	Bin A
Experiment	Wafer 73	23.07	Yielding	Bin A
Experiment	Wafer 74	22.63	Yielding	Bin A
Experiment	Wafer 75	22.95	Yielding	Bin A
Experiment	Wafer 76	23.01	Yielding	Bin A
Experiment	Wafer 77	23.05	Yielding	Bin A
Experiment	Wafer 78	22.62	Yielding	Bin A
Experiment	Wafer 79	22.95	Yielding	Bin A
Experiment	Wafer 80	22.94	Yielding	Bin A
Experiment	Wafer 81	22.87	Yielding	Bin A
Experiment	Wafer 82	22.79	Yielding	Bin A
Experiment	Wafer 83	22.91	Yielding	Bin A
Experiment	Wafer 84	22.79	Yielding	Bin A

Experiment	Wafer 85	22.87	Yielding	Bin A
Experiment	Wafer 86	22.94	Yielding	Bin A
Experiment	Wafer 87	22.93	Yielding	Bin A
Experiment	Wafer 88	22.84	Yielding	Bin A
Experiment	Wafer 89	22.82	Yielding	Bin A
Experiment	Wafer 90	22.83	Yielding	Bin A
Experiment	Wafer 91	22.90	Yielding	Bin A
Experiment	Wafer 92	22.91	Yielding	Bin A
Experiment	Wafer 93	22.92	Yielding	Bin A
Experiment	Wafer 94	22.87	Yielding	Bin A
Experiment	Wafer 95	22.75	Yielding	Bin A
Experiment	Wafer 96	22.96	Yielding	Bin A
Experiment	Wafer 97	22.95	Yielding	Bin A
Experiment	Wafer 98	22.91	Yielding	Bin A
Experiment	Wafer 99	22.86	Yielding	Bin A
Experiment	Wafer 100	23.05	Yielding	Bin A
Experiment	Wafer 101	22.97	Yielding	Bin A
Experiment	Wafer 102	22.95	Yielding	Bin A
Experiment	Wafer 103	22.96	Yielding	Bin A
Experiment	Wafer 104	22.99	Yielding	Bin A
Experiment	Wafer 105	22.82	Yielding	Bin A
Experiment	Wafer 106	23.05	Yielding	Bin A
Experiment	Wafer 107	22.94	Yielding	Bin A
Experiment	Wafer 108	23.07	Yielding	Bin A
Experiment	Wafer 109	23.02	Yielding	Bin A
Experiment	Wafer 110	23.04	Yielding	Bin A
Experiment	Wafer 111	23.09	Yielding	Bin A
Experiment	Wafer 112	23.00	Yielding	Bin A
Experiment	Wafer 113	22.99	Yielding	Bin A
Experiment	Wafer 114	22.96	Yielding	Bin A
Experiment	Wafer 115	23.08	Yielding	Bin A
Experiment	Wafer 116	23.09	Yielding	Bin A
Experiment	Wafer 117	23.02	Yielding	Bin A
Experiment	Wafer 118	22.97	Yielding	Bin A
Experiment	Wafer 119	22.73	Yielding	Bin A
Experiment	Wafer 120	22.73	Yielding	Bin A
Experiment	Wafer 121	22.93	Yielding	Bin A
Experiment	Wafer 122	23.04	Yielding	Bin A
Experiment	Wafer 123	22.97	Yielding	Bin A
Experiment	Wafer 124	22.96	Yielding	Bin A
Experiment	Wafer 125	22.85	Yielding	Bin A
Experiment	Wafer 126	23.14	Yielding	Bin A
Experiment	Wafer 127	23.00	Yielding	Bin A
Experiment	Wafer 128	22.95	Yielding	Bin A

Experiment	Wafer 129	22.80	Yielding	Bin A
Experiment	Wafer 130	22.93	Yielding	Bin A
Experiment	Wafer 131	22.79	Yielding	Bin A
Experiment	Wafer 132	23.00	Yielding	Bin A
Experiment	Wafer 133	23.00	Yielding	Bin A
Experiment	Wafer 134	23.01	Yielding	Bin A
Experiment	Wafer 135	23.20	Yielding	Bin A
Experiment	Wafer 136	22.87	Yielding	Bin A
Experiment	Wafer 137	23.06	Yielding	Bin A
Experiment	Wafer 138	23.14	Yielding	Bin A
Experiment	Wafer 139	23.05	Yielding	Bin A
Experiment	Wafer 140	22.98	Yielding	Bin A
Experiment	Wafer 141	23.07	Yielding	Bin A
Experiment	Wafer 142	22.98	Yielding	Bin A
Experiment	Wafer 143	23.04	Yielding	Bin A
Experiment	Wafer 144	23.30	Yielding	Bin A
Experiment	Wafer 145	22.86	Yielding	Bin A
Experiment	Wafer 146	23.08	Yielding	Bin A
Experiment	Wafer 147	23.05	Yielding	Bin A
Experiment	Wafer 148	23.07	Yielding	Bin A
Experiment	Wafer 149	22.97	Yielding	Bin A
Experiment	Wafer 150	23.01	Yielding	Bin A
Experiment	Wafer 151	22.82	Yielding	Bin A
Experiment	Wafer 152	22.83	Yielding	Bin A
Experiment	Wafer 153	22.70	Yielding	Bin A
Experiment	Wafer 154	22.95	Yielding	Bin A
Experiment	Wafer 155	22.99	Yielding	Bin A
Experiment	Wafer 156	22.87	Yielding	Bin A
Experiment	Wafer 157	22.93	Yielding	Bin A
Experiment	Wafer 158	22.74	Yielding	Bin A
Experiment	Wafer 159	22.99	Yielding	Bin A
Experiment	Wafer 160	23.07	Yielding	Bin A
Experiment	Wafer 161	23.00	Yielding	Bin A
Experiment	Wafer 162	23.09	Yielding	Bin A
Experiment	Wafer 163	23.05	Yielding	Bin A
Experiment	Wafer 164	22.99	Yielding	Bin A
Experiment	Wafer 165	23.01	Yielding	Bin A
Experiment	Wafer 166	23.05	Yielding	Bin A
Experiment	Wafer 167	23.12	Yielding	Bin A
Experiment	Wafer 168	23.14	Yielding	Bin A
Experiment	Wafer 169	23.14	Yielding	Bin A
Experiment	Wafer 170	22.91	Yielding	Bin A
Experiment	Wafer 171	22.60	Yielding	Bin A
Experiment	Wafer 172	22.86	Yielding	Bin A

Experiment	Wafer 173	22.92	Yielding	Bin A
Experiment	Wafer 174	22.89	Yielding	Bin A
Experiment	Wafer 175	22.84	Yielding	Bin A
Experiment	Wafer 176	22.88	Yielding	Bin A
Experiment	Wafer 177	23.01	Yielding	Bin A
Experiment	Wafer 178	22.85	Yielding	Bin A
Experiment	Wafer 179	22.92	Yielding	Bin A
Experiment	Wafer 180	22.80	Yielding	Bin A
Experiment	Wafer 181	22.82	Yielding	Bin A
Experiment	Wafer 182	22.54	Yielding	Bin A
Experiment	Wafer 183	22.91	Yielding	Bin A
Experiment	Wafer 184	23.11	Yielding	Bin A
Experiment	Wafer 185	22.94	Yielding	Bin A
Experiment	Wafer 186	22.85	Yielding	Bin A
Experiment	Wafer 187	22.95	Yielding	Bin A
Experiment	Wafer 188	23.01	Yielding	Bin A
Experiment	Wafer 189	22.87	Yielding	Bin A
Experiment	Wafer 190	22.96	Yielding	Bin A
Experiment	Wafer 191	22.96	Yielding	Bin A
Experiment	Wafer 192	23.12	Yielding	Bin A
Experiment	Wafer 193	22.62	Yielding	Bin A
Experiment	Wafer 194	22.95	Yielding	Bin A
Experiment	Wafer 195	23.05	Yielding	Bin A
Experiment	Wafer 196	22.96	Yielding	Bin A
Experiment	Wafer 197	22.91	Yielding	Bin A
Experiment	Wafer 198	23.01	Yielding	Bin A
Experiment	Wafer 199	23.05	Yielding	Bin A
Experiment	Wafer 200	23.02	Yielding	Bin A
Experiment	Wafer 201	22.89	Yielding	Bin A
Experiment	Wafer 202	22.77	Yielding	Bin A
Experiment	Wafer 203	22.85	Yielding	Bin A
Experiment	Wafer 204	23.11	Yielding	Bin A
Experiment	Wafer 205	22.98	Yielding	Bin A
Experiment	Wafer 206	23.08	Yielding	Bin A
Experiment	Wafer 207	23.01	Yielding	Bin A
Experiment	Wafer 208	22.77	Yielding	Bin A
Experiment	Wafer 209	23.01	Yielding	Bin A
Experiment	Wafer 210	22.79	Yielding	Bin A
Experiment	Wafer 211	22.95	Yielding	Bin A
Experiment	Wafer 212	22.97	Yielding	Bin A
Experiment	Wafer 213	23.00	Yielding	Bin A
Experiment	Wafer 214	22.93	Yielding	Bin A
Experiment	Wafer 215	22.82	Yielding	Bin A
Experiment	Wafer 216	23.03	Yielding	Bin A

Experiment	Wafer 217	22.82	Yielding	Bin A
Experiment	Wafer 218	22.90	Yielding	Bin A
Experiment	Wafer 219	22.87	Yielding	Bin A
Experiment	Wafer 220	22.72	Yielding	Bin A
Experiment	Wafer 221	22.93	Yielding	Bin A
Experiment	Wafer 222	22.80	Yielding	Bin A
Experiment	Wafer 223	22.83	Yielding	Bin A
Experiment	Wafer 224	22.92	Yielding	Bin A
Experiment	Wafer 225	23.02	Yielding	Bin A
Experiment	Wafer 226	22.91	Yielding	Bin A
Experiment	Wafer 227	22.91	Yielding	Bin A
Experiment	Wafer 228	23.02	Yielding	Bin A
Experiment	Wafer 229	23.02	Yielding	Bin A
Experiment	Wafer 230	22.89	Yielding	Bin A
Experiment	Wafer 231	22.93	Yielding	Bin A
Experiment	Wafer 232	22.90	Yielding	Bin A
Experiment	Wafer 233	22.94	Yielding	Bin A
Experiment	Wafer 234	23.12	Yielding	Bin A
Experiment	Wafer 235	22.85	Yielding	Bin A
Experiment	Wafer 236	23.17	Yielding	Bin A
Experiment	Wafer 237	23.03	Yielding	Bin A
Experiment	Wafer 238	23.07	Yielding	Bin A
Experiment	Wafer 239	22.96	Yielding	Bin A
Experiment	Wafer 240	23.04	Yielding	Bin A
Experiment	Wafer 241	22.85	Yielding	Bin A
Experiment	Wafer 242	22.89	Yielding	Bin A
Experiment	Wafer 243	22.80	Yielding	Bin A
Experiment	Wafer 244	23.07	Yielding	Bin A
Experiment	Wafer 245	23.02	Yielding	Bin A
Experiment	Wafer 246	23.02	Yielding	Bin A
Experiment	Wafer 247	22.84	Yielding	Bin A
Experiment	Wafer 248	23.00	Yielding	Bin A
Experiment	Wafer 249	23.01	Yielding	Bin A
Experiment	Wafer 250	23.01	Yielding	Bin A
Experiment	Wafer 251	22.93	Yielding	Bin A
Experiment	Wafer 252	22.60	Yielding	Bin A
Experiment	Wafer 253	23.11	Yielding	Bin A
Experiment	Wafer 254	22.98	Yielding	Bin A
Experiment	Wafer 255	22.94	Yielding	Bin A
Experiment	Wafer 256	22.89	Yielding	Bin A
Experiment	Wafer 257	22.87	Yielding	Bin A
Experiment	Wafer 258	22.97	Yielding	Bin A
Experiment	Wafer 259	22.94	Yielding	Bin A
Experiment	Wafer 260	23.14	Yielding	Bin A

Experiment	Wafer 261	23.01	Yielding	Bin A
Experiment	Wafer 262	23.07	Yielding	Bin A
Experiment	Wafer 263	22.94	Yielding	Bin A
Experiment	Wafer 264	23.03	Yielding	Bin A
Experiment	Wafer 265	22.94	Yielding	Bin A
Experiment	Wafer 266	23.02	Yielding	Bin A
Experiment	Wafer 267	22.95	Yielding	Bin A
Experiment	Wafer 268	22.88	Yielding	Bin A
Experiment	Wafer 269	22.92	Yielding	Bin A
Experiment	Wafer 270	22.67	Yielding	Bin A
Experiment	Wafer 271	22.84	Yielding	Bin A
Experiment	Wafer 272	22.81	Yielding	Bin A
Experiment	Wafer 273	23.03	Yielding	Bin A
Experiment	Wafer 274	23.02	Yielding	Bin A
Experiment	Wafer 275	22.99	Yielding	Bin A
Experiment	Wafer 276	23.02	Yielding	Bin A
Experiment	Wafer 277	22.82	Yielding	Bin A
Experiment	Wafer 278	23.09	Yielding	Bin A
Experiment	Wafer 279	22.80	Yielding	Bin A
Experiment	Wafer 280	23.00	Yielding	Bin A
Experiment	Wafer 281	23.19	Yielding	Bin A
Experiment	Wafer 282	23.01	Yielding	Bin A
Experiment	Wafer 283	22.91	Yielding	Bin A
Experiment	Wafer 284	23.08	Yielding	Bin A
Experiment	Wafer 285	22.94	Yielding	Bin A
Experiment	Wafer 286	22.98	Yielding	Bin A
Experiment	Wafer 287	23.02	Yielding	Bin A
Experiment	Wafer 288	23.00	Yielding	Bin A
Experiment	Wafer 289	23.09	Yielding	Bin A
Experiment	Wafer 290	22.90	Yielding	Bin A
Experiment	Wafer 291	23.00	Yielding	Bin A
Experiment	Wafer 292	23.13	Yielding	Bin A
Experiment	Wafer 293	22.94	Yielding	Bin A
Experiment	Wafer 294	22.65	Yielding	Bin A
Experiment	Wafer 295	23.13	Yielding	Bin A
Experiment	Wafer 296	22.81	Yielding	Bin A
Experiment	Wafer 297	22.87	Yielding	Bin A
Experiment	Wafer 298	22.98	Yielding	Bin A
Experiment	Wafer 299	22.72	Yielding	Bin A
Experiment	Wafer 300	22.91	Yielding	Bin A
Experiment	Wafer 301	22.99	Yielding	Bin A
Experiment	Wafer 302	22.74	Yielding	Bin A
Experiment	Wafer 303	22.72	Yielding	Bin A
Experiment	Wafer 304	23.00	Yielding	Bin A

Experiment	Wafer 305	22.88	Yielding	Bin A
Experiment	Wafer 306	22.89	Yielding	Bin A
Experiment	Wafer 307	22.77	Yielding	Bin A
Experiment	Wafer 308	23.09	Yielding	Bin A
Experiment	Wafer 309	23.05	Yielding	Bin A
Experiment	Wafer 310	23.07	Yielding	Bin A
Experiment	Wafer 311	22.99	Yielding	Bin A
Experiment	Wafer 312	22.88	Yielding	Bin A
Experiment	Wafer 313	23.08	Yielding	Bin A
Experiment	Wafer 314	22.90	Yielding	Bin A
Experiment	Wafer 315	22.90	Yielding	Bin A
Experiment	Wafer 316	22.88	Yielding	Bin A
Experiment	Wafer 317	22.83	Yielding	Bin A
Experiment	Wafer 318	22.85	Yielding	Bin A
Experiment	Wafer 319	22.87	Yielding	Bin A
Experiment	Wafer 320	22.83	Yielding	Bin A
Experiment	Wafer 321	22.96	Yielding	Bin A
Experiment	Wafer 322	23.16	Yielding	Bin A
Experiment	Wafer 323	22.98	Yielding	Bin A
Experiment	Wafer 324	23.04	Yielding	Bin A
Experiment	Wafer 325	22.97	Yielding	Bin A
Experiment	Wafer 326	23.00	Yielding	Bin A
Experiment	Wafer 327	23.03	Yielding	Bin A
Experiment	Wafer 328	22.94	Yielding	Bin A
Experiment	Wafer 329	22.07	Non-yielding	Bin A
Experiment	Wafer 330	22.95	Yielding	Bin A
Experiment	Wafer 331	23.03	Yielding	Bin A
Experiment	Wafer 332	22.98	Yielding	Bin A
Experiment	Wafer 333	22.98	Yielding	Bin A
Experiment	Wafer 334	22.89	Yielding	Bin A
Experiment	Wafer 335	22.82	Yielding	Bin A
Experiment	Wafer 336	22.93	Yielding	Bin A
Experiment	Wafer 337	22.77	Yielding	Bin A
Experiment	Wafer 338	22.78	Yielding	Bin A
Experiment	Wafer 339	22.88	Yielding	Bin A
Experiment	Wafer 340	23.06	Yielding	Bin A
Experiment	Wafer 341	22.98	Yielding	Bin A
Experiment	Wafer 342	22.88	Yielding	Bin A
Experiment	Wafer 343	22.87	Yielding	Bin A
Experiment	Wafer 344	23.09	Yielding	Bin A
Experiment	Wafer 345	23.10	Yielding	Bin A
Experiment	Wafer 346	22.88	Yielding	Bin A
Experiment	Wafer 347	22.99	Yielding	Bin A
Experiment	Wafer 348	22.92	Yielding	Bin A

Experiment	Wafer 349	23.04	Yielding	Bin A
Experiment	Wafer 350	22.56	Yielding	Bin A
Experiment	Wafer 351	23.04	Yielding	Bin A
Experiment	Wafer 352	22.80	Yielding	Bin A
Experiment	Wafer 353	22.88	Yielding	Bin A
Experiment	Wafer 354	22.92	Yielding	Bin A
Experiment	Wafer 355	22.90	Yielding	Bin A
Experiment	Wafer 356	22.98	Yielding	Bin A
Experiment	Wafer 357	22.95	Yielding	Bin A
Experiment	Wafer 358	22.96	Yielding	Bin A
Experiment	Wafer 359	22.67	Yielding	Bin A
Experiment	Wafer 360	22.98	Yielding	Bin A
Experiment	Wafer 361	23.20	Yielding	Bin A
Experiment	Wafer 362	22.81	Yielding	Bin A
Experiment	Wafer 363	23.10	Yielding	Bin A
Experiment	Wafer 364	22.77	Yielding	Bin A
Experiment	Wafer 365	23.00	Yielding	Bin A
Experiment	Wafer 366	22.75	Yielding	Bin A
Experiment	Wafer 367	23.10	Yielding	Bin A
Experiment	Wafer 368	23.00	Yielding	Bin A
Experiment	Wafer 369	22.96	Yielding	Bin A
Experiment	Wafer 370	22.92	Yielding	Bin A
Experiment	Wafer 371	22.99	Yielding	Bin A
Experiment	Wafer 372	23.02	Yielding	Bin A
Experiment	Wafer 373	23.04	Yielding	Bin A
Experiment	Wafer 374	22.99	Yielding	Bin A
Experiment	Wafer 375	22.93	Yielding	Bin A
Experiment	Wafer 376	22.99	Yielding	Bin A
Experiment	Wafer 377	23.10	Yielding	Bin A
Experiment	Wafer 378	22.96	Yielding	Bin A
Experiment	Wafer 379	23.00	Yielding	Bin A
Experiment	Wafer 380	22.84	Yielding	Bin A
Experiment	Wafer 381	22.91	Yielding	Bin A
Experiment	Wafer 382	22.74	Yielding	Bin A
Experiment	Wafer 383	23.10	Yielding	Bin A
Experiment	Wafer 384	22.95	Yielding	Bin A
Experiment	Wafer 385	22.92	Yielding	Bin A
Experiment	Wafer 386	22.92	Yielding	Bin A
Experiment	Wafer 387	22.93	Yielding	Bin A
Experiment	Wafer 388	23.05	Yielding	Bin A
Experiment	Wafer 389	22.88	Yielding	Bin A
Experiment	Wafer 390	23.08	Yielding	Bin A
Experiment	Wafer 391	22.90	Yielding	Bin A
Experiment	Wafer 392	22.96	Yielding	Bin A

Experiment	Wafer 393	23.08	Yielding	Bin A
Experiment	Wafer 394	22.69	Yielding	Bin A
Experiment	Wafer 395	22.94	Yielding	Bin A
Experiment	Wafer 396	23.06	Yielding	Bin A
Experiment	Wafer 397	22.89	Yielding	Bin A
Experiment	Wafer 398	22.89	Yielding	Bin A
Experiment	Wafer 399	22.96	Yielding	Bin A
Experiment	Wafer 400	23.07	Yielding	Bin A
Experiment	Wafer 401	22.92	Yielding	Bin A
Experiment	Wafer 402	22.98	Yielding	Bin A
Experiment	Wafer 403	22.95	Yielding	Bin A
Experiment	Wafer 404	23.07	Yielding	Bin A
Experiment	Wafer 405	22.69	Yielding	Bin A
Experiment	Wafer 406	23.07	Yielding	Bin A
Experiment	Wafer 407	23.10	Yielding	Bin A
Experiment	Wafer 408	23.02	Yielding	Bin A
Experiment	Wafer 409	23.08	Yielding	Bin A
Experiment	Wafer 410	23.09	Yielding	Bin A
Experiment	Wafer 411	22.98	Yielding	Bin A
Experiment	Wafer 412	22.99	Yielding	Bin A
Experiment	Wafer 413	23.03	Yielding	Bin A
Experiment	Wafer 414	23.02	Yielding	Bin A
Experiment	Wafer 415	23.05	Yielding	Bin A
Experiment	Wafer 416	22.95	Yielding	Bin A
Experiment	Wafer 417	22.90	Yielding	Bin A
Experiment	Wafer 418	23.26	Yielding	Bin A
Experiment	Wafer 419	22.92	Yielding	Bin A
Experiment	Wafer 420	22.96	Yielding	Bin A
Experiment	Wafer 421	23.03	Yielding	Bin A
Experiment	Wafer 422	23.12	Yielding	Bin A
Experiment	Wafer 423	23.06	Yielding	Bin A
Experiment	Wafer 424	22.96	Yielding	Bin A
Experiment	Wafer 425	23.00	Yielding	Bin A
Experiment	Wafer 426	23.19	Yielding	Bin A
Experiment	Wafer 427	23.12	Yielding	Bin A
Experiment	Wafer 428	23.10	Yielding	Bin A
Experiment	Wafer 429	23.05	Yielding	Bin A
Experiment	Wafer 430	23.15	Yielding	Bin A
Experiment	Wafer 431	22.98	Yielding	Bin A
Experiment	Wafer 432	22.99	Yielding	Bin A
Experiment	Wafer 433	23.14	Yielding	Bin A
Experiment	Wafer 434	22.75	Yielding	Bin A
Experiment	Wafer 435	23.07	Yielding	Bin A
Experiment	Wafer 436	23.09	Yielding	Bin A

Experiment	Wafer 437	22.87	Yielding	Bin A
Experiment	Wafer 438	22.89	Yielding	Bin A
Experiment	Wafer 439	22.89	Yielding	Bin A
Experiment	Wafer 440	22.92	Yielding	Bin A
Experiment	Wafer 441	22.79	Yielding	Bin A
Experiment	Wafer 442	23.11	Yielding	Bin A
Experiment	Wafer 443	23.02	Yielding	Bin A
Experiment	Wafer 444	23.06	Yielding	Bin A
Experiment	Wafer 445	22.94	Yielding	Bin A
Experiment	Wafer 446	23.10	Yielding	Bin A
Experiment	Wafer 447	23.03	Yielding	Bin A
Experiment	Wafer 448	22.95	Yielding	Bin A
Experiment	Wafer 449	22.85	Yielding	Bin A
Experiment	Wafer 450	23.04	Yielding	Bin A
Experiment	Wafer 451	23.17	Yielding	Bin A
Experiment	Wafer 452	23.15	Yielding	Bin A
Experiment	Wafer 453	22.92	Yielding	Bin A
Experiment	Wafer 454	23.11	Yielding	Bin A
Experiment	Wafer 455	22.97	Yielding	Bin A
Experiment	Wafer 456	22.83	Yielding	Bin A
Experiment	Wafer 457	22.86	Yielding	Bin A
Experiment	Wafer 458	23.02	Yielding	Bin A
Experiment	Wafer 459	22.98	Yielding	Bin A
Experiment	Wafer 460	23.11	Yielding	Bin A
Experiment	Wafer 461	23.25	Yielding	Bin A
Experiment	Wafer 462	23.15	Yielding	Bin A
Experiment	Wafer 463	23.01	Yielding	Bin A
Experiment	Wafer 464	22.98	Yielding	Bin A
Experiment	Wafer 465	23.08	Yielding	Bin A
Experiment	Wafer 466	22.99	Yielding	Bin A
Experiment	Wafer 467	22.99	Yielding	Bin A
Experiment	Wafer 468	22.98	Yielding	Bin A
Experiment	Wafer 469	23.09	Yielding	Bin A
Experiment	Wafer 470	22.97	Yielding	Bin A
Experiment	Wafer 471	23.00	Yielding	Bin A
Experiment	Wafer 472	23.04	Yielding	Bin A
Experiment	Wafer 473	22.85	Yielding	Bin A
Experiment	Wafer 474	22.96	Yielding	Bin A
Experiment	Wafer 475	23.15	Yielding	Bin A
Experiment	Wafer 476	22.89	Yielding	Bin A
Experiment	Wafer 477	22.99	Yielding	Bin B
Experiment	Wafer 478	23.01	Yielding	Bin B
Experiment	Wafer 479	22.97	Yielding	Bin B
Experiment	Wafer 480	23.05	Yielding	Bin B

Experiment	Wafer 481	23.00	Yielding	Bin B
Experiment	Wafer 482	22.84	Yielding	Bin B
Experiment	Wafer 483	22.92	Yielding	Bin B
Experiment	Wafer 484	22.95	Yielding	Bin B
Experiment	Wafer 485	23.04	Yielding	Bin B
Experiment	Wafer 486	23.03	Yielding	Bin B
Experiment	Wafer 487	23.11	Yielding	Bin B
Experiment	Wafer 488	23.05	Yielding	Bin B
Experiment	Wafer 489	23.07	Yielding	Bin B
Experiment	Wafer 490	22.77	Yielding	Bin B
Experiment	Wafer 491	22.86	Yielding	Bin B
Experiment	Wafer 492	22.94	Yielding	Bin B
Experiment	Wafer 493	22.69	Yielding	Bin B
Experiment	Wafer 494	23.08	Yielding	Bin B
Experiment	Wafer 495	23.03	Yielding	Bin B
Experiment	Wafer 496	23.05	Yielding	Bin B
Experiment	Wafer 497	22.97	Yielding	Bin B
Experiment	Wafer 498	22.94	Yielding	Bin B
Experiment	Wafer 499	22.86	Yielding	Bin B
Experiment	Wafer 500	22.89	Yielding	Bin B
Experiment	Wafer 501	22.57	Yielding	Bin B
Experiment	Wafer 502	22.87	Yielding	Bin B
Experiment	Wafer 503	23.07	Yielding	Bin B
Experiment	Wafer 504	23.00	Yielding	Bin B
Experiment	Wafer 505	22.74	Yielding	Bin B
Experiment	Wafer 506	23.06	Yielding	Bin B
Experiment	Wafer 507	23.05	Yielding	Bin B
Experiment	Wafer 508	22.90	Yielding	Bin B
Experiment	Wafer 509	23.10	Yielding	Bin B
Experiment	Wafer 510	22.82	Yielding	Bin B
Experiment	Wafer 511	22.82	Yielding	Bin B
Experiment	Wafer 512	22.82	Yielding	Bin B
Experiment	Wafer 513	22.85	Yielding	Bin B
Experiment	Wafer 514	22.86	Yielding	Bin B
Experiment	Wafer 515	22.85	Yielding	Bin B
Experiment	Wafer 516	22.84	Yielding	Bin B
Experiment	Wafer 517	22.89	Yielding	Bin B
Experiment	Wafer 518	22.87	Yielding	Bin B
Experiment	Wafer 519	22.75	Yielding	Bin B
Experiment	Wafer 520	22.66	Yielding	Bin B
Experiment	Wafer 521	22.79	Yielding	Bin B
Experiment	Wafer 522	22.62	Yielding	Bin B
Experiment	Wafer 523	22.98	Yielding	Bin B
Experiment	Wafer 524	22.87	Yielding	Bin B

Experiment	Wafer 525	22.91	Yielding	Bin B
Experiment	Wafer 526	22.93	Yielding	Bin B
Experiment	Wafer 527	22.72	Yielding	Bin B
Experiment	Wafer 528	22.55	Yielding	Bin B
Experiment	Wafer 529	22.93	Yielding	Bin B
Experiment	Wafer 530	22.79	Yielding	Bin B
Experiment	Wafer 531	22.86	Yielding	Bin B
Experiment	Wafer 532	22.92	Yielding	Bin B
Experiment	Wafer 533	22.46	Yielding	Bin B
Experiment	Wafer 534	22.67	Yielding	Bin B
Experiment	Wafer 535	22.93	Yielding	Bin B
Experiment	Wafer 536	22.84	Yielding	Bin B
Experiment	Wafer 537	22.80	Yielding	Bin B
Experiment	Wafer 538	22.90	Yielding	Bin B
Experiment	Wafer 539	22.86	Yielding	Bin B
Experiment	Wafer 540	22.93	Yielding	Bin B
Experiment	Wafer 541	22.86	Yielding	Bin B
Experiment	Wafer 542	22.82	Yielding	Bin B
Experiment	Wafer 543	22.77	Yielding	Bin B
Experiment	Wafer 544	22.59	Yielding	Bin B
Experiment	Wafer 545	22.95	Yielding	Bin B
Experiment	Wafer 546	22.90	Yielding	Bin B
Experiment	Wafer 547	23.03	Yielding	Bin B
Experiment	Wafer 548	23.10	Yielding	Bin B
Experiment	Wafer 549	22.45	Yielding	Bin B
Experiment	Wafer 550	22.69	Yielding	Bin B
Experiment	Wafer 551	22.99	Yielding	Bin B
Experiment	Wafer 552	22.94	Yielding	Bin B
Experiment	Wafer 553	22.90	Yielding	Bin B
Experiment	Wafer 554	22.84	Yielding	Bin B
Experiment	Wafer 555	22.78	Yielding	Bin B
Experiment	Wafer 556	22.99	Yielding	Bin B
Experiment	Wafer 557	22.90	Yielding	Bin B
Experiment	Wafer 558	22.93	Yielding	Bin B
Experiment	Wafer 559	22.57	Yielding	Bin B
Experiment	Wafer 560	22.89	Yielding	Bin B
Experiment	Wafer 561	22.99	Yielding	Bin B
Experiment	Wafer 562	22.07	Non-yielding	Bin B
Experiment	Wafer 563	23.07	Yielding	Bin B
Experiment	Wafer 564	22.76	Yielding	Bin B
Experiment	Wafer 565	23.01	Yielding	Bin B
Experiment	Wafer 566	22.68	Yielding	Bin B
Experiment	Wafer 567	23.37	Yielding	Bin B
Experiment	Wafer 568	23.04	Yielding	Bin B

Experiment	Wafer 569	22.89	Yielding	Bin B
Experiment	Wafer 570	22.30	Yielding	Bin B
Experiment	Wafer 571	22.85	Yielding	Bin B
Experiment	Wafer 572	23.06	Yielding	Bin B
Experiment	Wafer 573	22.71	Yielding	Bin B
Experiment	Wafer 574	23.00	Yielding	Bin B
Experiment	Wafer 575	23.00	Yielding	Bin B
Experiment	Wafer 576	22.84	Yielding	Bin B
Experiment	Wafer 577	23.09	Yielding	Bin B
Experiment	Wafer 578	23.10	Yielding	Bin B
Experiment	Wafer 579	22.95	Yielding	Bin B
Experiment	Wafer 580	22.90	Yielding	Bin B
Experiment	Wafer 581	22.93	Yielding	Bin B
Experiment	Wafer 582	23.00	Yielding	Bin B
Experiment	Wafer 583	23.08	Yielding	Bin B
Experiment	Wafer 584	23.06	Yielding	Bin B
Experiment	Wafer 585	22.94	Yielding	Bin B
Experiment	Wafer 586	22.91	Yielding	Bin B
Experiment	Wafer 587	22.95	Yielding	Bin B
Experiment	Wafer 588	23.03	Yielding	Bin B
Experiment	Wafer 589	22.87	Yielding	Bin B
Experiment	Wafer 590	23.22	Yielding	Bin B
Experiment	Wafer 591	22.97	Yielding	Bin B
Experiment	Wafer 592	22.98	Yielding	Bin B
Experiment	Wafer 593	23.08	Yielding	Bin B
Experiment	Wafer 594	22.96	Yielding	Bin B
Experiment	Wafer 595	22.89	Yielding	Bin B
Experiment	Wafer 596	23.11	Yielding	Bin B
Experiment	Wafer 597	22.94	Yielding	Bin B
Experiment	Wafer 598	22.87	Yielding	Bin B
Experiment	Wafer 599	22.87	Yielding	Bin B
Experiment	Wafer 600	22.97	Yielding	Bin B
Experiment	Wafer 601	23.03	Yielding	Bin B
Experiment	Wafer 602	22.87	Yielding	Bin B
Experiment	Wafer 603	23.07	Yielding	Bin B
Experiment	Wafer 604	22.60	Yielding	Bin B
Experiment	Wafer 605	23.03	Yielding	Bin B
Experiment	Wafer 606	22.85	Yielding	Bin B
Experiment	Wafer 607	23.03	Yielding	Bin B
Experiment	Wafer 608	22.85	Yielding	Bin B
Experiment	Wafer 609	23.01	Yielding	Bin B
Experiment	Wafer 610	22.98	Yielding	Bin B
Experiment	Wafer 611	23.15	Yielding	Bin B
Experiment	Wafer 612	23.04	Yielding	Bin B

Experiment	Wafer 613	23.17	Yielding	Bin B
Experiment	Wafer 614	23.14	Yielding	Bin B
Experiment	Wafer 615	22.86	Yielding	Bin B
Experiment	Wafer 616	22.99	Yielding	Bin B
Experiment	Wafer 617	22.97	Yielding	Bin B
Experiment	Wafer 618	23.06	Yielding	Bin B
Experiment	Wafer 619	23.06	Yielding	Bin B
Experiment	Wafer 620	23.10	Yielding	Bin B
Experiment	Wafer 621	23.11	Yielding	Bin B
Experiment	Wafer 622	23.15	Yielding	Bin B
Experiment	Wafer 623	22.99	Yielding	Bin B
Experiment	Wafer 624	23.17	Yielding	Bin B
Experiment	Wafer 625	22.97	Yielding	Bin B
Experiment	Wafer 626	22.84	Yielding	Bin B
Experiment	Wafer 627	23.00	Yielding	Bin B
Experiment	Wafer 628	22.95	Yielding	Bin B
Experiment	Wafer 629	23.12	Yielding	Bin B
Experiment	Wafer 630	22.86	Yielding	Bin B
Experiment	Wafer 631	22.94	Yielding	Bin B
Experiment	Wafer 632	23.36	Yielding	Bin B
Experiment	Wafer 633	22.87	Yielding	Bin B
Experiment	Wafer 634	23.01	Yielding	Bin B
Experiment	Wafer 635	23.08	Yielding	Bin B
Experiment	Wafer 636	23.11	Yielding	Bin B
Experiment	Wafer 637	23.13	Yielding	Bin B
Experiment	Wafer 638	23.07	Yielding	Bin B
Experiment	Wafer 639	22.68	Yielding	Bin B
Experiment	Wafer 640	23.04	Yielding	Bin B
Experiment	Wafer 641	22.95	Yielding	Bin B
Experiment	Wafer 642	22.84	Yielding	Bin B
Experiment	Wafer 643	22.85	Yielding	Bin B
Experiment	Wafer 644	22.98	Yielding	Bin B
Experiment	Wafer 645	23.01	Yielding	Bin B
Experiment	Wafer 646	22.92	Yielding	Bin B
Experiment	Wafer 647	22.82	Yielding	Bin B
Experiment	Wafer 648	22.83	Yielding	Bin B
Experiment	Wafer 649	22.79	Yielding	Bin B
Experiment	Wafer 650	22.60	Yielding	Bin B
Experiment	Wafer 651	22.79	Yielding	Bin B
Experiment	Wafer 652	22.96	Yielding	Bin B
Experiment	Wafer 653	22.93	Yielding	Bin B
Experiment	Wafer 654	23.02	Yielding	Bin B
Experiment	Wafer 655	23.03	Yielding	Bin B
Experiment	Wafer 656	23.04	Yielding	Bin B

Experiment	Wafer 657	22.95	Yielding	Bin B
Experiment	Wafer 658	22.75	Yielding	Bin B
Experiment	Wafer 659	22.92	Yielding	Bin B
Experiment	Wafer 660	23.10	Yielding	Bin B
Experiment	Wafer 661	22.87	Yielding	Bin B
Experiment	Wafer 662	23.01	Yielding	Bin B
Experiment	Wafer 663	23.02	Yielding	Bin B
Experiment	Wafer 664	22.90	Yielding	Bin B
Experiment	Wafer 665	22.99	Yielding	Bin B
Experiment	Wafer 666	22.77	Yielding	Bin B
Experiment	Wafer 667	23.00	Yielding	Bin B
Experiment	Wafer 668	22.89	Yielding	Bin B
Experiment	Wafer 669	22.93	Yielding	Bin B
Experiment	Wafer 670	22.96	Yielding	Bin B
Experiment	Wafer 671	22.95	Yielding	Bin B
Experiment	Wafer 672	23.06	Yielding	Bin B
Experiment	Wafer 673	22.84	Yielding	Bin B
Experiment	Wafer 674	22.78	Yielding	Bin B
Experiment	Wafer 675	23.18	Yielding	Bin B
Experiment	Wafer 676	22.70	Yielding	Bin B
Experiment	Wafer 677	22.79	Yielding	Bin B
Experiment	Wafer 678	22.92	Yielding	Bin B
Experiment	Wafer 679	22.60	Yielding	Bin B
Experiment	Wafer 680	23.14	Yielding	Bin B
Experiment	Wafer 681	22.93	Yielding	Bin B
Experiment	Wafer 682	22.89	Yielding	Bin B
Experiment	Wafer 683	23.07	Yielding	Bin B
Experiment	Wafer 684	23.00	Yielding	Bin B
Experiment	Wafer 685	22.87	Yielding	Bin B
Experiment	Wafer 686	22.85	Yielding	Bin B
Experiment	Wafer 687	22.19	Non-yielding	Bin B
Experiment	Wafer 688	22.97	Yielding	Bin B
Experiment	Wafer 689	22.97	Yielding	Bin B
Experiment	Wafer 690	22.99	Yielding	Bin B
Experiment	Wafer 691	22.85	Yielding	Bin B
Experiment	Wafer 692	22.60	Yielding	Bin B
Experiment	Wafer 693	22.68	Yielding	Bin B
Experiment	Wafer 694	22.93	Yielding	Bin B
Experiment	Wafer 695	22.76	Yielding	Bin B
Experiment	Wafer 696	22.79	Yielding	Bin B
Experiment	Wafer 697	22.76	Yielding	Bin B
Experiment	Wafer 698	22.84	Yielding	Bin B
Experiment	Wafer 699	23.01	Yielding	Bin B
Experiment	Wafer 700	22.92	Yielding	Bin B

Experiment	Wafer 701	22.92	Yielding	Bin B
Experiment	Wafer 702	23.00	Yielding	Bin B
Experiment	Wafer 703	22.89	Yielding	Bin B
Experiment	Wafer 704	22.80	Yielding	Bin B
Experiment	Wafer 705	22.95	Yielding	Bin B
Experiment	Wafer 706	22.90	Yielding	Bin B
Experiment	Wafer 707	22.97	Yielding	Bin B
Experiment	Wafer 708	22.87	Yielding	Bin B
Experiment	Wafer 709	22.85	Yielding	Bin B
Experiment	Wafer 710	23.03	Yielding	Bin B
Experiment	Wafer 711	22.80	Yielding	Bin B
Experiment	Wafer 712	22.93	Yielding	Bin B
Experiment	Wafer 713	22.90	Yielding	Bin B
Experiment	Wafer 714	22.86	Yielding	Bin B
Experiment	Wafer 715	23.11	Yielding	Bin B
Experiment	Wafer 716	22.94	Yielding	Bin B
Experiment	Wafer 717	22.60	Yielding	Bin B
Experiment	Wafer 718	23.04	Yielding	Bin B
Experiment	Wafer 719	22.93	Yielding	Bin B
Experiment	Wafer 720	22.89	Yielding	Bin B
Experiment	Wafer 721	23.06	Yielding	Bin B
Experiment	Wafer 722	22.88	Yielding	Bin B
Experiment	Wafer 723	22.87	Yielding	Bin B
Experiment	Wafer 724	22.98	Yielding	Bin B
Experiment	Wafer 725	22.81	Yielding	Bin B
Experiment	Wafer 726	22.97	Yielding	Bin B
Experiment	Wafer 727	22.80	Yielding	Bin B
Experiment	Wafer 728	22.80	Yielding	Bin B
Experiment	Wafer 729	22.69	Yielding	Bin B
Experiment	Wafer 730	22.95	Yielding	Bin B
Experiment	Wafer 731	22.88	Yielding	Bin B
Experiment	Wafer 732	22.75	Yielding	Bin B
Experiment	Wafer 733	22.92	Yielding	Bin B
Experiment	Wafer 734	22.71	Yielding	Bin B
Experiment	Wafer 735	22.79	Yielding	Bin B
Experiment	Wafer 736	22.45	Yielding	Bin B
Experiment	Wafer 737	22.84	Yielding	Bin B
Experiment	Wafer 738	22.63	Yielding	Bin B
Experiment	Wafer 739	22.89	Yielding	Bin B
Experiment	Wafer 740	22.78	Yielding	Bin B
Experiment	Wafer 741	22.80	Yielding	Bin B
Experiment	Wafer 742	23.03	Yielding	Bin B
Experiment	Wafer 743	23.14	Yielding	Bin B
Experiment	Wafer 744	22.90	Yielding	Bin B

Experiment	Wafer 745	22.87	Yielding	Bin B
Experiment	Wafer 746	22.87	Yielding	Bin B
Experiment	Wafer 747	22.78	Yielding	Bin B
Experiment	Wafer 748	22.71	Yielding	Bin B
Experiment	Wafer 749	22.84	Yielding	Bin B
Experiment	Wafer 750	22.96	Yielding	Bin B
Experiment	Wafer 751	22.74	Yielding	Bin B
Experiment	Wafer 752	22.98	Yielding	Bin B
Experiment	Wafer 753	23.01	Yielding	Bin B
Experiment	Wafer 754	22.99	Yielding	Bin B
Experiment	Wafer 755	22.79	Yielding	Bin B
Experiment	Wafer 756	22.65	Yielding	Bin B
Experiment	Wafer 757	22.93	Yielding	Bin B
Experiment	Wafer 758	22.85	Yielding	Bin B
Experiment	Wafer 759	22.85	Yielding	Bin B
Experiment	Wafer 760	22.82	Yielding	Bin B
Experiment	Wafer 761	22.92	Yielding	Bin B
Experiment	Wafer 762	22.80	Yielding	Bin B
Experiment	Wafer 763	22.43	Yielding	Bin B
Experiment	Wafer 764	22.69	Yielding	Bin B
Experiment	Wafer 765	22.72	Yielding	Bin B
Experiment	Wafer 766	22.83	Yielding	Bin B
Experiment	Wafer 767	22.63	Yielding	Bin B
Experiment	Wafer 768	22.71	Yielding	Bin B
Experiment	Wafer 769	22.96	Yielding	Bin B
Experiment	Wafer 770	22.72	Yielding	Bin B
Experiment	Wafer 771	22.99	Yielding	Bin B
Experiment	Wafer 772	22.82	Yielding	Bin B
Experiment	Wafer 773	22.76	Yielding	Bin B
Experiment	Wafer 774	23.00	Yielding	Bin B
Experiment	Wafer 775	22.83	Yielding	Bin B
Experiment	Wafer 776	22.80	Yielding	Bin B
Experiment	Wafer 777	22.70	Yielding	Bin B
Experiment	Wafer 778	22.90	Yielding	Bin B
Experiment	Wafer 779	22.80	Yielding	Bin B
Experiment	Wafer 780	22.44	Yielding	Bin B
Experiment	Wafer 781	22.93	Yielding	Bin B
Experiment	Wafer 782	22.84	Yielding	Bin B
Experiment	Wafer 783	22.97	Yielding	Bin B
Experiment	Wafer 784	22.98	Yielding	Bin B
Experiment	Wafer 785	22.69	Yielding	Bin B
Experiment	Wafer 786	22.71	Yielding	Bin B
Experiment	Wafer 787	22.92	Yielding	Bin B
Experiment	Wafer 788	22.95	Yielding	Bin B

Experiment	Wafer 789	22.98	Yielding	Bin B
Experiment	Wafer 790	22.98	Yielding	Bin B
Experiment	Wafer 791	23.35	Yielding	Bin B
Experiment	Wafer 792	22.95	Yielding	Bin B
Experiment	Wafer 793	22.75	Yielding	Bin B
Experiment	Wafer 794	22.98	Yielding	Bin B
Experiment	Wafer 795	22.12	Non-yielding	Bin B
Experiment	Wafer 796	22.72	Yielding	Bin B
Experiment	Wafer 797	22.74	Yielding	Bin B
Experiment	Wafer 798	22.64	Yielding	Bin B
Experiment	Wafer 799	22.99	Yielding	Bin B
Experiment	Wafer 800	22.86	Yielding	Bin B
Experiment	Wafer 801	22.76	Yielding	Bin B
Experiment	Wafer 802	22.84	Yielding	Bin B
Experiment	Wafer 803	22.10	Non-yielding	Bin B
Experiment	Wafer 804	23.12	Yielding	Bin B
Experiment	Wafer 805	22.92	Yielding	Bin B
Experiment	Wafer 806	22.61	Yielding	Bin B
Experiment	Wafer 807	22.94	Yielding	Bin B
Experiment	Wafer 808	22.96	Yielding	Bin B
Experiment	Wafer 809	22.99	Yielding	Bin B
Experiment	Wafer 810	22.53	Yielding	Bin B
Experiment	Wafer 811	23.02	Yielding	Bin B
Experiment	Wafer 812	22.89	Yielding	Bin B
Experiment	Wafer 813	22.93	Yielding	Bin B
Experiment	Wafer 814	22.85	Yielding	Bin B
Experiment	Wafer 815	22.65	Yielding	Bin B
Experiment	Wafer 816	23.07	Yielding	Bin B
Experiment	Wafer 817	22.91	Yielding	Bin B
Experiment	Wafer 818	22.98	Yielding	Bin B
Experiment	Wafer 819	22.90	Yielding	Bin B
Experiment	Wafer 820	22.67	Yielding	Bin B
Experiment	Wafer 821	22.90	Yielding	Bin B
Experiment	Wafer 822	22.98	Yielding	Bin B
Experiment	Wafer 823	22.93	Yielding	Bin B
Experiment	Wafer 824	23.00	Yielding	Bin B
Experiment	Wafer 825	23.12	Yielding	Bin B
Experiment	Wafer 826	22.71	Yielding	Bin B
Experiment	Wafer 827	22.98	Yielding	Bin C
Experiment	Wafer 828	22.82	Yielding	Bin C
Experiment	Wafer 829	22.64	Yielding	Bin C
Experiment	Wafer 830	22.86	Yielding	Bin C
Experiment	Wafer 831	22.91	Yielding	Bin C
Experiment	Wafer 832	23.09	Yielding	Bin C

Experiment	Wafer 833	22.84	Yielding	Bin C
Experiment	Wafer 834	22.92	Yielding	Bin C
Experiment	Wafer 835	22.78	Yielding	Bin C
Experiment	Wafer 836	22.89	Yielding	Bin C
Experiment	Wafer 837	22.85	Yielding	Bin C
Experiment	Wafer 838	22.87	Yielding	Bin C
Experiment	Wafer 839	22.55	Yielding	Bin C
Experiment	Wafer 840	22.37	Yielding	Bin C
Experiment	Wafer 841	23.04	Yielding	Bin C
Experiment	Wafer 842	22.86	Yielding	Bin C
Experiment	Wafer 843	22.95	Yielding	Bin C
Experiment	Wafer 844	23.01	Yielding	Bin C
Experiment	Wafer 845	22.79	Yielding	Bin C
Experiment	Wafer 846	22.93	Yielding	Bin C
Experiment	Wafer 847	22.50	Yielding	Bin C
Experiment	Wafer 848	22.70	Yielding	Bin C
Experiment	Wafer 849	22.84	Yielding	Bin C
Experiment	Wafer 850	22.85	Yielding	Bin C
Experiment	Wafer 851	22.88	Yielding	Bin C
Experiment	Wafer 852	22.62	Yielding	Bin C
Experiment	Wafer 853	22.74	Yielding	Bin C
Experiment	Wafer 854	22.20	Non-yielding	Bin C
Experiment	Wafer 855	22.80	Yielding	Bin C
Experiment	Wafer 856	23.16	Yielding	Bin C
Experiment	Wafer 857	22.99	Yielding	Bin C
Experiment	Wafer 858	23.17	Yielding	Bin C
Experiment	Wafer 859	23.16	Yielding	Bin C
Experiment	Wafer 860	23.12	Yielding	Bin C
Experiment	Wafer 861	23.12	Yielding	Bin C
Experiment	Wafer 862	23.06	Yielding	Bin C
Experiment	Wafer 863	23.17	Yielding	Bin C
Experiment	Wafer 864	23.12	Yielding	Bin C
Experiment	Wafer 865	23.19	Yielding	Bin C
Experiment	Wafer 866	23.18	Yielding	Bin C
Experiment	Wafer 867	23.12	Yielding	Bin C
Experiment	Wafer 868	23.09	Yielding	Bin C
Experiment	Wafer 869	23.15	Yielding	Bin C
Experiment	Wafer 870	23.04	Yielding	Bin C
Experiment	Wafer 871	23.00	Yielding	Bin C
Experiment	Wafer 872	23.12	Yielding	Bin C
Experiment	Wafer 873	23.10	Yielding	Bin C
Experiment	Wafer 874	23.13	Yielding	Bin C
Experiment	Wafer 875	23.10	Yielding	Bin C
Experiment	Wafer 876	23.10	Yielding	Bin C

Experiment	Wafer 877	23.22	Yielding	Bin C
Experiment	Wafer 878	23.19	Yielding	Bin C
Experiment	Wafer 879	23.14	Yielding	Bin C
Experiment	Wafer 880	23.11	Yielding	Bin C
Experiment	Wafer 881	23.16	Yielding	Bin C
Experiment	Wafer 882	23.10	Yielding	Bin C
Experiment	Wafer 883	22.78	Yielding	Bin C
Experiment	Wafer 884	23.06	Yielding	Bin C
Experiment	Wafer 885	23.17	Yielding	Bin C
Experiment	Wafer 886	23.06	Yielding	Bin C
Experiment	Wafer 887	22.96	Yielding	Bin C
Experiment	Wafer 888	23.16	Yielding	Bin C
Experiment	Wafer 889	23.11	Yielding	Bin C
Experiment	Wafer 890	23.01	Yielding	Bin C
Experiment	Wafer 891	23.00	Yielding	Bin C
Experiment	Wafer 892	23.02	Yielding	Bin C
Experiment	Wafer 893	23.11	Yielding	Bin C
Experiment	Wafer 894	23.12	Yielding	Bin C
Experiment	Wafer 895	23.07	Yielding	Bin C
Experiment	Wafer 896	23.18	Yielding	Bin C
Experiment	Wafer 897	22.98	Yielding	Bin C
Experiment	Wafer 898	23.15	Yielding	Bin C
Experiment	Wafer 899	23.20	Yielding	Bin C
Experiment	Wafer 900	23.11	Yielding	Bin C
Experiment	Wafer 901	23.21	Yielding	Bin C
Experiment	Wafer 902	23.55	Yielding	Bin C
Experiment	Wafer 903	23.11	Yielding	Bin C
Experiment	Wafer 904	23.20	Yielding	Bin C
Experiment	Wafer 905	23.15	Yielding	Bin C
Experiment	Wafer 906	22.97	Yielding	Bin C
Experiment	Wafer 907	23.12	Yielding	Bin C
Experiment	Wafer 908	23.25	Yielding	Bin C
Experiment	Wafer 909	23.04	Yielding	Bin C
Experiment	Wafer 910	23.18	Yielding	Bin C
Experiment	Wafer 911	23.07	Yielding	Bin C
Experiment	Wafer 912	23.20	Yielding	Bin C
Experiment	Wafer 913	23.06	Yielding	Bin C
Experiment	Wafer 914	23.11	Yielding	Bin C
Experiment	Wafer 915	23.00	Yielding	Bin C
Experiment	Wafer 916	23.05	Yielding	Bin C
Experiment	Wafer 917	23.13	Yielding	Bin C
Experiment	Wafer 918	23.04	Yielding	Bin C
Experiment	Wafer 919	23.03	Yielding	Bin C
Experiment	Wafer 920	22.99	Yielding	Bin C

Experiment	Wafer 921	23.09	Yielding	Bin C
Experiment	Wafer 922	23.13	Yielding	Bin C
Experiment	Wafer 923	23.11	Yielding	Bin C
Experiment	Wafer 924	23.12	Yielding	Bin C
Experiment	Wafer 925	23.20	Yielding	Bin C
Experiment	Wafer 926	23.15	Yielding	Bin C
Experiment	Wafer 927	23.13	Yielding	Bin C
Experiment	Wafer 928	22.94	Yielding	Bin C
Experiment	Wafer 929	23.11	Yielding	Bin C
Experiment	Wafer 930	23.13	Yielding	Bin C
Experiment	Wafer 931	23.07	Yielding	Bin C
Experiment	Wafer 932	22.95	Yielding	Bin C
Experiment	Wafer 933	23.01	Yielding	Bin C
Experiment	Wafer 934	22.96	Yielding	Bin C
Experiment	Wafer 935	22.99	Yielding	Bin C
Experiment	Wafer 936	23.15	Yielding	Bin C
Experiment	Wafer 937	22.98	Yielding	Bin C
Experiment	Wafer 938	23.07	Yielding	Bin C
Experiment	Wafer 939	23.09	Yielding	Bin C
Experiment	Wafer 940	23.37	Yielding	Bin C
Experiment	Wafer 941	23.15	Yielding	Bin C
Experiment	Wafer 942	23.21	Yielding	Bin C
Experiment	Wafer 943	23.17	Yielding	Bin C
Experiment	Wafer 944	22.98	Yielding	Bin C
Experiment	Wafer 945	23.10	Yielding	Bin C
Experiment	Wafer 946	23.17	Yielding	Bin C
Experiment	Wafer 947	23.12	Yielding	Bin C
Experiment	Wafer 948	23.12	Yielding	Bin C
Experiment	Wafer 949	23.13	Yielding	Bin C
Experiment	Wafer 950	23.19	Yielding	Bin C
Experiment	Wafer 951	23.03	Yielding	Bin C
Experiment	Wafer 952	23.19	Yielding	Bin C
Experiment	Wafer 953	23.09	Yielding	Bin C
Experiment	Wafer 954	23.12	Yielding	Bin C
Experiment	Wafer 955	22.98	Yielding	Bin C
Experiment	Wafer 956	23.16	Yielding	Bin C
Experiment	Wafer 957	23.16	Yielding	Bin C
Experiment	Wafer 958	23.00	Yielding	Bin C
Experiment	Wafer 959	23.13	Yielding	Bin C
Experiment	Wafer 960	23.20	Yielding	Bin C
Experiment	Wafer 961	23.04	Yielding	Bin C
Experiment	Wafer 962	23.11	Yielding	Bin C
Experiment	Wafer 963	22.99	Yielding	Bin C
Experiment	Wafer 964	23.03	Yielding	Bin C

Experiment	Wafer 965	23.13	Yielding	Bin C
Experiment	Wafer 966	23.15	Yielding	Bin C
Experiment	Wafer 967	23.12	Yielding	Bin C
Experiment	Wafer 968	23.10	Yielding	Bin C
Experiment	Wafer 969	22.72	Yielding	Bin C
Experiment	Wafer 970	23.09	Yielding	Bin C
Experiment	Wafer 971	23.11	Yielding	Bin C
Experiment	Wafer 972	23.08	Yielding	Bin C
Experiment	Wafer 973	23.08	Yielding	Bin C
Experiment	Wafer 974	23.17	Yielding	Bin C
Experiment	Wafer 975	22.93	Yielding	Bin C
Experiment	Wafer 976	22.98	Yielding	Bin C
Experiment	Wafer 977	23.02	Yielding	Bin C
Experiment	Wafer 978	23.01	Yielding	Bin C
Experiment	Wafer 979	23.02	Yielding	Bin C
Experiment	Wafer 980	23.07	Yielding	Bin C
Experiment	Wafer 981	23.12	Yielding	Bin C
Experiment	Wafer 982	23.19	Yielding	Bin C
Experiment	Wafer 983	22.89	Yielding	Bin C
Experiment	Wafer 984	22.93	Yielding	Bin C
Experiment	Wafer 985	21.64	Non-yielding	Bin C
Experiment	Wafer 986	22.86	Yielding	Bin C
Experiment	Wafer 987	22.75	Yielding	Bin C
Experiment	Wafer 988	23.05	Yielding	Bin C
Experiment	Wafer 989	23.14	Yielding	Bin C
Experiment	Wafer 990	23.04	Yielding	Bin C
Experiment	Wafer 991	23.10	Yielding	Bin C
Experiment	Wafer 992	23.08	Yielding	Bin C
Experiment	Wafer 993	22.91	Yielding	Bin C
Experiment	Wafer 994	23.12	Yielding	Bin C
Experiment	Wafer 995	22.99	Yielding	Bin C
Experiment	Wafer 996	23.14	Yielding	Bin C
Experiment	Wafer 997	23.11	Yielding	Bin C
Experiment	Wafer 998	23.24	Yielding	Bin C
Experiment	Wafer 999	23.23	Yielding	Bin C
Experiment	Wafer 1000	22.98	Yielding	Bin C
Control	Wafer 1	22.97	Yielding	Bin A
Control	Wafer 2	23.26	Yielding	Bin A
Control	Wafer 3	23.04	Yielding	Bin A
Control	Wafer 4	23.21	Yielding	Bin A
Control	Wafer 5	22.88	Yielding	Bin A
Control	Wafer 6	22.92	Yielding	Bin A
Control	Wafer 7	23.00	Yielding	Bin A
Control	Wafer 8	23.02	Yielding	Bin A

Control	Wafer 9	22.87	Yielding	Bin A
Control	Wafer 10	22.87	Yielding	Bin A
Control	Wafer 11	22.43	Yielding	Bin A
Control	Wafer 12	22.94	Yielding	Bin A
Control	Wafer 13	22.97	Yielding	Bin A
Control	Wafer 14	22.83	Yielding	Bin A
Control	Wafer 15	22.67	Yielding	Bin A
Control	Wafer 16	22.75	Yielding	Bin A
Control	Wafer 17	22.53	Yielding	Bin A
Control	Wafer 18	22.93	Yielding	Bin A
Control	Wafer 19	22.77	Yielding	Bin A
Control	Wafer 20	22.83	Yielding	Bin A
Control	Wafer 21	22.82	Yielding	Bin A
Control	Wafer 22	22.94	Yielding	Bin A
Control	Wafer 23	22.74	Yielding	Bin A
Control	Wafer 24	22.55	Yielding	Bin A
Control	Wafer 25	22.08	Yielding	Bin A
Control	Wafer 26	22.33	Yielding	Bin A
Control	Wafer 27	22.63	Yielding	Bin A
Control	Wafer 28	22.78	Yielding	Bin A
Control	Wafer 29	22.30	Yielding	Bin A
Control	Wafer 30	22.51	Yielding	Bin A
Control	Wafer 31	22.37	Yielding	Bin A
Control	Wafer 32	22.77	Yielding	Bin A
Control	Wafer 33	22.77	Yielding	Bin A
Control	Wafer 34	22.51	Yielding	Bin A
Control	Wafer 35	22.78	Yielding	Bin A
Control	Wafer 36	22.79	Yielding	Bin A
Control	Wafer 37	22.82	Yielding	Bin A
Control	Wafer 38	22.73	Yielding	Bin A
Control	Wafer 39	22.89	Yielding	Bin A
Control	Wafer 40	22.95	Yielding	Bin A
Control	Wafer 41	22.70	Yielding	Bin A
Control	Wafer 42	22.58	Yielding	Bin A
Control	Wafer 43	22.69	Yielding	Bin A
Control	Wafer 44	22.70	Yielding	Bin A
Control	Wafer 45	22.86	Yielding	Bin A
Control	Wafer 46	22.85	Yielding	Bin A
Control	Wafer 47	22.91	Yielding	Bin A
Control	Wafer 48	22.83	Yielding	Bin A
Control	Wafer 49	22.81	Yielding	Bin A
Control	Wafer 50	22.74	Yielding	Bin A
Control	Wafer 51	23.07	Yielding	Bin A
Control	Wafer 52	22.69	Yielding	Bin A

Control	Wafer 53	22.78	Yielding	Bin A
Control	Wafer 54	23.03	Yielding	Bin A
Control	Wafer 55	23.03	Yielding	Bin A
Control	Wafer 56	22.82	Yielding	Bin A
Control	Wafer 57	22.89	Yielding	Bin A
Control	Wafer 58	23.19	Yielding	Bin A
Control	Wafer 59	22.93	Yielding	Bin A
Control	Wafer 60	23.01	Yielding	Bin A
Control	Wafer 61	22.95	Yielding	Bin A
Control	Wafer 62	22.92	Yielding	Bin A
Control	Wafer 63	23.04	Yielding	Bin A
Control	Wafer 64	23.06	Yielding	Bin A
Control	Wafer 65	23.05	Yielding	Bin A
Control	Wafer 66	23.04	Yielding	Bin A
Control	Wafer 67	23.18	Yielding	Bin A
Control	Wafer 68	22.56	Yielding	Bin A
Control	Wafer 69	22.87	Yielding	Bin A
Control	Wafer 70	23.01	Yielding	Bin A
Control	Wafer 71	23.09	Yielding	Bin A
Control	Wafer 72	22.81	Yielding	Bin A
Control	Wafer 73	22.90	Yielding	Bin A
Control	Wafer 74	23.10	Yielding	Bin A
Control	Wafer 75	22.59	Yielding	Bin A
Control	Wafer 76	22.63	Yielding	Bin A
Control	Wafer 77	22.90	Yielding	Bin A
Control	Wafer 78	22.80	Yielding	Bin A
Control	Wafer 79	22.86	Yielding	Bin A
Control	Wafer 80	22.91	Yielding	Bin A
Control	Wafer 81	22.73	Yielding	Bin A
Control	Wafer 82	23.13	Yielding	Bin A
Control	Wafer 83	22.77	Yielding	Bin A
Control	Wafer 84	23.00	Yielding	Bin A
Control	Wafer 85	22.72	Yielding	Bin A
Control	Wafer 86	22.85	Yielding	Bin A
Control	Wafer 87	22.65	Yielding	Bin A
Control	Wafer 88	22.97	Yielding	Bin A
Control	Wafer 89	22.60	Yielding	Bin A
Control	Wafer 90	22.88	Yielding	Bin A
Control	Wafer 91	22.89	Yielding	Bin A
Control	Wafer 92	22.98	Yielding	Bin A
Control	Wafer 93	22.69	Yielding	Bin A
Control	Wafer 94	23.03	Yielding	Bin A
Control	Wafer 95	23.09	Yielding	Bin A
Control	Wafer 96	23.14	Yielding	Bin A

Control	Wafer 97	23.12	Yielding	Bin A
Control	Wafer 98	22.49	Yielding	Bin A
Control	Wafer 99	22.86	Yielding	Bin A
Control	Wafer 100	23.05	Yielding	Bin A
Control	Wafer 101	22.91	Yielding	Bin A
Control	Wafer 102	22.81	Yielding	Bin A
Control	Wafer 103	23.07	Yielding	Bin A
Control	Wafer 104	22.87	Yielding	Bin A
Control	Wafer 105	22.94	Yielding	Bin A
Control	Wafer 106	22.83	Yielding	Bin A
Control	Wafer 107	22.94	Yielding	Bin A
Control	Wafer 108	22.98	Yielding	Bin A
Control	Wafer 109	23.15	Yielding	Bin A
Control	Wafer 110	23.03	Yielding	Bin A
Control	Wafer 111	22.97	Yielding	Bin A
Control	Wafer 112	22.96	Yielding	Bin A
Control	Wafer 113	23.08	Yielding	Bin A
Control	Wafer 114	22.80	Yielding	Bin A
Control	Wafer 115	23.14	Yielding	Bin A
Control	Wafer 116	22.93	Yielding	Bin A
Control	Wafer 117	22.93	Yielding	Bin A
Control	Wafer 118	22.90	Yielding	Bin A
Control	Wafer 119	22.89	Yielding	Bin A
Control	Wafer 120	22.89	Yielding	Bin A
Control	Wafer 121	22.99	Yielding	Bin A
Control	Wafer 122	22.90	Yielding	Bin A
Control	Wafer 123	22.96	Yielding	Bin A
Control	Wafer 124	22.99	Yielding	Bin A
Control	Wafer 125	23.02	Yielding	Bin A
Control	Wafer 126	22.81	Yielding	Bin A
Control	Wafer 127	22.88	Yielding	Bin A
Control	Wafer 128	22.90	Yielding	Bin A
Control	Wafer 129	22.98	Yielding	Bin A
Control	Wafer 130	22.92	Yielding	Bin A
Control	Wafer 131	23.04	Yielding	Bin A
Control	Wafer 132	22.93	Yielding	Bin A
Control	Wafer 133	22.95	Yielding	Bin A
Control	Wafer 134	23.03	Yielding	Bin A
Control	Wafer 135	22.87	Yielding	Bin A
Control	Wafer 136	22.90	Yielding	Bin A
Control	Wafer 137	22.90	Yielding	Bin A
Control	Wafer 138	22.88	Yielding	Bin A
Control	Wafer 139	22.68	Yielding	Bin A
Control	Wafer 140	23.02	Yielding	Bin A

Control	Wafer 141	22.92	Yielding	Bin A
Control	Wafer 142	22.64	Yielding	Bin A
Control	Wafer 143	23.07	Yielding	Bin A
Control	Wafer 144	22.71	Yielding	Bin A
Control	Wafer 145	22.88	Yielding	Bin A
Control	Wafer 146	23.04	Yielding	Bin A
Control	Wafer 147	22.71	Yielding	Bin A
Control	Wafer 148	23.06	Yielding	Bin A
Control	Wafer 149	22.90	Yielding	Bin A
Control	Wafer 150	22.81	Yielding	Bin A
Control	Wafer 151	23.09	Yielding	Bin A
Control	Wafer 152	22.89	Yielding	Bin A
Control	Wafer 153	23.02	Yielding	Bin A
Control	Wafer 154	22.78	Yielding	Bin A
Control	Wafer 155	22.85	Yielding	Bin A
Control	Wafer 156	22.87	Yielding	Bin A
Control	Wafer 157	22.93	Yielding	Bin A
Control	Wafer 158	22.97	Yielding	Bin A
Control	Wafer 159	23.16	Yielding	Bin A
Control	Wafer 160	23.07	Yielding	Bin A
Control	Wafer 161	23.00	Yielding	Bin A
Control	Wafer 162	22.71	Yielding	Bin A
Control	Wafer 163	23.03	Yielding	Bin A
Control	Wafer 164	23.17	Yielding	Bin A
Control	Wafer 165	22.87	Yielding	Bin A
Control	Wafer 166	23.07	Yielding	Bin A
Control	Wafer 167	22.80	Yielding	Bin A
Control	Wafer 168	22.97	Yielding	Bin A
Control	Wafer 169	22.79	Yielding	Bin A
Control	Wafer 170	22.65	Yielding	Bin A
Control	Wafer 171	22.81	Yielding	Bin A
Control	Wafer 172	22.87	Yielding	Bin A
Control	Wafer 173	22.99	Yielding	Bin A
Control	Wafer 174	23.04	Yielding	Bin A
Control	Wafer 175	23.13	Yielding	Bin A
Control	Wafer 176	22.82	Yielding	Bin A
Control	Wafer 177	23.05	Yielding	Bin A
Control	Wafer 178	22.57	Yielding	Bin A
Control	Wafer 179	22.40	Yielding	Bin A
Control	Wafer 180	22.99	Yielding	Bin A
Control	Wafer 181	22.76	Yielding	Bin A
Control	Wafer 182	22.73	Yielding	Bin A
Control	Wafer 183	22.73	Yielding	Bin A
Control	Wafer 184	22.94	Yielding	Bin A

Control	Wafer 185	23.10	Yielding	Bin A
Control	Wafer 186	22.70	Yielding	Bin A
Control	Wafer 187	22.71	Yielding	Bin A
Control	Wafer 188	22.66	Yielding	Bin A
Control	Wafer 189	22.83	Yielding	Bin A
Control	Wafer 190	22.84	Yielding	Bin A
Control	Wafer 191	23.17	Yielding	Bin A
Control	Wafer 192	22.96	Yielding	Bin A
Control	Wafer 193	22.99	Yielding	Bin A
Control	Wafer 194	23.20	Yielding	Bin A
Control	Wafer 195	23.57	Yielding	Bin A
Control	Wafer 196	23.31	Yielding	Bin A
Control	Wafer 197	23.28	Yielding	Bin A
Control	Wafer 198	23.10	Yielding	Bin A
Control	Wafer 199	23.30	Yielding	Bin A
Control	Wafer 200	23.14	Yielding	Bin B
Control	Wafer 201	22.66	Yielding	Bin B
Control	Wafer 202	22.81	Yielding	Bin B
Control	Wafer 203	22.85	Yielding	Bin B
Control	Wafer 204	22.91	Yielding	Bin B
Control	Wafer 205	22.49	Yielding	Bin B
Control	Wafer 206	22.84	Yielding	Bin B
Control	Wafer 207	23.21	Yielding	Bin B
Control	Wafer 208	23.06	Yielding	Bin B
Control	Wafer 209	22.70	Yielding	Bin B
Control	Wafer 210	22.90	Yielding	Bin B
Control	Wafer 211	23.12	Yielding	Bin B
Control	Wafer 212	23.11	Yielding	Bin B
Control	Wafer 213	22.98	Yielding	Bin B
Control	Wafer 214	23.02	Yielding	Bin B
Control	Wafer 215	23.05	Yielding	Bin B
Control	Wafer 216	23.13	Yielding	Bin B
Control	Wafer 217	23.09	Yielding	Bin B
Control	Wafer 218	23.09	Yielding	Bin B
Control	Wafer 219	23.09	Yielding	Bin B
Control	Wafer 220	23.16	Yielding	Bin B
Control	Wafer 221	22.99	Yielding	Bin B
Control	Wafer 222	23.11	Yielding	Bin B
Control	Wafer 223	23.05	Yielding	Bin B
Control	Wafer 224	22.99	Yielding	Bin B
Control	Wafer 225	22.88	Yielding	Bin B
Control	Wafer 226	22.83	Yielding	Bin B
Control	Wafer 227	22.88	Yielding	Bin B
Control	Wafer 228	22.82	Yielding	Bin B

Control	Wafer 229	22.83	Yielding	Bin B
Control	Wafer 230	22.71	Yielding	Bin B
Control	Wafer 231	23.03	Yielding	Bin B
Control	Wafer 232	23.00	Yielding	Bin B
Control	Wafer 233	23.11	Yielding	Bin B
Control	Wafer 234	23.32	Yielding	Bin B
Control	Wafer 235	23.02	Yielding	Bin B
Control	Wafer 236	22.97	Yielding	Bin B
Control	Wafer 237	22.98	Yielding	Bin B
Control	Wafer 238	23.13	Yielding	Bin B
Control	Wafer 239	23.03	Yielding	Bin B
Control	Wafer 240	22.91	Yielding	Bin B
Control	Wafer 241	22.99	Yielding	Bin B
Control	Wafer 242	23.02	Yielding	Bin B
Control	Wafer 243	22.92	Yielding	Bin B
Control	Wafer 244	23.08	Yielding	Bin B
Control	Wafer 245	23.06	Yielding	Bin B
Control	Wafer 246	23.19	Yielding	Bin B
Control	Wafer 247	22.98	Yielding	Bin B
Control	Wafer 248	22.88	Yielding	Bin B
Control	Wafer 249	22.90	Yielding	Bin B
Control	Wafer 250	22.82	Yielding	Bin B
Control	Wafer 251	23.14	Yielding	Bin B
Control	Wafer 252	23.05	Yielding	Bin B
Control	Wafer 253	23.02	Yielding	Bin B
Control	Wafer 254	23.05	Yielding	Bin B
Control	Wafer 255	22.72	Yielding	Bin B
Control	Wafer 256	23.02	Yielding	Bin B
Control	Wafer 257	22.86	Yielding	Bin B
Control	Wafer 258	22.88	Yielding	Bin B
Control	Wafer 259	22.88	Yielding	Bin B
Control	Wafer 260	23.01	Yielding	Bin B
Control	Wafer 261	22.92	Yielding	Bin B
Control	Wafer 262	22.83	Yielding	Bin B
Control	Wafer 263	23.12	Yielding	Bin B
Control	Wafer 264	23.00	Yielding	Bin B
Control	Wafer 265	22.84	Yielding	Bin B
Control	Wafer 266	23.08	Yielding	Bin B
Control	Wafer 267	23.09	Yielding	Bin B
Control	Wafer 268	22.85	Yielding	Bin B
Control	Wafer 269	22.84	Yielding	Bin B
Control	Wafer 270	23.00	Yielding	Bin B
Control	Wafer 271	23.00	Yielding	Bin B
Control	Wafer 272	23.01	Yielding	Bin B

Control	Wafer 273	22.77	Yielding	Bin B
Control	Wafer 274	22.90	Yielding	Bin B
Control	Wafer 275	23.11	Yielding	Bin B
Control	Wafer 276	22.88	Yielding	Bin B
Control	Wafer 277	23.03	Yielding	Bin B
Control	Wafer 278	23.04	Yielding	Bin B
Control	Wafer 279	23.05	Yielding	Bin B
Control	Wafer 280	22.66	Yielding	Bin B
Control	Wafer 281	22.96	Yielding	Bin B
Control	Wafer 282	22.92	Yielding	Bin B
Control	Wafer 283	23.10	Yielding	Bin B
Control	Wafer 284	23.16	Yielding	Bin B
Control	Wafer 285	22.84	Yielding	Bin B
Control	Wafer 286	22.84	Yielding	Bin B
Control	Wafer 287	22.85	Yielding	Bin B
Control	Wafer 288	22.94	Yielding	Bin B
Control	Wafer 289	22.84	Yielding	Bin B
Control	Wafer 290	22.90	Yielding	Bin B
Control	Wafer 291	23.03	Yielding	Bin B
Control	Wafer 292	22.86	Yielding	Bin B
Control	Wafer 293	22.78	Yielding	Bin B
Control	Wafer 294	22.96	Yielding	Bin B
Control	Wafer 295	23.03	Yielding	Bin B
Control	Wafer 296	22.97	Yielding	Bin B
Control	Wafer 297	23.05	Yielding	Bin B
Control	Wafer 298	23.07	Yielding	Bin B
Control	Wafer 299	22.98	Yielding	Bin B
Control	Wafer 300	22.96	Yielding	Bin B
Control	Wafer 301	22.98	Yielding	Bin B
Control	Wafer 302	22.95	Yielding	Bin B
Control	Wafer 303	22.88	Yielding	Bin B
Control	Wafer 304	22.78	Yielding	Bin B
Control	Wafer 305	22.76	Yielding	Bin B
Control	Wafer 306	22.76	Yielding	Bin B
Control	Wafer 307	23.07	Yielding	Bin B
Control	Wafer 308	23.10	Yielding	Bin B
Control	Wafer 309	22.73	Yielding	Bin B
Control	Wafer 310	23.00	Yielding	Bin B
Control	Wafer 311	22.76	Yielding	Bin B
Control	Wafer 312	22.97	Yielding	Bin B
Control	Wafer 313	22.79	Yielding	Bin B
Control	Wafer 314	22.97	Yielding	Bin B
Control	Wafer 315	22.60	Yielding	Bin B
Control	Wafer 316	23.05	Yielding	Bin B

Control	Wafer 317	23.09	Yielding	Bin B
Control	Wafer 318	22.90	Yielding	Bin B
Control	Wafer 319	22.61	Yielding	Bin B
Control	Wafer 320	23.03	Yielding	Bin B
Control	Wafer 321	22.88	Yielding	Bin B
Control	Wafer 322	22.83	Yielding	Bin B
Control	Wafer 323	22.72	Yielding	Bin B
Control	Wafer 324	22.91	Yielding	Bin B
Control	Wafer 325	22.91	Yielding	Bin B
Control	Wafer 326	22.96	Yielding	Bin B
Control	Wafer 327	22.77	Yielding	Bin B
Control	Wafer 328	22.82	Yielding	Bin B
Control	Wafer 329	22.95	Yielding	Bin B
Control	Wafer 330	22.94	Yielding	Bin B
Control	Wafer 331	23.26	Yielding	Bin B
Control	Wafer 332	22.89	Yielding	Bin B
Control	Wafer 333	23.18	Yielding	Bin B
Control	Wafer 334	22.74	Yielding	Bin B
Control	Wafer 335	22.86	Yielding	Bin B
Control	Wafer 336	22.87	Yielding	Bin B
Control	Wafer 337	22.70	Yielding	Bin B
Control	Wafer 338	22.97	Yielding	Bin B
Control	Wafer 339	23.10	Yielding	Bin B
Control	Wafer 340	22.97	Yielding	Bin B
Control	Wafer 341	23.29	Yielding	Bin B
Control	Wafer 342	23.16	Yielding	Bin B
Control	Wafer 343	22.86	Yielding	Bin B
Control	Wafer 344	22.96	Yielding	Bin B
Control	Wafer 345	23.05	Yielding	Bin B
Control	Wafer 346	23.01	Yielding	Bin B
Control	Wafer 347	23.01	Yielding	Bin B
Control	Wafer 348	23.08	Yielding	Bin B
Control	Wafer 349	23.00	Yielding	Bin B
Control	Wafer 350	22.85	Yielding	Bin B
Control	Wafer 351	23.03	Yielding	Bin B
Control	Wafer 352	23.10	Yielding	Bin B
Control	Wafer 353	22.98	Yielding	Bin B
Control	Wafer 354	23.08	Yielding	Bin B
Control	Wafer 355	22.44	Yielding	Bin B
Control	Wafer 356	22.69	Yielding	Bin B
Control	Wafer 357	23.15	Yielding	Bin B
Control	Wafer 358	22.94	Yielding	Bin B
Control	Wafer 359	22.92	Yielding	Bin B
Control	Wafer 360	23.23	Yielding	Bin B

Control	Wafer 361	22.93	Yielding	Bin B
Control	Wafer 362	22.90	Yielding	Bin B
Control	Wafer 363	22.87	Yielding	Bin B
Control	Wafer 364	22.85	Yielding	Bin B
Control	Wafer 365	23.11	Yielding	Bin B
Control	Wafer 366	22.72	Yielding	Bin B
Control	Wafer 367	22.73	Yielding	Bin B
Control	Wafer 368	22.76	Yielding	Bin B
Control	Wafer 369	23.00	Yielding	Bin B
Control	Wafer 370	22.91	Yielding	Bin B
Control	Wafer 371	22.54	Yielding	Bin B
Control	Wafer 372	22.97	Yielding	Bin B
Control	Wafer 373	22.83	Yielding	Bin B
Control	Wafer 374	22.90	Yielding	Bin B
Control	Wafer 375	23.09	Yielding	Bin B
Control	Wafer 376	23.07	Yielding	Bin B
Control	Wafer 377	23.48	Yielding	Bin B
Control	Wafer 378	23.03	Yielding	Bin B
Control	Wafer 379	22.91	Yielding	Bin B
Control	Wafer 380	23.05	Yielding	Bin B
Control	Wafer 381	23.09	Yielding	Bin B
Control	Wafer 382	23.04	Yielding	Bin B
Control	Wafer 383	22.57	Yielding	Bin B
Control	Wafer 384	22.95	Yielding	Bin B
Control	Wafer 385	23.08	Yielding	Bin B
Control	Wafer 386	22.89	Yielding	Bin B
Control	Wafer 387	22.98	Yielding	Bin B
Control	Wafer 388	22.82	Yielding	Bin B
Control	Wafer 389	23.19	Yielding	Bin B
Control	Wafer 390	22.79	Yielding	Bin B
Control	Wafer 391	23.07	Yielding	Bin B
Control	Wafer 392	23.02	Yielding	Bin B
Control	Wafer 393	22.85	Yielding	Bin B
Control	Wafer 394	22.94	Yielding	Bin B
Control	Wafer 395	22.89	Yielding	Bin B
Control	Wafer 396	23.08	Yielding	Bin B
Control	Wafer 397	22.72	Yielding	Bin B
Control	Wafer 398	22.98	Yielding	Bin B
Control	Wafer 399	22.98	Yielding	Bin B
Control	Wafer 400	22.86	Yielding	Bin B
Control	Wafer 401	22.82	Yielding	Bin B
Control	Wafer 402	22.96	Yielding	Bin B
Control	Wafer 403	22.99	Yielding	Bin B
Control	Wafer 404	22.90	Yielding	Bin B

Control	Wafer 405	23.01	Yielding	Bin B
Control	Wafer 406	22.67	Yielding	Bin B
Control	Wafer 407	22.99	Yielding	Bin B
Control	Wafer 408	23.00	Yielding	Bin B
Control	Wafer 409	22.96	Yielding	Bin B
Control	Wafer 410	22.86	Yielding	Bin B
Control	Wafer 411	22.66	Yielding	Bin B
Control	Wafer 412	22.83	Yielding	Bin B
Control	Wafer 413	22.49	Yielding	Bin B
Control	Wafer 414	22.75	Yielding	Bin B
Control	Wafer 415	23.07	Yielding	Bin B
Control	Wafer 416	22.82	Yielding	Bin B
Control	Wafer 417	22.77	Yielding	Bin B
Control	Wafer 418	22.75	Yielding	Bin B
Control	Wafer 419	22.98	Yielding	Bin B
Control	Wafer 420	22.93	Yielding	Bin B
Control	Wafer 421	22.83	Yielding	Bin B
Control	Wafer 422	23.00	Yielding	Bin B
Control	Wafer 423	23.02	Yielding	Bin B
Control	Wafer 424	22.90	Yielding	Bin B
Control	Wafer 425	22.37	Yielding	Bin B
Control	Wafer 426	22.59	Yielding	Bin B
Control	Wafer 427	23.01	Yielding	Bin B
Control	Wafer 428	23.09	Yielding	Bin B
Control	Wafer 429	23.07	Yielding	Bin B
Control	Wafer 430	22.43	Yielding	Bin B
Control	Wafer 431	23.04	Yielding	Bin B
Control	Wafer 432	23.20	Yielding	Bin B
Control	Wafer 433	23.02	Yielding	Bin B
Control	Wafer 434	23.14	Yielding	Bin B
Control	Wafer 435	22.47	Yielding	Bin B
Control	Wafer 436	22.49	Yielding	Bin B
Control	Wafer 437	23.04	Yielding	Bin B
Control	Wafer 438	23.04	Yielding	Bin B
Control	Wafer 439	23.07	Yielding	Bin B
Control	Wafer 440	23.25	Yielding	Bin B
Control	Wafer 441	22.86	Yielding	Bin B
Control	Wafer 442	22.87	Yielding	Bin B
Control	Wafer 443	22.79	Yielding	Bin B
Control	Wafer 444	23.02	Yielding	Bin B
Control	Wafer 445	22.90	Yielding	Bin B
Control	Wafer 446	22.91	Yielding	Bin B
Control	Wafer 447	23.05	Yielding	Bin B
Control	Wafer 448	22.97	Yielding	Bin B

Control	Wafer 449	22.97	Yielding	Bin B
Control	Wafer 450	22.90	Yielding	Bin B
Control	Wafer 451	23.03	Yielding	Bin B
Control	Wafer 452	23.01	Yielding	Bin B
Control	Wafer 453	23.13	Yielding	Bin B
Control	Wafer 454	22.76	Yielding	Bin B
Control	Wafer 455	23.05	Yielding	Bin B
Control	Wafer 456	22.52	Yielding	Bin B
Control	Wafer 457	22.91	Yielding	Bin B
Control	Wafer 458	22.89	Yielding	Bin B
Control	Wafer 459	22.14	Yielding	Bin B
Control	Wafer 460	22.85	Yielding	Bin B
Control	Wafer 461	22.95	Yielding	Bin B
Control	Wafer 462	22.65	Yielding	Bin B
Control	Wafer 463	22.78	Yielding	Bin B
Control	Wafer 464	23.20	Yielding	Bin B
Control	Wafer 465	23.21	Yielding	Bin B
Control	Wafer 466	23.07	Yielding	Bin B
Control	Wafer 467	22.88	Yielding	Bin B
Control	Wafer 468	23.04	Yielding	Bin B
Control	Wafer 469	22.99	Yielding	Bin B
Control	Wafer 470	22.72	Yielding	Bin B
Control	Wafer 471	22.92	Yielding	Bin B
Control	Wafer 472	22.97	Yielding	Bin B
Control	Wafer 473	22.95	Yielding	Bin B
Control	Wafer 474	22.80	Yielding	Bin B
Control	Wafer 475	22.85	Yielding	Bin B
Control	Wafer 476	22.94	Yielding	Bin B
Control	Wafer 477	22.93	Yielding	Bin B
Control	Wafer 478	23.11	Yielding	Bin B
Control	Wafer 479	23.03	Yielding	Bin B
Control	Wafer 480	22.75	Yielding	Bin B
Control	Wafer 481	23.08	Yielding	Bin B
Control	Wafer 482	22.55	Yielding	Bin B
Control	Wafer 483	22.83	Yielding	Bin B
Control	Wafer 484	23.02	Yielding	Bin B
Control	Wafer 485	23.11	Yielding	Bin B
Control	Wafer 486	22.79	Yielding	Bin B
Control	Wafer 487	22.85	Yielding	Bin B
Control	Wafer 488	22.91	Yielding	Bin B
Control	Wafer 489	22.88	Yielding	Bin B
Control	Wafer 490	22.99	Yielding	Bin B
Control	Wafer 491	22.97	Yielding	Bin B
Control	Wafer 492	22.89	Yielding	Bin B

Control	Wafer 493	23.00	Yielding	Bin B
Control	Wafer 494	23.04	Yielding	Bin B
Control	Wafer 495	22.78	Yielding	Bin B
Control	Wafer 496	22.92	Yielding	Bin B
Control	Wafer 497	22.99	Yielding	Bin B
Control	Wafer 498	23.18	Yielding	Bin B
Control	Wafer 499	23.27	Yielding	Bin B
Control	Wafer 500	22.95	Yielding	Bin B
Control	Wafer 501	23.01	Yielding	Bin B
Control	Wafer 502	22.83	Yielding	Bin B
Control	Wafer 503	23.10	Yielding	Bin B
Control	Wafer 504	22.91	Yielding	Bin B
Control	Wafer 505	22.99	Yielding	Bin B
Control	Wafer 506	22.75	Yielding	Bin B
Control	Wafer 507	23.00	Yielding	Bin B
Control	Wafer 508	23.07	Yielding	Bin B
Control	Wafer 509	22.98	Yielding	Bin B
Control	Wafer 510	22.83	Yielding	Bin B
Control	Wafer 511	22.79	Yielding	Bin B
Control	Wafer 512	23.04	Yielding	Bin B
Control	Wafer 513	22.92	Yielding	Bin B
Control	Wafer 514	22.99	Yielding	Bin B
Control	Wafer 515	22.86	Yielding	Bin B
Control	Wafer 516	22.98	Yielding	Bin B
Control	Wafer 517	22.84	Yielding	Bin B
Control	Wafer 518	22.89	Yielding	Bin B
Control	Wafer 519	23.00	Yielding	Bin B
Control	Wafer 520	23.00	Yielding	Bin B
Control	Wafer 521	23.06	Yielding	Bin B
Control	Wafer 522	22.86	Yielding	Bin B
Control	Wafer 523	22.98	Yielding	Bin B
Control	Wafer 524	23.02	Yielding	Bin B
Control	Wafer 525	22.95	Yielding	Bin B
Control	Wafer 526	22.87	Yielding	Bin B
Control	Wafer 527	22.70	Yielding	Bin B
Control	Wafer 528	23.02	Yielding	Bin B
Control	Wafer 529	22.86	Yielding	Bin B
Control	Wafer 530	22.99	Yielding	Bin B
Control	Wafer 531	23.17	Yielding	Bin B
Control	Wafer 532	22.90	Yielding	Bin B
Control	Wafer 533	23.02	Yielding	Bin B
Control	Wafer 534	22.86	Yielding	Bin B
Control	Wafer 535	22.85	Yielding	Bin B
Control	Wafer 536	23.03	Yielding	Bin B

Control	Wafer 537	23.00	Yielding	Bin B
Control	Wafer 538	23.01	Yielding	Bin B
Control	Wafer 539	23.01	Yielding	Bin B
Control	Wafer 540	22.97	Yielding	Bin B
Control	Wafer 541	22.80	Yielding	Bin B
Control	Wafer 542	22.57	Yielding	Bin B
Control	Wafer 543	22.83	Yielding	Bin B
Control	Wafer 544	23.00	Yielding	Bin B
Control	Wafer 545	23.25	Yielding	Bin B
Control	Wafer 546	23.12	Yielding	Bin B
Control	Wafer 547	22.98	Yielding	Bin B
Control	Wafer 548	23.07	Yielding	Bin B
Control	Wafer 549	23.03	Yielding	Bin B
Control	Wafer 550	23.13	Yielding	Bin B
Control	Wafer 551	23.06	Yielding	Bin B
Control	Wafer 552	22.94	Yielding	Bin B
Control	Wafer 553	23.08	Yielding	Bin B
Control	Wafer 554	22.98	Yielding	Bin B
Control	Wafer 555	23.06	Yielding	Bin B
Control	Wafer 556	23.20	Yielding	Bin B
Control	Wafer 557	23.06	Yielding	Bin B
Control	Wafer 558	23.01	Yielding	Bin B
Control	Wafer 559	23.08	Yielding	Bin B
Control	Wafer 560	23.22	Yielding	Bin B
Control	Wafer 561	23.12	Yielding	Bin B
Control	Wafer 562	23.09	Yielding	Bin B
Control	Wafer 563	22.95	Yielding	Bin B
Control	Wafer 564	22.86	Yielding	Bin B
Control	Wafer 565	23.05	Yielding	Bin B
Control	Wafer 566	23.14	Yielding	Bin B
Control	Wafer 567	23.14	Yielding	Bin B
Control	Wafer 568	23.18	Yielding	Bin B
Control	Wafer 569	22.98	Yielding	Bin B
Control	Wafer 570	23.01	Yielding	Bin B
Control	Wafer 571	23.07	Yielding	Bin B
Control	Wafer 572	22.82	Yielding	Bin B
Control	Wafer 573	22.80	Yielding	Bin B
Control	Wafer 574	23.04	Yielding	Bin B
Control	Wafer 575	23.11	Yielding	Bin B
Control	Wafer 576	22.94	Yielding	Bin B
Control	Wafer 577	23.05	Yielding	Bin B
Control	Wafer 578	22.93	Yielding	Bin B
Control	Wafer 579	22.91	Yielding	Bin B
Control	Wafer 580	23.04	Yielding	Bin B

Control	Wafer 581	22.71	Yielding	Bin B
Control	Wafer 582	22.12	Yielding	Bin B
Control	Wafer 583	23.01	Yielding	Bin B
Control	Wafer 584	22.95	Yielding	Bin B
Control	Wafer 585	23.18	Yielding	Bin B
Control	Wafer 586	23.28	Yielding	Bin B
Control	Wafer 587	23.28	Yielding	Bin B
Control	Wafer 588	22.81	Yielding	Bin B
Control	Wafer 589	23.10	Yielding	Bin B
Control	Wafer 590	23.06	Yielding	Bin B
Control	Wafer 591	23.17	Yielding	Bin B
Control	Wafer 592	23.10	Yielding	Bin B
Control	Wafer 593	22.92	Yielding	Bin B
Control	Wafer 594	23.03	Yielding	Bin B
Control	Wafer 595	22.89	Yielding	Bin B
Control	Wafer 596	23.08	Yielding	Bin B
Control	Wafer 597	23.15	Yielding	Bin B
Control	Wafer 598	23.14	Yielding	Bin B
Control	Wafer 599	23.09	Yielding	Bin B
Control	Wafer 600	23.09	Yielding	Bin B
Control	Wafer 601	22.53	Yielding	Bin B
Control	Wafer 602	22.89	Yielding	Bin B
Control	Wafer 603	22.72	Yielding	Bin B
Control	Wafer 604	22.96	Yielding	Bin B
Control	Wafer 605	22.98	Yielding	Bin B
Control	Wafer 606	23.28	Yielding	Bin B
Control	Wafer 607	23.15	Yielding	Bin B
Control	Wafer 608	23.08	Yielding	Bin B
Control	Wafer 609	22.93	Yielding	Bin B
Control	Wafer 610	23.07	Yielding	Bin B
Control	Wafer 611	23.01	Yielding	Bin B
Control	Wafer 612	23.11	Yielding	Bin B
Control	Wafer 613	23.03	Yielding	Bin B
Control	Wafer 614	22.74	Yielding	Bin B
Control	Wafer 615	22.44	Yielding	Bin B
Control	Wafer 616	23.02	Yielding	Bin B
Control	Wafer 617	22.80	Yielding	Bin B
Control	Wafer 618	22.94	Yielding	Bin B
Control	Wafer 619	22.79	Yielding	Bin B
Control	Wafer 620	22.62	Yielding	Bin B
Control	Wafer 621	22.89	Yielding	Bin B
Control	Wafer 622	22.93	Yielding	Bin B
Control	Wafer 623	22.98	Yielding	Bin B
Control	Wafer 624	22.97	Yielding	Bin B

Control	Wafer 625	23.16	Yielding	Bin B
Control	Wafer 626	22.48	Yielding	Bin B
Control	Wafer 627	22.27	Yielding	Bin B
Control	Wafer 628	22.82	Yielding	Bin B
Control	Wafer 629	22.81	Yielding	Bin B
Control	Wafer 630	22.83	Yielding	Bin B
Control	Wafer 631	22.81	Yielding	Bin B
Control	Wafer 632	22.58	Yielding	Bin B
Control	Wafer 633	22.83	Yielding	Bin B
Control	Wafer 634	22.83	Yielding	Bin B
Control	Wafer 635	23.08	Yielding	Bin B
Control	Wafer 636	23.15	Yielding	Bin B
Control	Wafer 637	22.98	Yielding	Bin B
Control	Wafer 638	22.83	Yielding	Bin B
Control	Wafer 639	22.84	Yielding	Bin B
Control	Wafer 640	22.79	Yielding	Bin B
Control	Wafer 641	22.86	Yielding	Bin B
Control	Wafer 642	22.72	Yielding	Bin B
Control	Wafer 643	23.02	Yielding	Bin B
Control	Wafer 644	22.95	Yielding	Bin B
Control	Wafer 645	23.07	Yielding	Bin B
Control	Wafer 646	23.07	Yielding	Bin B
Control	Wafer 647	22.96	Yielding	Bin B
Control	Wafer 648	23.07	Yielding	Bin B
Control	Wafer 649	22.55	Yielding	Bin B
Control	Wafer 650	22.79	Yielding	Bin B
Control	Wafer 651	22.28	Yielding	Bin B
Control	Wafer 652	22.97	Yielding	Bin B
Control	Wafer 653	22.96	Yielding	Bin B
Control	Wafer 654	22.78	Yielding	Bin B
Control	Wafer 655	22.76	Yielding	Bin B
Control	Wafer 656	22.79	Yielding	Bin B
Control	Wafer 657	22.64	Yielding	Bin B
Control	Wafer 658	22.90	Yielding	Bin B
Control	Wafer 659	22.98	Yielding	Bin B
Control	Wafer 660	22.96	Yielding	Bin B
Control	Wafer 661	22.83	Yielding	Bin B
Control	Wafer 662	22.54	Yielding	Bin B
Control	Wafer 663	22.87	Yielding	Bin B
Control	Wafer 664	22.77	Yielding	Bin B
Control	Wafer 665	22.98	Yielding	Bin B
Control	Wafer 666	22.99	Yielding	Bin B
Control	Wafer 667	22.82	Yielding	Bin B
Control	Wafer 668	23.04	Yielding	Bin B

Control	Wafer 669	22.51	Yielding	Bin B
Control	Wafer 670	22.88	Yielding	Bin B
Control	Wafer 671	22.94	Yielding	Bin B
Control	Wafer 672	22.98	Yielding	Bin B
Control	Wafer 673	22.91	Yielding	Bin B
Control	Wafer 674	22.66	Yielding	Bin B
Control	Wafer 675	22.01	Non-yielding	Bin B
Control	Wafer 676	23.00	Yielding	Bin B
Control	Wafer 677	22.98	Yielding	Bin B
Control	Wafer 678	22.80	Yielding	Bin B
Control	Wafer 679	22.96	Yielding	Bin B
Control	Wafer 680	22.96	Yielding	Bin B
Control	Wafer 681	22.95	Yielding	Bin B
Control	Wafer 682	22.71	Yielding	Bin B
Control	Wafer 683	22.80	Yielding	Bin B
Control	Wafer 684	22.60	Yielding	Bin B
Control	Wafer 685	22.81	Yielding	Bin B
Control	Wafer 686	22.78	Yielding	Bin B
Control	Wafer 687	22.88	Yielding	Bin B
Control	Wafer 688	23.08	Yielding	Bin B
Control	Wafer 689	22.76	Yielding	Bin B
Control	Wafer 690	22.89	Yielding	Bin B
Control	Wafer 691	21.14	Non-yielding	Bin B
Control	Wafer 692	22.81	Yielding	Bin B
Control	Wafer 693	22.85	Yielding	Bin B
Control	Wafer 694	22.87	Yielding	Bin B
Control	Wafer 695	22.87	Yielding	Bin B
Control	Wafer 696	22.89	Yielding	Bin B
Control	Wafer 697	23.02	Yielding	Bin B
Control	Wafer 698	23.03	Yielding	Bin B
Control	Wafer 699	23.01	Yielding	Bin B
Control	Wafer 700	22.92	Yielding	Bin B
Control	Wafer 701	22.96	Yielding	Bin B
Control	Wafer 702	22.65	Yielding	Bin B
Control	Wafer 703	22.91	Yielding	Bin B
Control	Wafer 704	22.81	Yielding	Bin B
Control	Wafer 705	21.97	Non-yielding	Bin B
Control	Wafer 706	23.17	Yielding	Bin B
Control	Wafer 707	22.14	Yielding	Bin B
Control	Wafer 708	22.63	Yielding	Bin B
Control	Wafer 709	22.39	Yielding	Bin B
Control	Wafer 710	22.94	Yielding	Bin B
Control	Wafer 711	22.84	Yielding	Bin B
Control	Wafer 712	22.77	Yielding	Bin B

Control	Wafer 713	23.06	Yielding	Bin B
Control	Wafer 714	22.89	Yielding	Bin B
Control	Wafer 715	22.56	Yielding	Bin B
Control	Wafer 716	22.77	Yielding	Bin B
Control	Wafer 717	22.64	Yielding	Bin B
Control	Wafer 718	22.69	Yielding	Bin B
Control	Wafer 719	22.15	Yielding	Bin B
Control	Wafer 720	22.41	Yielding	Bin B
Control	Wafer 721	22.28	Yielding	Bin B
Control	Wafer 722	22.74	Yielding	Bin B
Control	Wafer 723	22.64	Yielding	Bin B
Control	Wafer 724	22.58	Yielding	Bin B
Control	Wafer 725	22.94	Yielding	Bin B
Control	Wafer 726	22.90	Yielding	Bin B
Control	Wafer 727	22.80	Yielding	Bin B
Control	Wafer 728	23.41	Yielding	Bin B
Control	Wafer 729	22.99	Yielding	Bin B
Control	Wafer 730	22.93	Yielding	Bin B
Control	Wafer 731	23.00	Yielding	Bin B
Control	Wafer 732	22.95	Yielding	Bin B
Control	Wafer 733	22.80	Yielding	Bin B
Control	Wafer 734	22.90	Yielding	Bin B
Control	Wafer 735	22.83	Yielding	Bin B
Control	Wafer 736	22.61	Yielding	Bin B
Control	Wafer 737	23.03	Yielding	Bin B
Control	Wafer 738	23.28	Yielding	Bin B
Control	Wafer 739	23.04	Yielding	Bin B
Control	Wafer 740	22.38	Yielding	Bin B
Control	Wafer 741	22.62	Yielding	Bin B
Control	Wafer 742	22.67	Yielding	Bin B
Control	Wafer 743	22.92	Yielding	Bin B
Control	Wafer 744	22.99	Yielding	Bin B
Control	Wafer 745	22.91	Yielding	Bin B
Control	Wafer 746	22.95	Yielding	Bin B
Control	Wafer 747	22.95	Yielding	Bin B
Control	Wafer 748	22.90	Yielding	Bin B
Control	Wafer 749	22.49	Yielding	Bin B
Control	Wafer 750	23.05	Yielding	Bin B
Control	Wafer 751	22.87	Yielding	Bin B
Control	Wafer 752	22.27	Yielding	Bin B
Control	Wafer 753	22.21	Yielding	Bin B
Control	Wafer 754	22.68	Yielding	Bin B
Control	Wafer 755	23.00	Yielding	Bin B
Control	Wafer 756	22.83	Yielding	Bin B

Control	Wafer 757	22.97	Yielding	Bin B
Control	Wafer 758	22.89	Yielding	Bin B
Control	Wafer 759	22.69	Yielding	Bin B
Control	Wafer 760	22.78	Yielding	Bin B
Control	Wafer 761	22.82	Yielding	Bin B
Control	Wafer 762	23.00	Yielding	Bin B
Control	Wafer 763	22.96	Yielding	Bin B
Control	Wafer 764	22.41	Yielding	Bin B
Control	Wafer 765	23.06	Yielding	Bin B
Control	Wafer 766	22.41	Yielding	Bin B
Control	Wafer 767	22.34	Yielding	Bin B
Control	Wafer 768	22.39	Yielding	Bin B
Control	Wafer 769	22.77	Yielding	Bin B
Control	Wafer 770	22.11	Yielding	Bin B
Control	Wafer 771	22.80	Yielding	Bin B
Control	Wafer 772	22.51	Yielding	Bin B
Control	Wafer 773	22.88	Yielding	Bin B
Control	Wafer 774	22.80	Yielding	Bin B
Control	Wafer 775	22.59	Yielding	Bin B
Control	Wafer 776	22.99	Yielding	Bin B
Control	Wafer 777	22.36	Yielding	Bin B
Control	Wafer 778	22.43	Yielding	Bin B
Control	Wafer 779	22.61	Yielding	Bin B
Control	Wafer 780	22.71	Yielding	Bin B
Control	Wafer 781	22.81	Yielding	Bin B
Control	Wafer 782	22.82	Yielding	Bin B
Control	Wafer 783	22.90	Yielding	Bin B
Control	Wafer 784	22.71	Yielding	Bin B
Control	Wafer 785	22.89	Yielding	Bin B
Control	Wafer 786	22.79	Yielding	Bin B
Control	Wafer 787	22.74	Yielding	Bin B
Control	Wafer 788	23.05	Yielding	Bin B
Control	Wafer 789	22.66	Yielding	Bin B
Control	Wafer 790	22.70	Yielding	Bin B
Control	Wafer 791	23.04	Yielding	Bin B
Control	Wafer 792	23.00	Yielding	Bin B
Control	Wafer 793	22.95	Yielding	Bin B
Control	Wafer 794	23.08	Yielding	Bin B
Control	Wafer 795	22.88	Yielding	Bin B
Control	Wafer 796	22.98	Yielding	Bin B
Control	Wafer 797	22.79	Yielding	Bin B
Control	Wafer 798	22.84	Yielding	Bin B
Control	Wafer 799	22.88	Yielding	Bin B
Control	Wafer 800	22.91	Yielding	Bin B

Control	Wafer 801	22.97	Yielding	Bin B
Control	Wafer 802	22.04	Non-yielding	Bin B
Control	Wafer 803	22.32	Yielding	Bin B
Control	Wafer 804	22.61	Yielding	Bin B
Control	Wafer 805	22.70	Yielding	Bin B
Control	Wafer 806	22.86	Yielding	Bin B
Control	Wafer 807	22.66	Yielding	Bin B
Control	Wafer 808	22.64	Yielding	Bin B
Control	Wafer 809	22.53	Yielding	Bin B
Control	Wafer 810	22.93	Yielding	Bin B
Control	Wafer 811	22.74	Yielding	Bin B
Control	Wafer 812	22.92	Yielding	Bin B
Control	Wafer 813	22.47	Yielding	Bin B
Control	Wafer 814	22.59	Yielding	Bin B
Control	Wafer 815	22.82	Yielding	Bin B
Control	Wafer 816	22.23	Yielding	Bin B
Control	Wafer 817	22.48	Yielding	Bin B
Control	Wafer 818	22.82	Yielding	Bin B
Control	Wafer 819	22.60	Yielding	Bin B
Control	Wafer 820	22.83	Yielding	Bin B
Control	Wafer 821	22.45	Yielding	Bin B
Control	Wafer 822	22.48	Yielding	Bin B
Control	Wafer 823	22.88	Yielding	Bin B
Control	Wafer 824	22.74	Yielding	Bin B
Control	Wafer 825	22.93	Yielding	Bin B
Control	Wafer 826	22.72	Yielding	Bin B
Control	Wafer 827	22.56	Yielding	Bin B
Control	Wafer 828	22.79	Yielding	Bin B
Control	Wafer 829	23.00	Yielding	Bin B
Control	Wafer 830	22.06	Yielding	Bin B
Control	Wafer 831	22.79	Yielding	Bin B
Control	Wafer 832	22.80	Yielding	Bin B
Control	Wafer 833	22.17	Yielding	Bin B
Control	Wafer 834	21.98	Non-yielding	Bin B
Control	Wafer 835	22.72	Yielding	Bin B
Control	Wafer 836	22.29	Yielding	Bin B
Control	Wafer 837	22.69	Yielding	Bin B
Control	Wafer 838	22.89	Yielding	Bin B
Control	Wafer 839	22.82	Yielding	Bin B
Control	Wafer 840	23.21	Yielding	Bin B
Control	Wafer 841	22.50	Yielding	Bin B
Control	Wafer 842	22.82	Yielding	Bin B
Control	Wafer 843	23.02	Yielding	Bin B
Control	Wafer 844	22.51	Yielding	Bin B

Control	Wafer 845	22.58	Yielding	Bin C
Control	Wafer 846	22.91	Yielding	Bin C
Control	Wafer 847	22.60	Yielding	Bin C
Control	Wafer 848	22.85	Yielding	Bin C
Control	Wafer 849	22.82	Yielding	Bin C
Control	Wafer 850	22.87	Yielding	Bin C
Control	Wafer 851	22.93	Yielding	Bin C
Control	Wafer 852	22.75	Yielding	Bin C
Control	Wafer 853	22.98	Yielding	Bin C
Control	Wafer 854	22.51	Yielding	Bin C
Control	Wafer 855	22.89	Yielding	Bin C
Control	Wafer 856	22.58	Yielding	Bin C
Control	Wafer 857	22.79	Yielding	Bin C
Control	Wafer 858	22.80	Yielding	Bin C
Control	Wafer 859	22.38	Yielding	Bin C
Control	Wafer 860	22.35	Yielding	Bin C
Control	Wafer 861	22.60	Yielding	Bin C
Control	Wafer 862	22.43	Yielding	Bin C
Control	Wafer 863	22.72	Yielding	Bin C
Control	Wafer 864	22.28	Yielding	Bin C
Control	Wafer 865	22.68	Yielding	Bin C
Control	Wafer 866	23.08	Yielding	Bin C
Control	Wafer 867	23.08	Yielding	Bin C
Control	Wafer 868	23.00	Yielding	Bin C
Control	Wafer 869	22.84	Yielding	Bin C
Control	Wafer 870	22.81	Yielding	Bin C
Control	Wafer 871	22.80	Yielding	Bin C
Control	Wafer 872	22.92	Yielding	Bin C
Control	Wafer 873	23.05	Yielding	Bin C
Control	Wafer 874	23.13	Yielding	Bin C
Control	Wafer 875	22.78	Yielding	Bin C
Control	Wafer 876	22.50	Yielding	Bin C
Control	Wafer 877	22.28	Yielding	Bin C
Control	Wafer 878	22.56	Yielding	Bin C
Control	Wafer 879	22.56	Yielding	Bin C
Control	Wafer 880	22.54	Yielding	Bin C
Control	Wafer 881	22.68	Yielding	Bin C
Control	Wafer 882	22.75	Yielding	Bin C
Control	Wafer 883	22.77	Yielding	Bin C
Control	Wafer 884	22.44	Yielding	Bin C
Control	Wafer 885	22.78	Yielding	Bin C
Control	Wafer 886	22.67	Yielding	Bin C
Control	Wafer 887	22.09	Yielding	Bin C
Control	Wafer 888	22.88	Yielding	Bin C

Control	Wafer 889	22.69	Yielding	Bin C
Control	Wafer 890	23.02	Yielding	Bin C
Control	Wafer 891	22.77	Yielding	Bin C
Control	Wafer 892	22.75	Yielding	Bin C
Control	Wafer 893	22.09	Yielding	Bin C
Control	Wafer 894	22.63	Yielding	Bin C
Control	Wafer 895	22.50	Yielding	Bin C
Control	Wafer 896	22.59	Yielding	Bin C
Control	Wafer 897	22.33	Yielding	Bin C
Control	Wafer 898	22.64	Yielding	Bin C
Control	Wafer 899	22.73	Yielding	Bin C
Control	Wafer 900	22.79	Yielding	Bin C
Control	Wafer 901	22.70	Yielding	Bin C
Control	Wafer 902	22.72	Yielding	Bin C
Control	Wafer 903	22.00	Non-yielding	Bin C
Control	Wafer 904	22.49	Yielding	Bin C
Control	Wafer 905	22.26	Yielding	Bin C
Control	Wafer 906	22.52	Yielding	Bin C
Control	Wafer 907	21.75	Non-yielding	Bin C
Control	Wafer 908	22.90	Yielding	Bin C
Control	Wafer 909	23.06	Yielding	Bin C
Control	Wafer 910	22.87	Yielding	Bin C
Control	Wafer 911	23.05	Yielding	Bin C
Control	Wafer 912	22.95	Yielding	Bin C
Control	Wafer 913	22.16	Yielding	Bin C
Control	Wafer 914	21.99	Non-yielding	Bin C
Control	Wafer 915	22.83	Yielding	Bin C
Control	Wafer 916	22.80	Yielding	Bin C
Control	Wafer 917	22.95	Yielding	Bin C
Control	Wafer 918	22.87	Yielding	Bin C
Control	Wafer 919	22.88	Yielding	Bin C
Control	Wafer 920	22.79	Yielding	Bin C
Control	Wafer 921	22.56	Yielding	Bin C
Control	Wafer 922	23.09	Yielding	Bin C
Control	Wafer 923	22.48	Yielding	Bin C
Control	Wafer 924	22.15	Yielding	Bin C
Control	Wafer 925	22.78	Yielding	Bin C
Control	Wafer 926	22.63	Yielding	Bin C
Control	Wafer 927	22.64	Yielding	Bin C
Control	Wafer 928	22.63	Yielding	Bin C
Control	Wafer 929	22.39	Yielding	Bin C
Control	Wafer 930	22.47	Yielding	Bin C
Control	Wafer 931	22.53	Yielding	Bin C
Control	Wafer 932	22.69	Yielding	Bin C

Control	Wafer 933	22.68	Yielding	Bin C
Control	Wafer 934	22.80	Yielding	Bin C
Control	Wafer 935	22.72	Yielding	Bin C
Control	Wafer 936	22.74	Yielding	Bin C
Control	Wafer 937	22.88	Yielding	Bin C
Control	Wafer 938	22.51	Yielding	Bin C
Control	Wafer 939	22.48	Yielding	Bin C
Control	Wafer 940	22.97	Yielding	Bin C
Control	Wafer 941	22.36	Yielding	Bin C
Control	Wafer 942	22.52	Yielding	Bin C
Control	Wafer 943	22.19	Yielding	Bin C
Control	Wafer 944	22.81	Yielding	Bin C
Control	Wafer 945	22.89	Yielding	Bin C
Control	Wafer 946	22.75	Yielding	Bin C
Control	Wafer 947	22.60	Yielding	Bin C
Control	Wafer 948	22.67	Yielding	Bin C
Control	Wafer 949	23.07	Yielding	Bin C
Control	Wafer 950	23.08	Yielding	Bin C
Control	Wafer 951	22.94	Yielding	Bin C
Control	Wafer 952	22.81	Yielding	Bin C
Control	Wafer 953	22.93	Yielding	Bin C
Control	Wafer 954	22.80	Yielding	Bin C
Control	Wafer 955	22.31	Yielding	Bin C
Control	Wafer 956	22.84	Yielding	Bin C
Control	Wafer 957	22.65	Yielding	Bin C
Control	Wafer 958	22.34	Yielding	Bin C
Control	Wafer 959	22.95	Yielding	Bin C
Control	Wafer 960	22.17	Yielding	Bin C
Control	Wafer 961	22.55	Yielding	Bin C
Control	Wafer 962	23.02	Yielding	Bin C
Control	Wafer 963	22.92	Yielding	Bin C
Control	Wafer 964	21.83	Non-yielding	Bin C
Control	Wafer 965	22.70	Yielding	Bin C
Control	Wafer 966	22.96	Yielding	Bin C
Control	Wafer 967	22.81	Yielding	Bin C
Control	Wafer 968	22.98	Yielding	Bin C
Control	Wafer 969	23.09	Yielding	Bin C
Control	Wafer 970	22.91	Yielding	Bin C
Control	Wafer 971	23.10	Yielding	Bin C
Control	Wafer 972	22.81	Yielding	Bin C
Control	Wafer 973	23.03	Yielding	Bin C
Control	Wafer 974	22.94	Yielding	Bin C
Control	Wafer 975	23.11	Yielding	Bin C
Control	Wafer 976	23.09	Yielding	Bin C

Control	Wafer 977	23.00	Yielding	Bin C
Control	Wafer 978	23.14	Yielding	Bin C
Control	Wafer 979	23.21	Yielding	Bin C
Control	Wafer 980	22.83	Yielding	Bin C
Control	Wafer 981	22.96	Yielding	Bin C
Control	Wafer 982	23.02	Yielding	Bin C
Control	Wafer 983	23.02	Yielding	Bin C
Control	Wafer 984	22.94	Yielding	Bin C
Control	Wafer 985	23.11	Yielding	Bin C
Control	Wafer 986	23.16	Yielding	Bin C
Control	Wafer 987	23.02	Yielding	Bin C
Control	Wafer 988	23.05	Yielding	Bin C
Control	Wafer 989	23.25	Yielding	Bin C
Control	Wafer 990	23.03	Yielding	Bin D
Control	Wafer 991	22.88	Yielding	Bin D
Control	Wafer 992	22.79	Yielding	Bin D
Control	Wafer 993	22.62	Yielding	Bin D
Control	Wafer 994	22.94	Yielding	Bin D
Control	Wafer 995	23.11	Yielding	Bin D
Control	Wafer 996	22.83	Yielding	Bin D
Control	Wafer 997	22.80	Yielding	Bin D
Control	Wafer 998	22.90	Yielding	Bin D
Control	Wafer 999	23.01	Yielding	Bin D
Control	Wafer 1000	22.71	Yielding	Bin D