

## WORK-FUNCTION TUNING ON ANALOGUE PROPERTIES OF JUNCTION-LESS STRAINED DG-MOSFET

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### Abstract

This paper discusses an extensive investigation on the influence of work-function ( $WF$ ) tuning on analogue properties of the n-type junction-less strained double-gate MOSFET. The investigation on the device has been conducted with fixed level of input parameters operating in saturation mode by taking the dependency of analogue properties on the  $WF$  tuning into account. Numerical simulation was performed using industrial-based process/device simulator, Silvaco TCAD tools. The simulation results revealed that analogue properties of the device such as transconductance ( $g_m$ ), transconductance generation factor ( $TGF$ ) and output conductance ( $g_d$ ), output impedance ( $r_o$ ) and intrinsic gain ( $A_V$ ) varies erratically as  $WF$  increases from 4.1 to 4.8 eV. However, the early voltage ( $V_{EA}$ ) of the device decreases with increase in  $WF$  of metal gate. Despite scaling the physical gate length to 6nm, the device exhibits decent analogue qualities with  $g_m$  and  $A_V$  values of 3.56 mS/m and 37.14 dB, respectively.

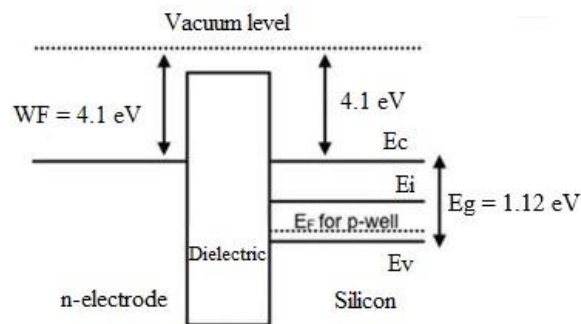
Keywords: Early voltage, Intrinsic gain, Output conductance, Transconductance.

## 1. Introduction

The supply voltage ( $V_{DD}$ ) must be reduced to accommodate the low power requirement of metal-oxide- semiconductor field-effect transistors (MOSFETs). Furthermore, substantially small subthreshold swing ( $SS$ ) is required to sustain high on-current ( $I_{ON}$ ) despite the  $V_{DD}$  reduction. However, it is widely known that the  $SS$  of a MOSFET is notoriously difficult to minimize at room temperature, owing to the fact that its operation is reliant on thermionic carrier injection [1]. Junction-less ultrathin channel transistors may be a potential option for a next-generation low-power device due to its low  $SS$  at room temperature and strong complementary MOS (CMOS) process compatibility [2-5]. Nevertheless, there are still several hurdles to overcome before commercialization, including leakage current from unwanted drain-side tunnelling and poor  $I_{ON}$ .

To overcome these drawbacks, junction-less double gate strained MOSFET have been proposed, as the device not only reduces tunnelling resistance by using material with smaller band gap, such as SiGe, as a channel material, but also suppresses leakage current by forming the two pair front and bottom-sided ultrathin Si layers sandwiched the SiGe layer. The ultrathin Si layer must be extensively doped to allow for sufficient current flow to power the device. In sub-micron transistor technologies, process variables such as, work-function variation, random doping fluctuation and line edge roughness have been identified as major concerns [6].

According to the International Technology Roadmap for Semiconductors (ITRS) High Performance (HP) suggested approach, metal gate is the most effective high performance booster owing to its minimal equivalent oxide thickness ( $EOT$ ) and might dominate the industry prior to 2018. Accordingly, it is critical to choose a gate material with the proper  $WF$ . The gate  $WF$  variation associated with the conduction band for bulk n-channel device spans from 4.1 to 4.8 eV. The function of the gate relies on the type of metal utilized. Metal may be inferior or superior to highly-doped poly (either n+ or p+).  $WF$  controls semiconductor device energy band. For instance, a greater work function inclines the energy band upwards. To achieve a low threshold voltage, a modest  $WF$  gap between gate and channel material should be attained as depicted in Fig. 1.



**Fig. 1. Energy diagrams for n-channel device.**

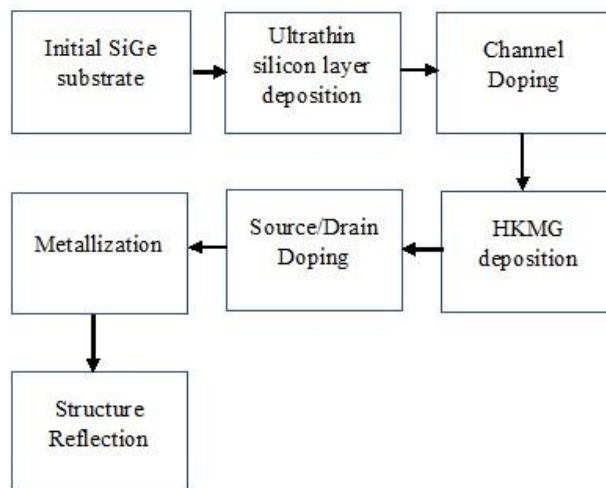
Kumar et al. (2020) have reported that an excellent immunity from short channel effects has been realized with implementation of *high-k dielectrics* with multiple metal-gate work-functions. Material with a high dielectric constant such as Hafnium

dioxide ( $\text{HfO}_2$ ) demonstrates minimal leakage current as compared to traditional  $\text{SiO}_2$ . The enhancement of  $DIBL$ ,  $V_{th}$  roll-off and  $SS$  is directly contributed by the metal-gate work-function tuning [7]. Dai et al. [5] have also reported that tuning the metal-gate work-function is the key factor in achieving better output properties of junction-less transistor. Rao et al. [8] explored strain silicon channel to enhance the analogue performances of triple material junction-less MOSFE. Improvement in device performance were attained by increasing the values of strain, positive fixed charge density, and oxide thickness in the weak inversion area, and likewise in the region above the threshold voltage. Recent study done by Singh et al. [9] realizes ultra-steep and process variation resistant configuration in which the gate stack ferroelectric material is employed in conjunction with a high- $k$  gate dielectric  $\text{HfO}_2/\text{TiO}_2$ . It demonstrates that the work-function gap between the source/drain electrodes and the silicon generates electrostatic doping, subsequently generating major effects on analogue performances.

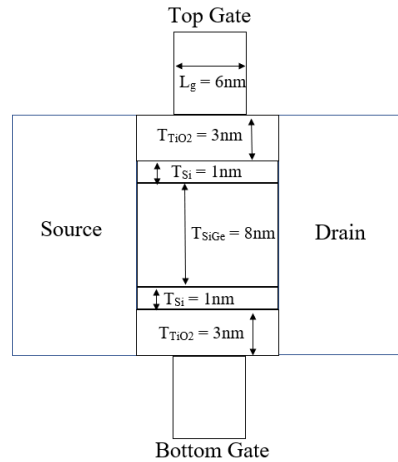
Apart from that, the dominant dependency on saturation drain voltage indicates the inversion charges from drain region pinned channel potential influenced by the work-function variations [6]. Previous study has been conducted in investigating the impact of work-function variation on electrostatic and RF properties of n-type junction-less strained double-gate MOSFET [10]. However, this paper particularly emphasizes on the influence of work-function tuning on analogue properties of the n-type junction-less strained double-gate MOSFET.

## 2. Device Structure and Simulation

The process simulation flow and cross-sectional layout for a n-type junction-less strained double-gate MOSFET device are illustrated in Figs. 2 and 3 respectively. In this device, the main substrate was made of  $\text{SiGe}$  material (with  $\text{Ge}$  content of 20%) with an 8nm thickness, which was chosen primarily because it has a higher lattice constant than silicon ( $\text{Si}$ ). A strained  $\text{Si}$  layer was then formed by depositing an ultrathin  $\text{Si}$  layer (1nm) on top of the initial  $\text{SiGe}$  layer. It was the stretched  $\text{Si}$  atoms that exerted a strain on the  $\text{Si}$  layer which attempted to align themselves with the  $\text{SiGe}$  atoms.



**Fig. 2. Simulation process flow of n-type junction-less strained double-gate MOSFET.**



**Fig. 3. Layout of n-type junction-less strained double-gate MOSFET.**

Following that, both strained *Si* and *SiGe* layers were significantly implanted with an Arsenic dosage of  $1 \times 10^{17} \text{ cm}^{-3}$  (n-type). It was decided to use a tungsten silicide (*WSi<sub>x</sub>*) layer as the gate material because of its remarkably adjustable *WF* [11]. Both top and bottom gate layout was designed for increased controllability over the stressed channel, hence boosting the mobility of carriers. The gate length ( $L_g$ ) of the proposed device was scaled to around 6nm, which is a significant reduction in size. An additional *WSi<sub>x</sub>* layer was formed on top of the insulator to minimize any flaws at the dielectric/gate boundary that might lead to threshold voltage ( $V_{TH}$ ) pinning.

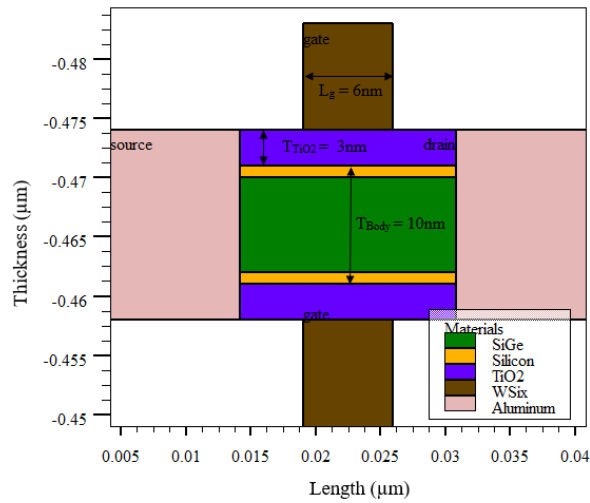
Titanium dioxide ( $\text{TiO}_2$ ) was chosen as a gate dielectric (insulator) mostly due to its high dielectric permittivity ( $\sim 85 \text{ eV}$ ). Using  $\text{TiO}_2$  as the gate dielectric opened the door to the potential of using a thicker dielectric for future metal-gate technology. In order to minimize leakage while maintaining the same capacitance as the silicon dioxide layer (3.9 eV), it is possible to scale the  $\text{TiO}_2$  layer (85eV) to nearly 21 times its thickness relative to silicon dioxide (3.9eV). Equivalent oxide thickness (*EOT*) is a standard measurement used to determine the needed thickness of *SiO<sub>2</sub>* layer in order to generate the same effect as a specific high-*k* dielectric material with the same dielectric constant. As a result, the *EOT* for the device can be calculated as follows:

$$EOT = \left[ \frac{\epsilon_{SiO_2}}{\epsilon_{high-k}} \right] T_{high-k} \quad (1)$$

where  $\epsilon_{SiO_2}$  is the permittivity of *SiO<sub>2</sub>* (3.9 eV), the permittivity of high-*k* dielectric is denoted by  $\epsilon_{high-k}$ , while the physical thickness of high-*k* dielectric is denoted by  $T_{high-k}$ .

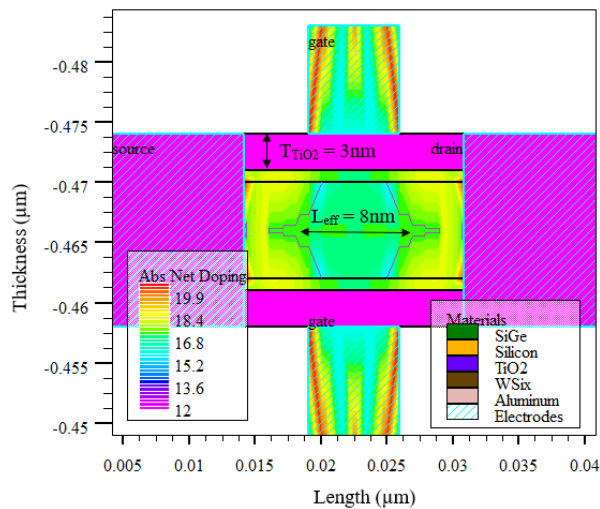
Source/drain (S/D) implantation was the next procedure performed, in which similar type of dopant is utilized during the channel doping procedure (Arsenic). Such a procedure was intended to produce the N N+ N configuration, which would prevent any junctions from forming between the channel and S/D regions (Junction-less). In order to ensure a high drive current, the strained thin film was heavily reliant on the

high implant concentration, which was made possible by the junction-less structure. The metallization was then carried out for contact formation. Etching away the undesirable aluminum layer, both contacts and electrodes are formed desirably. The device layout was then mirrored in both top and bottom axis to result in n-type junction-less strained DG-MOSFET structure, as depicted in Fig. 4.



**Fig. 4. 2D structure of n-type junction-less strained double-gate MOSFET.**

By using the 2D numerical ATLAS simulator [12], the device properties for the n-type junction-less strained DG-MOSFET device were extracted and compared with each other. A constant drain-to-source voltage of  $V_{ds} = 0.5$  V (which is half the supply voltage, or  $V_{DD}/2$ ) was used to investigate the influence of *WF* tuning on analogue properties. This was done to take into account the device subthreshold characteristics. Figure 5 shows the doping profile across the device, indicating the net doping for *SiGe*, *Si*,  $TiO_2$ ,  $WSi_x$  and aluminum.



**Fig. 5. Contour mode of junction-less strained double-gate MOSFET.**

### 3. Effect of Work-function on Analogue Properties

From the perspective of design consideration for analogue circuits, some crucial analogue properties of junction-less strained DG-MOSFET such as transconductance ( $g_m$ ), transconductance generation factor ( $TGF$ ), output conductance ( $g_d$ ), output impedance ( $r_o$ ), early voltage ( $V_{EA}$ ) and intrinsic gain ( $A_V$ ) are required to be intensively investigated. Transconductance ( $g_m$ ) is a very important characteristic that computes the amplifier's gain. It is used to indicate how minimum the  $V_{gs}$  is required to increase the  $I_{ds}$  of a transistor which can be mathematically described as:

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}} \quad (2)$$

Figure 6 shows a plot of  $g_m$  as a function of  $V_{gs}$  at a fixed  $V_{ds} = 0.5V$  for  $WF$  ranging from 4.1 eV to 4.8 eV. The highest  $g_m$  is measured at 3.56 mS/ $\mu\text{m}$ , implying that the device with  $WF$  of 4.6 eV does have the highest tunnelling volume in the strained channel. This is mainly due to the fact that the amount of electron inversion is slightly increased as the associated electric field in the strained channel becomes weak by virtue of decreasing  $WF$ . Therefore, less  $V_{gs}$  would be required to increase a significant amount of  $I_{ds}$ , which subsequently leads to higher  $g_m$ . The results obtained agreed with previous works carried out by Fang et al. [13] and Pradhan et al. [14].

Figure 7 shows a plot of  $g_m$  with respect to  $WF$  at a maximum  $V_{gs}$ . It is observed that the  $g_m$  linearly increases as  $WF$  increases from 4.1 to 4.6 eV. However, when  $WF$  increases from 4.6 to 4.8 eV,  $g_m$  begins to decrease, mostly as a result of the quasi-saturation of the electron velocity in the source-gate area, induced by the region's electric field reaching its maximum value.

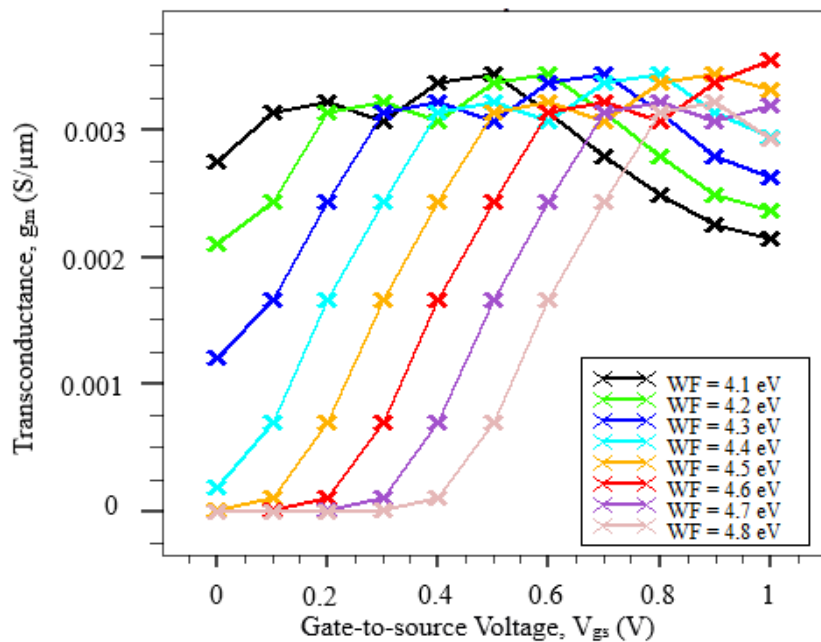


Fig. 6. Plot of  $g_m$  as a function of  $V_{gs}$ .

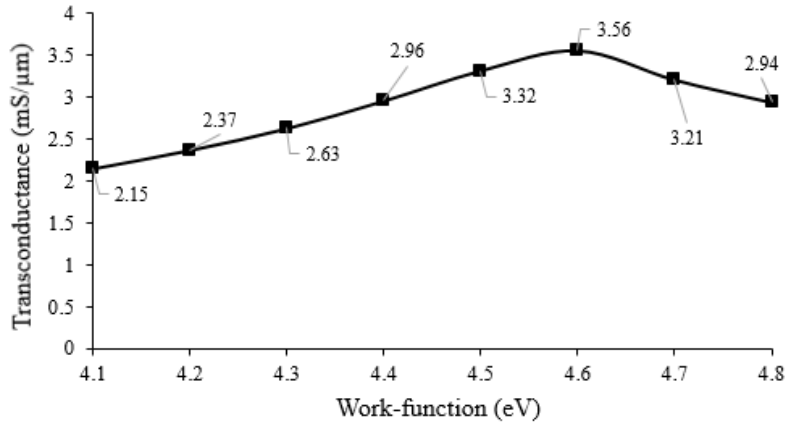


Fig. 7. Plot of  $g_m$  as a function of  $WF$ .

Besides that, the transconductance generation factor ( $TGF$ ) also an important characteristic which is utilized to indicate how effective the generated  $I_{ds}$  in attaining a desired value of  $g_m$ . A higher value of  $TGF$  is needed in order to design an analog circuits that can be operated even at a lower  $V_{DD}$  supply. The  $TGF$  of the device is mathematically denoted as:

$$TGF = \frac{g_m}{I_{ds}} \tag{3}$$

The variation in  $TGF$  is studied at the subthreshold region of the device operation. Figure 8 shows a plot of  $TGF$  as a function of  $V_{gs}$  at a fixed  $V_{ds} = 0.5V$  for  $WF$  ranging from 4.1 eV to 4.8 eV. The highest  $TGF$  recorded is  $141 V^{-1}$ , indicating that the device with a  $WF$  of 4.5 eV is the most efficient. The device's performance improves as a result of its ability to function with a low supply voltage.

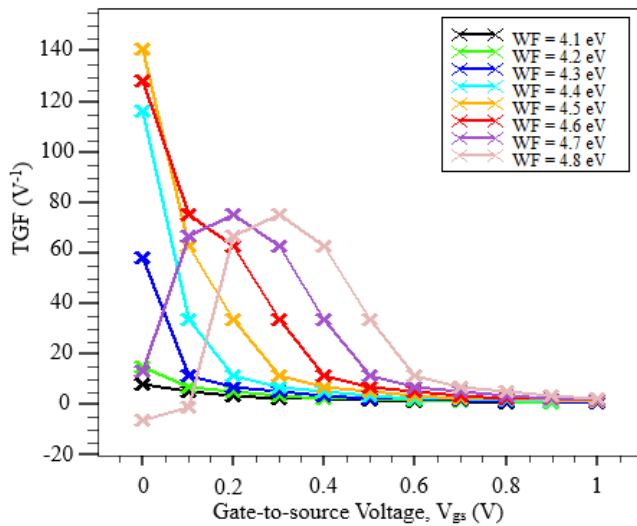


Fig. 8. Plot of  $TGF$  as a function of  $V_{gs}$ .

Figure 9 shows a plot of  $TGF$  with respect to  $WF$  at a minimum  $V_{gs}$ . The  $TGF$  tremendously increases as the  $WF$  increases from 4.1 eV to 4.5 eV. However, when  $WF$  increases from 4.5 to 4.8 eV,  $TGF$  begins to steeply decline, predominantly due to significant improvements in drain current. This implies that the variation in  $WF$  does contribute an enormous impact on the  $TGF$  of the device. Therefore, the  $WF$  should be carefully calibrated, as a very high  $TGF$  is not ideal for high frequency applications with high linearity. A very low  $TGF$  is clearly detrimental, as the power consumption in the subthreshold range would be lesser.

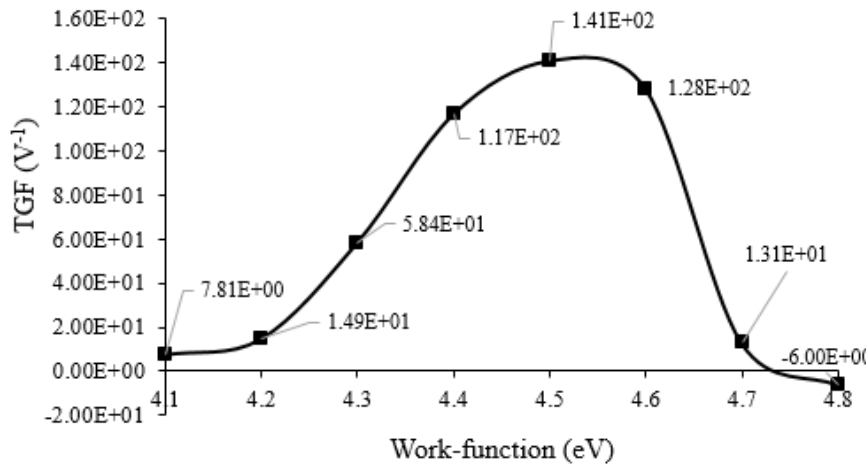


Fig. 9. Plot of  $TGF$  as a function of  $WF$ .

Output conductance ( $g_d$ ) is a crucial characteristic that could decide the behaviors of the proposed device in analog circuits. Ionization effects such as the kink effect and parasitic bipolar action may have an enormous impact on the  $g_d$  value in most transistors [15]. To overcome this issue, the device employs a very thin body ( $\sim 10\text{nm}$ ), so that the strained channel could be fully depleted at certain input  $V_{gs}$  [16]. With the top and bottom gate configuration, engulfing the fully depleted strained channel, those aforementioned impact ionization effects could be further minimized. The  $g_d$  of the device can be computed as:

$$g_d = \frac{\partial I_{ds}}{\partial V_{ds}} \quad (4)$$

Figure 10 depicts a plot of  $g_d$  as a function of  $V_{ds}$  at a fixed  $V_{gs} = 0.5\text{V}$  for  $WF$  ranging from 4.1 eV to 4.8 eV. For low  $WF$ ,  $g_d$  declines linearly with  $V_{ds}$ , and for larger  $V_{ds}$ , it saturates to its minimal value. This suggests that the  $V_{ds}$  has no influence on the band-to-band tunnelling (BTBT) process. Figure 11 shows a plot of  $g_d$  with respect to  $WF$  at a maximum  $V_{ds}$ . The lowest  $g_d$  is measured at  $0.04\text{ mS}/\mu\text{m}$ , produced by the device with  $WF$  of 4.8 eV. This is mainly due to an interruption in electric field at the point along the channel that is graded with a greater carrier concentration, which disperses the electric field mostly toward the terminus of drain. As  $V_{ds}$  grows in the saturation area, a high density channel takes in the additional  $V_{ds}$  after saturation and hinders the electric field's ability to pass through to the terminus of source. This events, known as the screening effect, is the primary source of the decrease in  $g_d$ . In regard of CMOS design consideration, the transistors with low  $g_d$  are always preferable for attaining high gain [17].



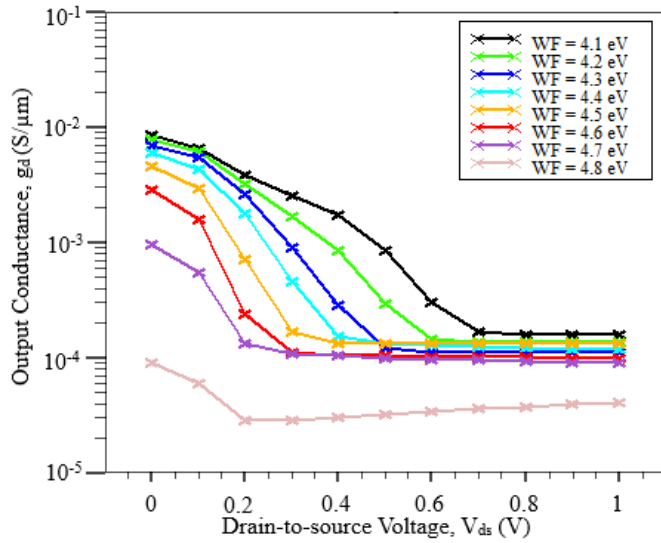


Fig. 10. Plot of  $g_d$  as a function of  $V_{ds}$

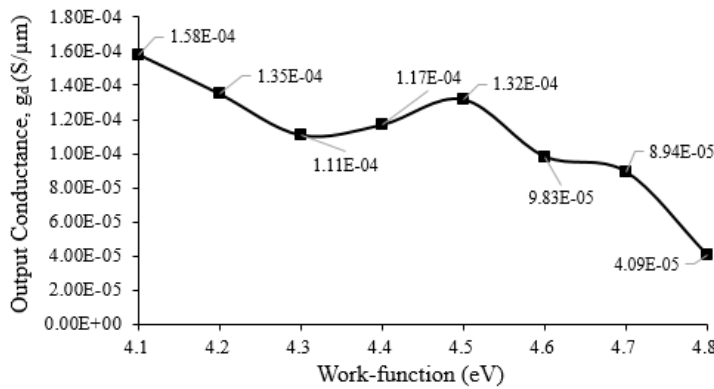


Fig. 11. Plot of  $g_d$  as a function of  $WF$ .

Output resistance ( $r_o$ ) is an important characteristic that contribute a significant impact on the channel length modulation (CLM) of a transistor. A higher  $r_o$  is much desirable for suppressing the CLM effects which can cause an increase in  $I_{ds}$  with increase in drain bias for a transistor that operates in the saturation region. The output resistance ( $r_o$ ) for the proposed device can be computed as:

$$r_o = \frac{1}{g_d} \tag{5}$$

Figure 12 depicts a plot of  $r_o$  as a function of  $V_{ds}$  at a fixed  $V_{gs} = 0.5V$  for  $WF$  ranging from 4.1 eV to 4.8 eV. At all  $WF$  levels,  $r_o$  increases linearly with lower  $V_{ds}$ , and as  $V_{ds}$  increases, it reaches its saturate value. Due to the production of the electric field by the charged carrier, the  $r_o$  will be controlled by the flow of current through its channels. The operation of a transistor begins with the threshold voltage that arises from a current flow with minimum resistance. A limited  $r_o$  is also a result

of the channel length modulation mechanism. Figure 13 shows a plot of  $r_o$  with respect to  $WF$  at a maximum  $V_{ds}$ . The highest  $r_o$  is also demonstrated by the device with  $WF = 4.8$  which is measured at  $24.5 \text{ k}\Omega/\mu\text{m}$ . The higher  $g_d$  implies that the strained channel has lower  $r_o$  which consequently resulting a slight increase in  $I_{ds}$  against the drain bias in saturation regime. As the  $V_{ds}$  increases, its control over the  $I_{ds}$  extends further toward the source region. As a result, the strained channel expands toward the source region, reducing the  $L_{eff}$ , eventually cause much prominent SCEs. Therefore, the impact of  $WF$  variation on  $r_o$  are very important to be considered in analog circuits such as current mirrors and amplifiers. A lower  $r_o$  indicates that the output can serve as a reliable voltage source. It is the function of the amplifier to transform a low-voltage, low-energy input signal into a higher-voltage output signal. The primary benefit of reducing  $r_o$  in transistors is achieving a larger intrinsic gain. Circuits having a low  $r_o$  are also potentially hazardous due to their high current draw. A higher  $r_o$  indicates that the output can serve as a good source of current. Due of higher  $r_o$ , it draws relatively little current.

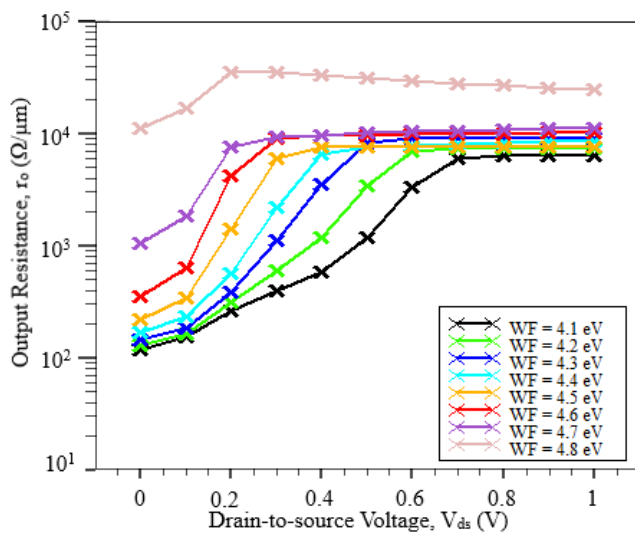


Fig. 12. Plot of  $r_o$  as a function of  $V_{ds}$ .

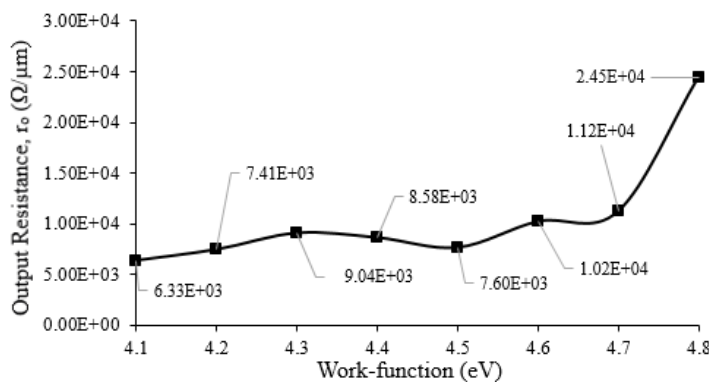


Fig. 13. Plot of  $r_o$  as a function of  $WF$ .

Furthermore, a lower  $g_d$  is capable of driving a higher drain current ( $I_{ds}$ ) to output conductance ( $g_d$ ) ratio which called as an early voltage ( $V_{EA}$ ). The  $V_{EA}$  is a figure of merit that describing the variation of the  $I_{ds}$  of a transistor either in the active or the saturation mode as the drain bias increases. The early voltage ( $V_{EA}$ ) can be mathematically described as:

$$V_{EA} = \frac{I_{ds}}{g_d} \tag{6}$$

Figure 14 depicts a plot of  $V_{EA}$  as a function of  $V_{ds}$  at a fixed  $V_{gs} = 0.5V$  for  $WF$  ranging from 4.1 eV to 4.8 eV. Before reaching threshold,  $V_{EA}$  grows linearly for all  $WF$  levels, and as  $V_{ds}$  increases, it approaches its saturated value. This is mostly due to the channel length modulation (CLM) effect, which can reduce the length of the inverted channel area when the drain bias is increased. CLM results in a rise in drain bias current and a decrease in  $r_o$ . Figure 15 shows a plot of  $V_{EA}$  with respect to  $WF$  at a maximum  $V_{ds}$ . The largest  $V_{EA}$  measured is 0.47 V/ $\mu m$ , as evidenced by the device with  $WF = 4.1$  eV. The decrease in  $WF$  enhances the controllability of both top and bottom gates over the electrons inside the strained channel, thereby increasing the  $V_{EA}$ . Higher  $V_{EA}$  indicates that the dependence of  $I_{ds}$  upon the increasing  $V_{ds}$  is further minimized. The value of  $V_{EA}$  should be as high as possible for better analog performance.  $V_{EA}$  is a performance factor that defines the value of  $g_d$  for a certain  $I_{ds}$  for CMOS amplifier circuits. Similar to how  $TGF$  must be maximized in order to enhance  $g_m$ ,  $V_{EA}$  must be maximized in order to reduce  $g_d$  (or equivalently to maximize  $r_o$ ).  $V_{EA}$  is a current-normalized measure of  $g_d$  that cannot be presumed constant, as is the case with bipolar transistors.

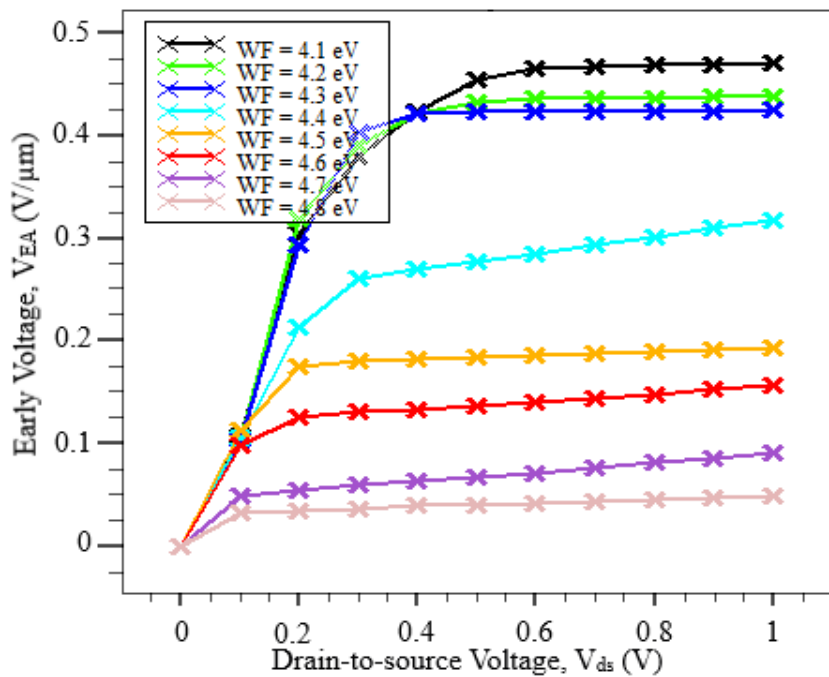


Fig. 14. Plot of  $V_{EA}$  as a function of  $V_{ds}$ .

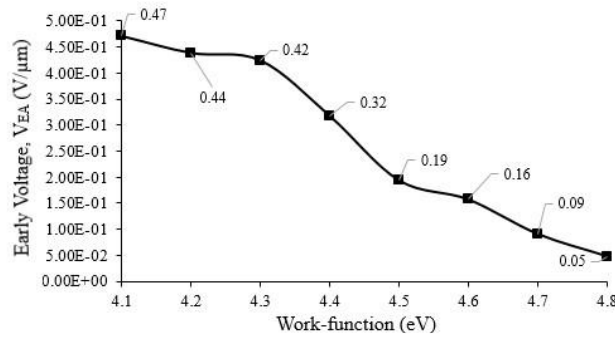


Fig. 15. Plot of  $V_{EA}$  as a function of  $WF$ .

Apart from  $V_{EA}$ , the intrinsic gain ( $A_V$ ) is also an important characteristic for evaluating the analog performance of the proposed device. The  $A_V$  is defined as a ratio of transconductance and output conductance which can be mathematically expressed as:

$$A_V = \frac{g_m}{g_d} = \left(\frac{g_m}{I_D}\right) \cdot V_{EA} \tag{7}$$

Figure 16 shows a plot of  $A_V$  with respect to  $WF$ , ranging from 4.1 to 4.8 eV. The  $A_V$  for the device with  $WF = 4.8$  eV exhibits the highest value which is measured at 97.14 dB.  $WF$  variations exert a substantial impact on the  $g_d$ . A larger  $WF$ , corresponding to a greater  $g_d$ , would result in a greater  $A_V$ . As long as the transistor is functioning in the subthreshold region, the value of  $A_V$  is mostly independent of its bias. The contribution of  $g_d$  to  $A_V$  stems from the effective  $V_{EA}$ , which in turn affects the  $r_o$  of the device.  $A_V$  is one of the most essential characteristics of an amplifier. Moreover, transistors are the fundamental building components of an amplifier. Moreover, the  $A_V$  is a significant performance indicator for a transistor, since it represents the maximum voltage gain that can be obtained by an amplifier with the simplest transistor configuration. Therefore, it is of utmost importance to manufacture a transistor with a high  $A_V$  for the application of amplifiers in the sensor signal processing. A transistor with higher  $A_V$  is also very desirable for operational transconductance amplifiers because it could boost the efficiency of the amplifier to magnify the input signal as it is biased in both active and saturation region of operation. The extracted and calculated value of  $g_m$ ,  $TGF$ ,  $g_d$ ,  $r_o$ ,  $V_{EA}$  and  $A_V$  for multiple  $WF$  are summarized in Table 1.

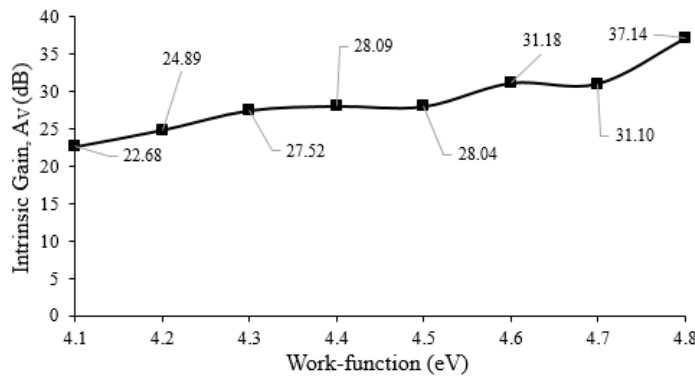


Fig. 16. Plot of  $A_V$  as a function of  $WF$ .

**Table 1. Analogue performance for multiple WF.**

WF (eV)	$g_m$ (mS/ $\mu$ m)	TGF ( $V^{-1}$ )	$g_d$ (mS/ $\mu$ m)	$r_o$ (k $\Omega$ / $\mu$ m)	$V_{EA}$ (V/ $\mu$ m)	$A_V$ (dB)
4.1	2.15	7.81	0.16	6.3	0.47	22.68
4.2	2.37	14.9	0.14	7.4	0.44	24.89
4.3	2.63	58.4	0.11	9	0.42	27.52
4.4	2.96	117	0.12	8.6	0.32	28.09
4.5	3.32	141	0.13	7.6	0.19	28.04
4.6	3.56	128	0.1	10.2	0.16	31.18
4.7	3.21	13.1	0.09	11.2	0.09	31.10
4.8	2.94	-6	0.04	24.5	0.05	37.14

Based on the observation of the results, the *WF* tuning seems to noticeably affect the analogue properties of the device. It also indicates that desired analogue properties of the device could be attained by properly tuned the *WF*. Table 2 shows the comparison of our work with the state of art. The table also shows that our work demonstrate decent  $A_V$  as compared to most of the previous works. Furthermore, our work emphasizes on downscaling the physical gate length to 6nm while keeping acceptable analogue performances. Implementing high-*k* gate dielectrics with strain technology is one of numerous solutions designed to enable the continued shrinking of microelectronic components, sometimes known as extending Moore's Law. The transition to new transistor technology is difficult, and supply schedules for nanosheet FETs vary per foundry. Samsung, for instance, produces a number of technologies based on 7nm and 5nm FinFETs, with ambitions to introduce 3nm nano sheets in 2022/23. IBS indicates that Taiwan Semiconductor Manufacturing Company (TSMC) will increase FinFET to 3nm but will switch to nanosheet FET at 2nm in 2024/25. Intel and other companies are also developing nanosheets. Throughout all generations of CMOS technology, silicon is the preferred material for transistor channels down to 7nm nodes. SiGe is used as the channel material in FinFET structures for the first time in TSMC's 5nm technology, which is the first advanced logic manufacturing method to use this material.

**Table 2. Comparison with state of the art.**

References	Year	Transistor	Gate Length (nm)	$A_V$ (dB)
Sreenivasulu and Narendar [18]	2021	Multi-fin SOI FET	18	~ 18
Misra et al. [19]	2021	SJLGC MOSFET	30	~ 27
Rao et al. [8]	2021	TMGS-GCDG-JL s-Si	35	63.91
Raut and Nanda [20]	2021	JLGAA MOSFET	30	~ 30
Singh and Singh [9]	2022	Si:HfO <sub>2</sub> - NC-EDTFET	50	~ 100
Our work	Current	JL strained DG-MOSFET	6	37.14

Apart from *WF* variation that causing the random fluctuations on the analogue properties, the variations inflicted by design parameters; implant concentration, physical thickness, high-*k* dielectric constant should also be taken into account for

further intensive investigation. In regard with the influence of multiple input parameters on the junction-less strained DG-MOSFET upon the analogue properties, numerous optimization techniques could be possibly deployed in minimizing the output fluctuations, thus enhancing the overall device performances [21-23].

#### 4. Conclusions

The influence of work-function ( $WF$ ) tuning upon analogue properties of junction-less strained DG-MOSFET has been extensively investigated via industrial based process/device simulator, Silvaco TCAD tools. Analogue properties such as transconductance,  $TGF$ , output conductance, output resistance, early voltage and intrinsic gain are comprehensively analysed under acceptable range of  $WF$  tuning (4.1eV-4.8eV) for n-channel device. The final results indicate that the  $WF$  tuning has contributed quite significant impact on the analogue properties of the device. Desired analogue properties such as high transconductance and high intrinsic gain can be achievable via proper tuning of metal  $WF$  which makes the junction-less strained DG-MOSFET as a promising transistor device especially for low power analogue applications.

#### Acknowledgment

The authors would like to thank the Ministry of Higher Education (MOHE) of Malaysia and Micro and Nano Electronics Research Group (MiNE), CeTRI, FKEKK, UTeM for sponsoring this research study under research grant (FRGS/1/2022/TK07/UTEM/02/47).

#### Nomenclatures

$A_V$	Intrinsic gain, dB
$E_C$	Conduction band
$E_F$	Fermi level energy
$E_V$	Valence band
$Ge$	Germanium
$HfO_2$	Hafnium dioxide
$g_d$	Output conductance, S/ $\mu\text{m}$
$g_m$	Transconductance, S/ $\mu\text{m}$
$I_{ds}$	Source-to-drain Current, A/ $\mu\text{m}$
$I_{ON}$	On-state current, A/ $\mu\text{m}$
$I_{OFF}$	Off-state current, A/ $\mu\text{m}$
$r_o$	Output resistance
$Si$	Silicon
$SiGe$	Silicon germanium
$SiO_2$	Silicon dioxide
$T_{high-k}$	High- $k$ dielectric's thickness
$TiO_2$	Titanium dioxide
$V_{ds}$	Source-to-drain voltage, V
$V_{DD}$	Supply voltage, V
$V_{EA}$	Early voltage, V
$V_{gs}$	Gate-to-source Voltage, V
$V_{th}$	Threshold voltage, V

$WSi_x$	Tungsten silicide
<b>Abbreviations</b>	
CLM	Channel length modulation
DIBL	Drain induced barrier lowering
ITRS	International Technology Roadmap for Semiconductors
MOSFET	Metal-oxide-semiconductor field effect transistor
RF	Radio frequency
S/D	Source/drain
TGF	Transconductance generation factor
WF	Work-function

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