DEVELOPMENT AND OPTIMIZATION OF BI-GFET USING TAGUCHI-BASED GREY RELATIONAL ANALYSIS WITH ARTIFICIAL NEURAL NETWORK

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MASTER OF SCIENCE IN ELECTRONIC ENGINEERING

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UNIVERSITI TEKNIKAL MALAYSIA MELAKA

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NUR HAZWANI NAILI BINTI MOHD NIZAM

A thesis submitted
in fulfillment of the requirements for the degree of
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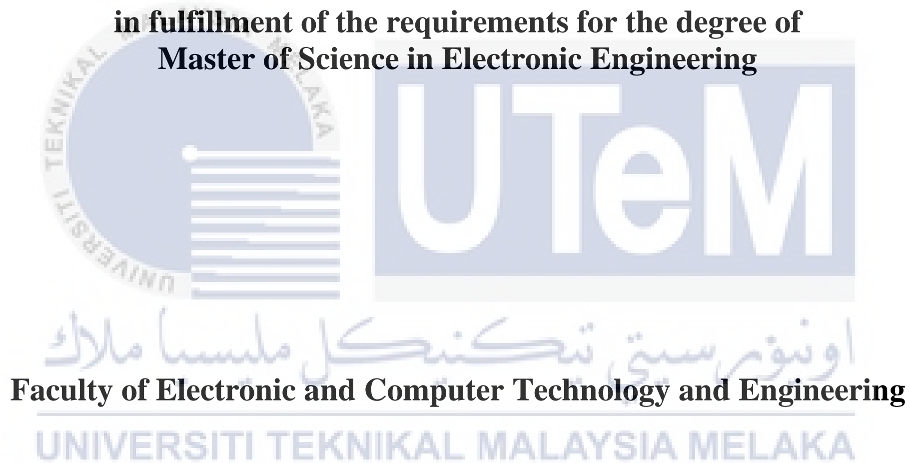

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DEDICATION

To my beloved mother and father, brother and sisters, thank you for your endless love and support. To my supervisor and co-supervisor, thank you for your guidance and knowledge.

ABSTRACT

The semiconductor and electronics industries of micro-to-nano downscaling refer to the trend of miniaturizing electronic devices. The goal of this downscaling is to increase performance while reducing power consumption. However, it has become more complex because of their downscaling limit which possibilities to produce a short channel effect. To address this issue, an additional kind of MOSFET architecture with a double-gate design has been proposed to replace the single-gate MOSFET including replacing the SiO_2/polysilicon gate with a high-k/metal gate to reduce the power consumption of the device. The implementation of bilayer graphene is employed to create a band gap, resulting in a greater on-off ratio. The purpose of this research is to develop the Bi-GFET horizontal double gate NMOS and PMOS device by using Silvaco Software's ATHENA and ATLAS modules and optimize it by using Taguchi-based grey relational analysis (GRA) with an artificial neural network (ANN). For the NMOS device, hafnium dioxide (HfO_2) with tungsten silicide (WSi_x) will be utilized to examine the performance of the characteristics of the threshold voltage (V_{TH}), drive current (I_{ON}), and leakage current (I_{OFF}). Meanwhile, HfO_2 with titanium silicide ($TiSi_x$) will be utilized in the PMOS device. In order to optimize the NMOS and PMOS device, the process parameters of V_{TH} adjustment implant dose, V_{TH} adjustment implant energy, S/D implant dose, and S/D implant energy were studied. The full potential of the Taguchi method as a tool for optimizing the performance of processes with a wide range of input variables has been realized. Based on the Taguchi results, S/D adjustment implant energy is identified as the dominant factor in the NMOS device with a contributing factor effect percentage of 89.77%, while V_{TH} adjustment implant energy is identified as the dominant factor in the PMOS with a contributing factor percentage of 55.91%. To solve optimization problems with multiple responses of V_{TH}, I_{ON}, and I_{OFF}, GRA is used in conjunction with the Taguchi method in NMOS and PMOS devices. After optimization by using Taguchi-based GRA, the V_{TH}, I_{ON}, and I_{OFF} of the NMOS devices are observed to be at 0.20849 V, 5192.22 µA/µm, and 0.56513 nA/µm respectively. Meanwhile, the V_{TH}, I_{ON}, and I_{OFF} of the PMOS devices are observed to be at 0.19793 V, 167.873 µA/µm, and 32.5728 nA/µm respectively. The grey relational grade (GRG) of NMOS devices increased slightly by 3.44%, while the PMOS device was reduced by 0.86%. To forecast optimal optimization outcomes for the NMOS and PMOS devices a well-trained ANN is developed using the Levenberg-Marquardt algorithm. Results showed that V_{TH}, I_{OFF}, and I_{ON} values for NMOS devices met the prediction of the International Technology Roadmap Semiconductor (ITRS) with a value of 0.20987 V, 4979.58 µA/µm, and 0.10375 nA/µm respectively. For the PMOS device, V_{TH} and I_{OFF} met the prediction of the ITRS with the value of 0.20452 V, and 20.3584 nA/µm respectively, while the I_{ON} value is lower than the prediction with the value of 153.996 µA/µm due to the higher mobility of electrons resulting in a higher drain current.

PEMBANGUNAN DAN PENGOPTIMUMAN BI-GFET MENGGUNAKAN ANALISIS HUBUNGAN KELABU BERASASKAN TAGUCHI DENGAN RANGKAIAN NEURAL BUATAN

ABSTRAK

Industri semikonduktor dan elektronik penurunan skala mikro-ke-nano merujuk kepada tren meminimumkan peranti elektronik. Matlamat penurunan ini adalah untuk meningkatkan prestasi sambil mengurangkan penggunaan kuasa. Walau bagaimanapun, ia telah menjadi lebih kompleks kerana had penurunan yang berkemungkinan menghasilkan kesan saluran pendek. Untuk menangani isu ini, jenis seni bina MOSFET tambahan dengan reka bentuk dua get telah dicadangkan untuk menggantikan MOSFET satu get termasuk menggantikan SiO_2*/polisilikon get dengan get tinggi-k/logam untuk mengurangkan penggunaan kuasa peranti. Pelaksanaan grafin dwilapisan digunakan untuk mewujudkan jurang jalur, menghasilkan nisbah ON/OFF yang lebih besar. Tujuan penyelidikan ini adalah untuk membangunkan peranti NMOS dan PMOS dua get mendatar Bi-GFET dengan menggunakan modul ATHENA dan ATLAS daripada perisian Silvaco dan mengoptimumkannya dengan menggunakan analisis hubungan kelabu (GRA) berasaskan Taguchi dengan rangkaian neural tiruan (ANN). Untuk peranti NMOS, hafnium dioksida (*HfO_2*) dengan tungsten silicid (*WSi_x*) akan digunakan untuk mengkaji prestasi ciri-ciri voltan ambang (*V_{TH}*), arus pemacu (*I_{ON}*), dan arus bocor (*I_{OFF}*). Sementara itu,* HfO_2 *dengan titanium silicid (*$TiSi_x$*) akan digunakan dalam peranti PMOS. Untuk mengoptimumkan peranti NMOS dan PMOS, parameter proses dos implan pelarasan* V_{TH}*, tenaga implan pelarasan* V_{TH}*, dos implan S/D, dan tenaga implan S/D telah dikaji. Potensi penuh kaedah Taguchi sebagai alat untuk mengoptimumkan prestasi proses dengan pelbagai pembolehubah input telah direalisasikan. Berdasarkan keputusan Taguchi, tenaga implan pelarasan S/D dikenal pasti sebagai faktor dominan dalam peranti NMOS dengan peratusan kesan faktor penyumbang sebanyak 89.77%, manakala tenaga implan pelarasan* V_{TH} *dikenal pasti sebagai faktor dominan dalam PMOS dengan peratusan faktor penyumbang sebanyak 55.91%. Untuk menyelesaikan masalah pengoptimuman dengan pelbagai respons, GRA digunakan bersama dengan kaedah Taguchi dalam peranti NMOS dan PMOS. Selepas pengoptimuman dengan menggunakan GRA berasaskan Taguchi,* V_{TH}*,* I_{ON}*, dan* I_{OFF} *peranti NMOS diperhatikan berada pada 0.20849 V, 5192.22 μA/μm, dan 0.56513 nA/μm masing-masing. Sementara itu,* V_{TH}*,* I_{ON}*, dan* I_{OFF} *peranti PMOS diperhatikan masing-masing pada 0.19793 V, 167.873 μA/μm, dan 32.5728 nA/μm. GRA peranti NMOS meningkat sedikit sebanyak 3.44%, manakala peranti PMOS dikurangkan sebanyak 0.86%. Untuk meramalkan hasil pengoptimuman optimum untuk peranti NMOS dan PMOS, ANN yang terlatih dibangunkan menggunakan algoritma Levenberg-Marquardt. Keputusan menunjukkan bahawa nilai* V_{TH}*,* I_{OFF}*, dan* I_{ON} *untuk peranti NMOS memenuhi ramalan ITRS dengan nilai 0.20987 V, 4979.58 μA/μm, dan 0.10375 nA /μm masing-masing. Bagi peranti PMOS,* V_{TH} *dan* I_{OFF} *menepati ITRS dengan nilai 0.20452 V, dan 20.3584 nA/μm masing-masing, manakala nilai* I_{ON} *adalah lebih rendah daripada ramalan dengan nilai 153.996 μA/μm kerana mobiliti yang lebih tinggi, elektron menghasilkan arus saliran yang lebih tinggi.*

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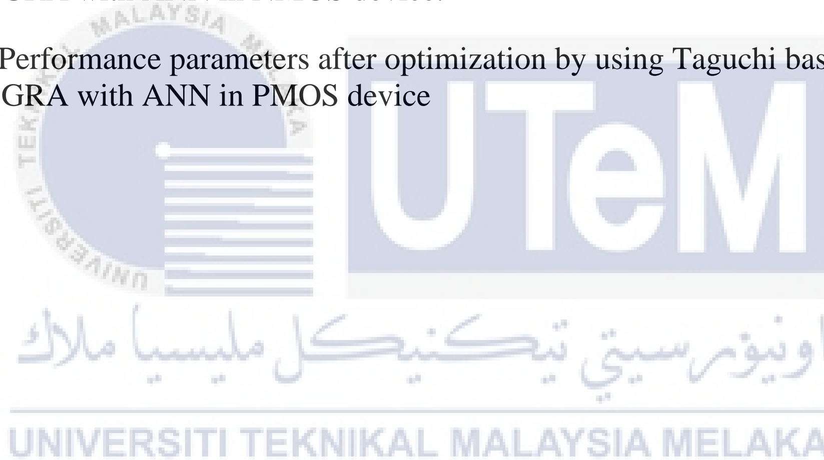

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LIST OF ABBREVIATIONS

ANN	-	Artificial Neural Network
ANOVA	-	Analysis of Variance
Bi-GFET	-	Bilayer Graphene Field Effect Transistor
CMOS	-	Complementary Metal Oxide Semiconductor
DF	-	Degree of Freedom
DIBL	-	Drain Induced Barrier Lowering
DoE	-	Design of Experiment
GRA	-	Grey Relational Analysis
GRC	-	Grey Relational Coefficient
GRG	-	Grey Relational Grade
ITRS	-	International Technology Roadmap for Semiconductor
LMBP	-	Levenberg-Marquardt Back Propagation
MOSFET	-	Metal Oxide Semiconductor Field Effect Transistor
MS	-	Mean Square
MG	-	Multi-gate
NMOS	-	Negative Channel Metal Oxide Semiconductor
OA	-	Orthogonal Array
PMOS	-	Positive Channel Metal Oxide Semiconductor
S/D	-	Source Drain
SNR	-	Signal noise ratio
TCAD	-	Technology Computer Aided Design
SSQ	-	Sum of Squares

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LIST OF SYMBOLS

Al_2O_3	-	Aluminium dioxide
F-value	-	Ration of the mean squares divide by the mean error sum of squares
FP	-	F-value for each process parameter
HfO_2	-	Hafnium dioxide
I_{ON}	-	Drive current
I_{OFF}	-	Leakage current
I_{DS}	-	Drain current
P-value	-	Probability value
Poly-Si	-	Polysilicon
SiO_2	-	Silicon dioxide
$TiSi_x$	-	Titanium silicide
VG	-	Gate voltage
V_{DS}	-	Drain voltage
VP	-	Variance
V_{TH}	-	Threshold voltage
Wsi_x	-	Tunsgten silicide
xi (k)	-	Original sequence
xi*(k)	-	Comparable sequence
$x_o(k)$	-	Target value
xo*(k)	-	Reference sequence
μ	-	Carrier mobility in the channel

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ρ	-	Percentage contribution
Δ0i(k)	-	Deviation sequence of the refrence sequence
ξi	-	Identifaction coeffiecient

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LIST OF PUBLICATIONS

The followings are the list of publications related to the work on this thesis:

Nizam, N.H.N.M., AH, A.M., Salehuddin, F., Kaharudin, K.E., ZA, N.F. and Jaya, H.T., 2023. Virtual Fabrication of 14nm Gate Length n-Type Double Gate MOSFET. *International Journal of Nanoelectronics and Materials*, *16*(1).

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Nizam, N.H.N.M., AH, A.M., Salehuddin, F., Kaharudin, K.E. and ZA, N.F., 2022. Optimization of 14nm Horizontal Double Gate for Optimum Threshold Voltage Using L9 Taguchi Method. *International Journal of Nanoelectronics and Materials*, *15*.

Conference Proceedings

Naili, N.H., Afifah Maheran, A.H., Salehuddin, F., Kaharudin, K.E. and Faizah, Z., 2024, February. Virtual fabrication in modelling 14 nm horizontal double gate bilayer graphene FET NMOS/PMOS. In *AIP Conference Proceedings* (Vol. 2898, No. 1). AIP Publishing.

Nizam, N.H.N.M., AH, A.M., Salehuddin, F., Kaharudin, K.E. and ZA, N.F., 2022. Optimization of 14nm Horizontal Double Gate for Optimum Threshold Voltage Using L9 Taguchi Method. *International Journal of Nanoelectronics and Materials*, *15*.

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CHAPTER 1

INTRODUCTION

1.1 Background

With the advancing technology of the semiconductor industry, the feature size of Metal Oxide Semiconductor Field Effect Transistors (MOSFET) has been dramatically reduced. Moore's Law producing a proper operating ultra-small transistor becomes extremely important as silicon approaches atomic resolution and reaches its physical and electrical constraints. The International Technology Roadmap Semiconductor (ITRS) prediction the idea of scaling up devices over the next 15 years. To resolve this challenge, researchers have been working on new materials that can be utilized to produce transistors as an alternative to silicon. Due to various outstanding electrical properties of graphene, it is possible to do significant research on graphene field effect transistor (GFET) devices with a variety of structures.

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Moore's Law, formulated by Gordon Moore, a co-founder of Intel Corporation, in 1965, forecasts that the quantity of transistors packed onto a microchip would roughly double every couple of years. This exponential growth trend has resulted in significant boosts in computing capabilities while concurrently driving down the expense per transistor. Over time, Moore's observation has remained remarkably accurate, catalyzing the swift evolution of the electronics sector and enhancing the potency and availability of computing resources. The law is often cited as an example of exponential technological progress and has become a guiding principle for the semiconductor industry (Thompson and Parthasarathy, 2006).

While the pace of progress has slowed somewhat in recent years, due in part to the physical limitations of miniaturizing transistors, the fundamental trend predicted by Moore's Law continues to drive innovation and growth in the field of computing and technology (Waldrop, 2016).

In order to produce a reliable design and high-performance device, the majority of device modelling and particularly MOSFET's design require an appropriate optimization strategy. For MOSFET channel engineering specifically, such precise dopant control is essential. Reduced silicon substrate atom number corresponds to decreasing MOSFET dimensions. Because of this, regulating dopant concentrations and localization will become essential (Lu, Lu and Taur, 2008). Statistical variance in several process parameters is necessary due to the difficulty of perfect control during the MOSFET manufacturing process.

Maintaining single gate of complementary metal oxide semiconductor (CMOS) devices on target for 20 nm node technology is one of the critical downsizing issues (Afifah Maheran et al., 2016). To counteract this short channel effect (SCE), multi gate with high performance has been implemented in this research. Previous research were conducted to incorporate a double gate architecture into the MOSFET design, which is expected to be very effective in lowering the short channel effects (SCE) (Kaharudin et al., 2014; Mendiratta and Tripathi, 2021). Moreover, several studies have been conducted to enhance the performance of devices by controlling the doping profile in the channel region.

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1.2 Problem Statement

Although traditional MOSFET devices have dominated the semiconductor industry for decades, keeping up with Moore’s Law has become more difficult due to the various

challenges provided by exceedingly small feature sizes. Shrinking the conventional MOSFET requires innovation to circumvent barriers due to the fundamental physics (Sood et al., 2018). Due to the presence of SCEs in ultra-small field effect transistor (FETs), scaling device of the oxide thickness might result in a high tunneling current and a lower I_{ON}/I_{OFF} ratio, resulting in poor power consumption.

Traditional poly-Si/SiO_2 technology could be utilized in smaller MOSFET devices to satisfy the low power technology standards set by ITRS 2013. Nevertheless, the effectiveness of classic Poly-Si/SiO_2 technology diminishes below the 22 nm technology node due to issues like short channel effects and poly depletion effects, which negatively impact transistor performance. Consequently, for semiconductor devices at the nanoscale, there has been consideration of using high-k dielectrics as a substitute for SiO_2 as the gate dielectric material.

In recent years, there has been significant interest in graphene owing to its exceptional electrical characteristics (Hamam et al., 2018; Novodchuk et al., 2020).

Reports indicate that intrinsic graphene possesses elevated levels of carrier mobility, carrier density, thermal conductivity, and durability (Wang et al., 2019). GFET are challenging to be used in digital logic despite their outstanding electronic properties because graphene does not have a band gap in its normal form, making them difficult to turn off. As a result, bilayer graphene was used in this research to address this problem. With this method, the graphene channel in the transistor is able to induce a band gap leading to higher on-off ratio (Chin et al., 2014; Hamam et al., 2018).

Scaling down the MOSFET will cause SCE. Thus, another kind of MOSFET architecture that has been used to address the problems caused by the SCE is the double gate variety. For the simple reason that increasing the channel's gate count enhances electrostatic

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