DESIGN AND ANALYSIS OF 22 NM DG-MOSFET WITH HIGH-K METAL GATE GRAPHENE STRUCTURE FOR BETTER CURRENT PERFORMANCE

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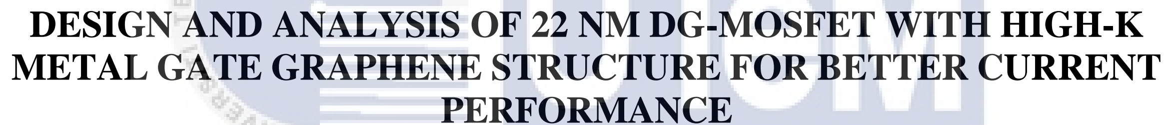
MASTER OF SCIENCE IN ELECTRONIC ENGINEERING

2024

Faculty of Electronics and Computer Technology and Engineering



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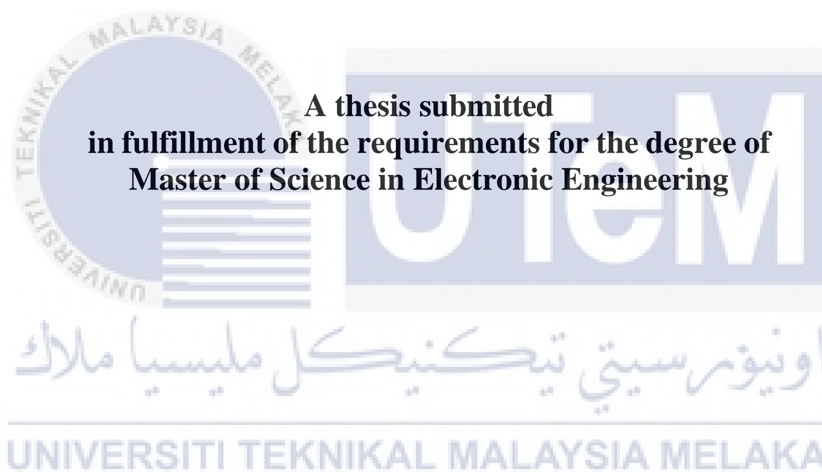
A thesis submitted
in fulfillment of the requirements for the degree of
Master of Science in Electronic Engineering



Faculty of Electronics and Computer Technology and Engineering

UNIVERSITI TEKNIKAL MALAYSIA MELAKA

2024

DEDICATION

I honour my parents with this thesis

Mariah Binti Hashim and Allahyarham Yahaya bin Abd. Rahman

My lovely wife, Nursahizalina Mohd Sa’at and my kids Muhamad Aniq Haziq,

Qaseh Nur Damia, Qaseh Nur Zahraa’, and Muhamad Umar Hafiy

They gave me new inspiration and support

Ts. Dr. Afifah Maheran and PM. Ir. Dr. Fauziyah, who gave me guidance,

advice, and enthusiasm to do this research until the end of today

with full dedication and determination

Without their love and support, this study would not have been completed

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ABSTRACT

One of the innovations with the unique properties of graphene, which is frequently a complementary material of today's advanced materials technology, is the design process for the virtual fabrication of double layer graphene MOSFET 22 nm with high-k metal gate (HKMG). Aggressive scaling of MOSFET designs with channel lengths below 100 nm and oxide gate thicknesses below 3 nm is required to enhance performance and packaging density. As a result, several variables, such as threshold voltage, sub-threshold slope, ON current, and OFF current, significantly impact how well a device scales. Both devices were the focus of simulation work that was carried out and documented in publications. The TCAD fabrication tool from SILVACO software was used. Both the ATLAS and ATHENA simulation modules were used to create the device design and to describe the electrical characteristics of the device. Using the fixed field scaling method, it is possible to determine the electrical characterization of transistors according to international standards. Nano-sized transistors are produced using cutting-edge and novel techniques, which reduce production issues while enhancing transistor performance. Titanium dioxide (TiO_2) and Tungsten Silicide (WSix) are used for the metal gate. Applying graphene to MOSFETs will increase current drive and decrease current leakage, hence improving electron mobility. Due to the connection between the graphene layer and the high-k metal gate, double gate (DG) MOSFETs are electrostatically superior to single gate (SG) MOSFETs, enabling further gate length scaling. A model that complies with the International Technology Roadmap for Semiconductor (ITRS) specification. The required V_{TH} for logic technology high performance (HP) data should get the value is 0.206 ±12.7%V. The Taguchi method correctly predicted the best solution for fabricating the desired DG-MOSFET 22 nm with bilayer graphene. The primary response used to decide whether or not the designed device operates is the threshold voltage. One of the process variables that had the biggest impact on response characteristics in this study was the threshold voltage implant. The threshold voltage value for NMOS is 0.197858V and PMOS is -0.20744V. Both of these values are still within the ITRS standard range. Whereas for PMOS and NMOS devices, the S/D Implant Energy dose was identified as an adjustment factor to obtain nominal threshold voltage values of PMOS -0.206V ±12.7% and NMOS +0.206V ±12.7%, respectively. The I_{ON} value must be greater than 1469 uA/um, and the I_{OFF} value must be less than 100 nA/um. This is achieved by performing experiments using designed arrays of MOSFETs, each with different design parameters, and then using statistical analysis to identify the ideal set of parameters. Taguchi's method has been successful in finding designs that minimize the variability of performance metrics, making devices more robust and predictable.

REKA BENTUK DAN ANALISIS DG-MOSFET 22 NM DENGAN STRUKTUR GRAFIN GET LOGAM TINGGI-K BAGI PRESTASI ARUS YANG LEBIH BAIK

ABSTRAK

Salah satu inovasi dengan sifat unik grafin, yang sering menjadi bahan pelengkap teknologi bahan termaju hari ini, ialah proses reka bentuk fabrikasi maya grafin dua lapisan MOSFET 22 nm dengan get logam tinggi-k (HKMG). Penskalaan agresif reka bentuk MOSFET dengan panjang saluran di bawah 100 nm dan ketebalan get oksida di bawah 3 nm diperlukan untuk meningkatkan prestasi dan ketumpatan pembungkusan. Akibatnya, beberapa pembolehubah, seperti voltan ambang, cerun kecil ambang, arus ON dan arus OFF, mempunyai kesan yang ketara ke atas seberapa baik skala peranti. Kedua-dua peranti adalah fokus kerja simulasi yang telah dijalankan dan didokumenkan dalam penerbitan. Alat fabrikasi TCAD perisian SILVACO telah digunakan, dengan modul simulasi ATHENA digunakan untuk membina reka bentuk peranti dan modul ATLAS digunakan untuk menerangkan sifat elektrik peranti. Menggunakan kaedah penskalaan medan tetap, adalah mungkin untuk menentukan pencirian elektrik transistor mengikut piawaian antarabangsa. Transistor bersaiz nano dihasilkan menggunakan teknik canggih dan baru, yang mengurangkan isu pengeluaran sambil meningkatkan prestasi transistor. Titanium dioksida (TiO_2) digunakan, dan Silika Tungsten (WSix) digunakan sebagai get logam. Menggunakan grafin pada MOSFET akan meningkatkan pemacu semasa dan mengurangkan kebocoran semasa, seterusnya meningkatkan mobiliti elektron. Disebabkan sambungan antara lapisan grafin dan get logam tinggi-k, MOSFET dua get (DG) adalah lebih baik secara elektrostatik daripada MOSFET get tunggal (SG) dan membolehkan penskalaan panjang get selanjutnya. Model yang mematuhi spesifikasi International Technology Roadmap for Semiconductor (ITRS). Mengikut keputusan, V_{TH} ialah 0.206 ±12.7% V untuk keperluan teknologi logik prestasi tinggi (HP). Kaedah Taguchi dengan betul meramalkan penyelesaian terbaik untuk merekacipta DG-MOSFET 22 nm yang dikehendaki dengan grafin. Voltan ambang adalah tindak balas utama dalam menentukan sama ada peranti yang direka bentuk berfungsi atau tidak. Implan voltan ambang dikenal pasti sebagai salah satu parameter proses yang mempunyai pengaruh terbesar terhadap ciri tindak balas dalam kajian ini. Nilai voltan ambang untuk NMOS yang diperolehi ialah 0.197858V dan PMOS pula ialah -0.20744V. Kedua-dua nilai ini masih di dalam julat piawaian ITRS. Manakala bagi peranti PMOS dan NMOS, dos Tenaga Implan S/D dikenal pasti sebagai faktor pelarasan untuk mendapatkan nilai voltan ambang nominal masing-masing -0.206V ±12.7% dan +0.206V ±12.7%. Nilai arus ON mestilah melebihi 1469uA/um dan nilai arus OFF mestilah di bawah nilai 100nA/um. Ini dicapai dengan melakukan eksperimen menggunakan tatasusunan MOSFET yang direka bentuk, setiap satu dengan parameter reka bentuk yang berbeza, dan kemudian menggunakan analisis statistik untuk menentukan gabungan parameter yang optimum. Kaedah Taguchi telah berjaya untuk mencari reka bentuk yang meminimumkan kebolehubahan metrik prestasi, menjadikan peranti lebih teguh dan boleh diramal.

ACKNOWLEDGEMENTS

I dedicate this research to all researchers in the field of microelectronic devices in Malaysia, proud to be indirectly involved in this research field. I could only complete my master's research with the help of some of your studies. I am indebted to you all. I would also like to express my appreciation to the Ministry of Higher Education (KPT) for giving me a scholarship and the opportunity to further my studies through the Federal Training Scholarship (HLP) and Universiti Teknikal Malaysia Melaka (UTeM) for providing the research platform.

First and most importantly, I would like to express my sincere appreciation to my main supervisor, Ts. Dr. Afifah Maheran Abdul Hamid, and my second supervisor, PM. Dr. Ir. Fauziyah Salehuddin. I want to thank him for his helpful criticism and ongoing encouragement during my research. I sincerely appreciate everything he has done to help me prepare and write a master's thesis of the highest calibre and for letting me use this thesis to express my interests. Second, I would like to thank all my university lecturers, including as well as supported staff at the School of Graduate Studies and Faculty of Electronics and Computer Technology and Engineering, Universiti Teknikal Malaysia Melaka. They taught me various subjects that may have contributed directly and indirectly to writing this thesis, especially the various courses and training conducted on writing thesis or papers and preparing and motivating oneself before and after embarking on this master's journey. Finally, my special thanks go to Dr. Khairul Ezwan for all the help and support I received from him.

Thank you to all my friends, especially Wong and Lukman, who provided me with the assistance, support and inspiration to embark on my study. The last and most important person I want to thank is my family, my in laws, and my wife, Nursahizalina Mohd Sa'at. She has made a significant contribution in terms of love, motivation, and financial and moral support in helping me finish this master's thesis.

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LIST OF SYMBOLS AND ABBREVIATIONS

SiO_2	-	Silicon Dioxide
TiO_2	-	Titanium Dioxide
WSix	-	Tungsten Silicide
FET	-	Field Effect Transistor
Si	-	Silicon
MOSFET	-	Metal-oxide semiconductor field effect transistor
EOT	-	Electrical Oxide Thickness
V_{TH}	-	Threshold voltage
I_{OFF}	-	Leak current
I_{ON}	-	Drive current
ITRS	-	International Technology Roadmap for Semiconductor
V_{GS}	-	Gate source voltage
V_G	-	Gate voltage
LPCVD	-	Low Pressure Chemical Vapor Deposition Process
BPSG	-	Borophosphosilicate Glass
PMD	-	Pre-Metal Dielectric
CF	-	Control Factor
NF	-	Noise Factor
high-k	-	High dielectric constant k
EOT	-	Electrical Oxide Thickness
SOS	-	Silicon-on-Sapphire
OA	-	Orthogonal Array
S/D	-	Source/Drain
HKMG	-	High-k metal gate
DG	-	Double-gate
SG	-	Single-gate
TCAD	-	Technology Computer Aided Design
HP	-	High Performance
SCE	-	Short Channel Effects

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Indexed Journal

Izwanizam Yahaya, A.H. Afifah Maheran, F. Salehuddin and K. E. Kaharudin, 2022. Design and Electrical Simulation of a 22 nm MOSFET with Graphene Bilayer Channel using Double High-κ Metal Gate. *International Journal of Nanoelectronics and Materials.* Volume 15, No. 2, April 2022, pp. 79-90. (Scopus Indexed, Q3)

Izwanizam Yahaya, A.H. Afifah Maheran, F. Salehuddin and K. E. Kaharudin, 2023. Taguchi Method for PMOS Threshold Voltage Optimization with a Gate Length of 22 nm. *International Journal of Nanoelectronics and Materials.* Volume 16, January 2023, pp. 1-9 (Scopus Indexed, Q3)

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Izwanizam Yahaya, Afifah Maheran A.H., F. Salehuddin, and K.E. Kaharudin, 2020. 22 nm Graphene FET Design Structure, Fabrication and Characterization. *Proceeding of Mechanical Engineering Research Day* 2020, pp. 129-130.

Y. Izwanizam, A. H. Afifah Maheran, F. Salehuddin, and K. E. Kaharudin, 2022. Optimization of 22 nm Bi-GFET Device for Threshold Voltage Using Taguchi Method. *AIP Conference Proceeding* 2465, 040004.

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CHAPTER 1

INTRODUCTION

In this chapter, the background of MOSFETs in the field of device performance is presented and discusses the characteristics that make the best choice in designing new or improved MOSFET devices for material characterization applications. It also explains the objectives and scope of work. Furthermore, the structure organization of the thesis has been discussed more detail in this chapter (Faro et al., 2020).

1.1 Background

In order to meet the demands of the digital electronics industry, over the past few decades, the chip semiconductor design industry has placed a significant emphasis on the creation of smaller, more compact, quicker, and less expensive products (S. Chopra et al., 2015). The highest density chip design in the Ultra Large-Scale Integration (ULSI) technology requires that the metal oxide semiconductor transistor effect transistors (MOSFET) packing density be used in the highest possible range and, therefore, the smallest transistor sizes. Down scaling not only produces higher integration densities but also transistor drives and higher densities for faster switching speeds. This is the primary factor that contributed to the smaller MOSFETs, faster switching speeds, and lower production costs. A.H. Afifah Maheran et al. (2014) suggested that manipulation at the atomic scale is necessary to obtain the performance and density required in Si materials systems, in accordance with International Technology Roadmap for Semiconductor (ITRS) (M. S. Alam., 2011). MOSFET dimension down scaling is commonly called scale

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(X. Wangl., 2016). Measuring the gate dielectric thickness has long been recognized as one of the keys to measuring devices. The ultra-thin gate dielectric in MOSFET remains a critical element of conventional silicon-based microelectronic devices. Since the beginning of the era of microelectronic technology, SiO_2 oxide gates have played an important role in device performance and scaling (X. Wang et al., 2014). Based on the SiO_2 gate oxide thickness of the first transistor, which is several hundred nanometers, the functionality and performance of the state-of-the-art equipment now depend on the gate oxide of a few layers of atoms 1-2 nm thick.

Because the physical thickness of SiO_2 based gate oxides approaches 2 nm, several fundamental problems arise (A. H. Afifah Maheran et al., 2014). In this ultra-thin regime, several major dielectric parameters are impaired like gate leakage current, oxide breakdown, boron penetration of polysilicon and channel mobility (S. Chopra et al., 2015). Each parameter is important for device operation. In other words, the scaling scenario of conventional devices involving SiO_2 based dielectric distribution below 1 nm has become impractical (X. Wang, 2016). Based on the weakness of SiO_2, researchers have previously substituted high-k metal gates to increase the capability and efficiency of semiconductor devices. For better current performance semiconductor devices, after the replacement to WSix as high-k metal gate, the semiconductor design layer was innovated with a graphene layer. The two dimensional substance known as graphene is made up of a single layer of carbon atoms arranged in a honeycomb pattern. Its strong points are its excellent heat and electrical conductivity. Graphite is the stacked form of graphene. The use of graphene technology has increased its use in semiconductor device manufacturing technology due to high best mobility and current performance.

The DG-MOSFETs allow for greater gate length scaling and are electrostatically superior than single gate (SG) MOSFETs (Mr. Sanjay Chopade et al., 2013). Devices with

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two gates on either side of the channel are known as DG-MOSFETs. In contrast to the bottom gate, which is on the lower part of the channel, the top gate is there. It enhances channel control by utilizing the gate electrodes (Zhihong Chen et al., 2008). As a result, every section of the channel is close to a gate electrode. As a result of the DG-MOSFETs structure's reduction of short-channel effects, devices may be down scaled more aggressively, up to a 10 nm gate length (Santosh Kumar Gupta et al., 2012).

The benefits of utilizing a planar arrangement include the ability to employ current production techniques and higher consistency of Silicon channel thickness. It is difficult to reach the bottom gate for device wiring and to manufacture the back gate and gate dielectric underneath the silicon channel. These drawbacks may affect device density.

Using non-planar structures, such as the wraparound gate, has the advantages of making both gates easier to construct and access and increasing device density. Front and back gates cannot be separately biased from traditional manufacturing procedures, and channel thickness is determined by lithography (poorer homogeneity) as a drawback (Tsu Jae King Liu, 2012). The DG planar structure is utilized for design and stimulation because planar structures are simple to create. The electric field and the amount of current flowing through the channel are both controlled by the voltage provided to the gate terminals.

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The most popular design for double-gate MOSFETs is the planar structure, which consists of a thin silicon film sandwiched between two gates. A source and drain region are connected by a channel region in a planar double-gate MOSFET, much like a conventional MOSFET. However, there are two gate electrodes on either side of the channel region rather than just one gate electrode on top of it. A thin silicon film, which serves as the channel region, divides the two gates. To produce an electric field that regulates the flow of electrons through the channel region, the two gates can each be biased independently.

The effective channel length can be changed by varying the voltages applied to the gates, providing greater control over the transistor's performance. In addition, compared to conventional MOSFETs, the double-gate MOSFET can achieve better electrostatic control of the channel region, which enhances performance and lowers power consumption.

The double gate MOSFET is a common option for research and development due to its planar structure, which is relatively straightforward and simple to manufacture. The planar structure may, however, result in some performance drawbacks, such as heightened parasitic capacitances and short channel effects. Alternative double gate MOSFET structures, such as FinFETs and nanowire transistors, have been created by researchers to get around these restrictions.

1.2 Problem Statement

The continuous development of MOSFETs technology has reduced the size and length of channels from micrometres to sub micrometres and then to sub micrometres following Moore's Law (F. Salehuddin et al., 2011). The length of MOSFET was reduced to 35 nm. A reducing length of conventional MOSFETs will undertake innovation to avoid obstacles caused by basic physics (Ferain I. et al., 2011). Short-channel effects (SCEs) are always a major problem when dealing with such tiny transistors. Therefore, the goal of achieving the perfect switch for transistors and minimizing SCEs can lead to new ways of designing transistors such as multi-gate transistors. Invariability of metal-oxide semiconductor processes using ion implantation into the channel area, which alters the doping profile near the silicon substrate surface. Changing the dosage, rotation and energy of the implant will change the device features such as leakage current and threshold voltage (Nayereh Ghobadi et al., 2014). Statistical modelling techniques will be used in this research design to identify and optimize the input process parameters on various device

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features. Modern semiconductor businesses have adapted their production methods to be more economical and competitive in the face of global competition. As a result, several modern technologies have scaled down the MOSFET to the nanoscale range. Because MOSFETs are frequently scaled down to generate improved performance, gate length and oxide thickness also decrease. MOSET's distinguishing feature is scaling, which allows for size reduction in the nanoscale realm. Scaling allows for a dimension reduction in all particular aspects, however it cannot be scaled for continue indefinitely. There is a limited scalability beyond which the gadget will provide unexpected results (X. Wang, 2016). Tunneling leak currents grow dramatically when the thickness scales are decreased, causing increased power consumption and poor device dependability. As a result, replacing and increasing the gate capacitance of SiO_2 with a high-k material is possible. Most difficulties, such as lowering gate leakage current and requiring an increased capacitance gate dielectric to manage short channel effects, may be resolved by shifting to a high-k material. Because of their thicker physical thickness, the introduction of new dielectric materials with higher dielectric constants (high-k) and identical equivalent oxide thicknesses (EOT) is promising. Because of this, WSix can be used as a metal gate and is compatible with both NMOS and PMOS devices due to engineering of the metal gate work function, as claimed in the Hong et al. (2014) patent. For more than a decade, researchers have been looking into high-k materials for gate dielectrics all over the world. To date, hafnium dioxides (HfO_2) have outperformed other high-k dielectrics in the EOT range around 1 nm. To limit short channel effects in transistors with small sizes, a higher gate dielectric capacitance is required. It has been studied to replace SiO_2 with a high-k dielectric material such as Tungsten Silicide (WSix). High-k material resulted in a reduction of dielectric thickness from 3 nm to 1 nm. High mobility could benefit graphene applications such as high-frequency transistors, sensors, optoelectronic modulators, and transparent conductive electrodes. Moreover

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researchers have introduced the graphene layer to improve current in semiconductor device design. Consequently, this graphene performance is presented to address the issues.

1.3 Research Objective

The following are the primary objectives of this study:

i. To design and simulate a 22 nm DG-MOSFET with a high-k Metal Gate (HKMG) bilayer graphene device.

ii. To analyze and optimize the threshold voltage, current drive, and current leakage of the device by using the Taguchi statistical method.

iii. To improve the electron mobility by increasing current drive and reducing current leakage by using graphene in MOSFET.

1.4 Scope of Research

The scope of this project is to design and optimize DG-MOSFETs modified from conventional MOSFETs. The design and fabrication of silicon MOSFET will be performed using SILVACO TCAD with ATHENA software while doing the simulation using ATLAS software. After the fabrication simulation, more experiments in designing the DG-MOSFET device will be performed by changing some input process parameters. Data will be collected, and the input optimizing process parameters will be done using appropriate statistical and analysis techniques. Each fabrication step and the fabrication step are very important to ensure the right DG-MOSFET device is made. Instead, it also highlights some of the features of the MOSFET that need to be studied to obtain the desired threshold voltage level (V_{TH}), current drive (I_{ON}), current leakage (I_{OFF}) - threshold swing (SS) and current ratio. In Figure 1.1, the flowchart for the scope of work for the project is shown.

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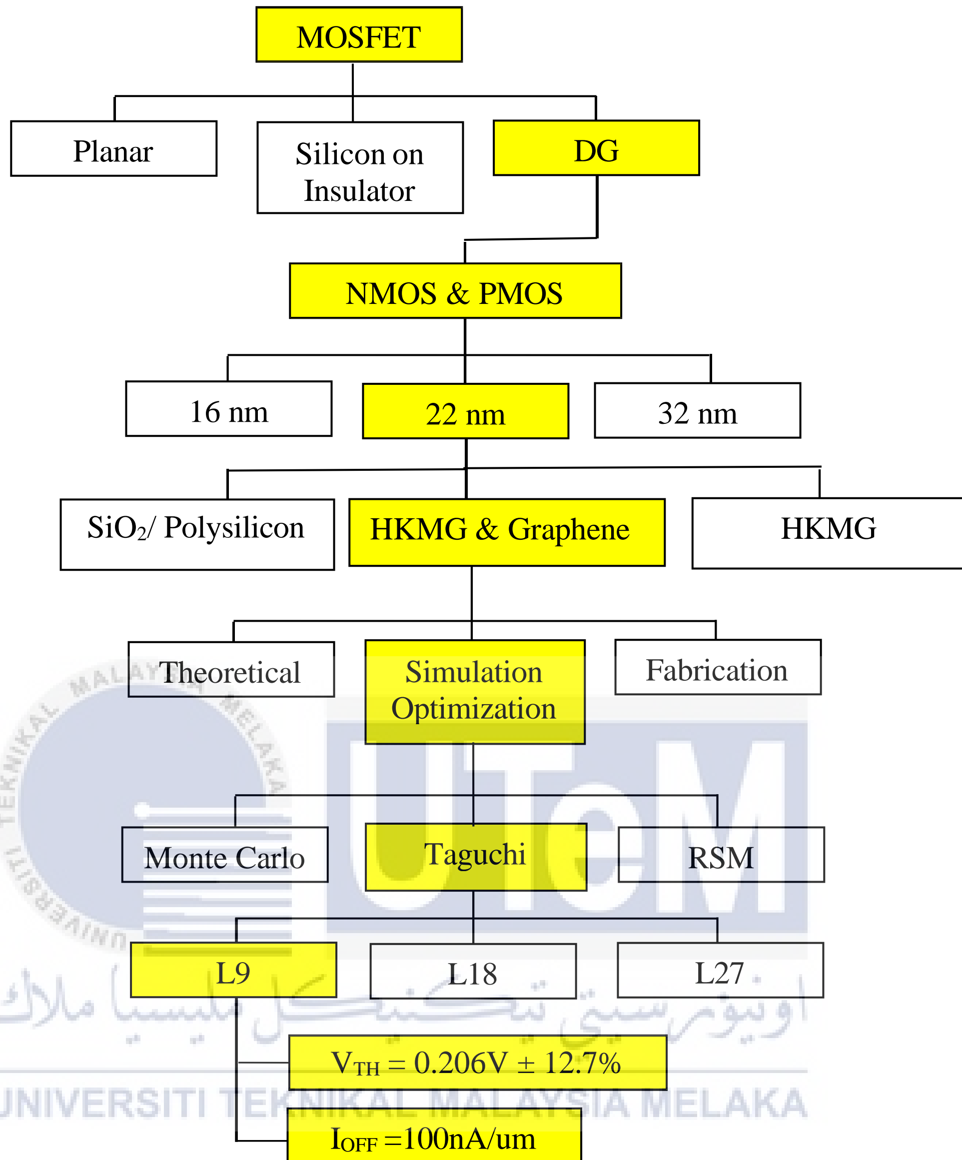

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Figure 1.1: Project's scope and design process

The execution of this analysis is based on simulation, programme development, and downscaling of a 22 nm DG PMOS and NMOS with phenomena related to device dependability and their performance by incorporating a bilayer graphene using SILVACO TCAD software. The L9 experimental array of the Taguchi method is used to look into the electrical characteristics of this device. The simulation by the ATLAS module executes