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Power losses analysis for reduced switch 9-level cascaded H-bridge multilevel inverter

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ABSTRACT

This study provides a thorough examination of power losses and total harmonic distortion (THD) in single-phase 9-level cascaded H-bridge multilevel inverters (CHB MLI) at low switching frequencies. The aim is to analyze the efficiency of a single-phase 9-level cascaded CHB MLI using three distinct switch configurations: 16-switch, 11-switch, and proposed 8-switch. The calculated switching angles are optimized using the feed-forward methodology. Two types of load conditions—R load and R-L load—are being examined. The results suggest that the proposed 8-switch design exhibits superior efficiency by limiting power losses compared to other topologies. Regarding THD, the conventional topology yields a somewhat lower value, however, the disparity is less than 1% when compared to both reduced switch topologies.

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1. INTRODUCTION

The multilevel inverter (MLI) has several advantages compared to the standard bipolar inverter [1], [2]. The voltage stress on each switch is reduced as a result of the switches being connected in series [3], [4]. Hence, by increasing the rated voltage, the overall power of the inverter can be safely augmented. Furthermore, the decrease in voltage swing during each switching cycle leads to a reduction in the rate of change of voltage (dv/dt) [5], [6]. Additionally, the increase in output levels leads to a reduction in harmonic distortion [7], [8]. Unfortunately, raising the level will result in an increase in the components, thereby leading to an increase in power losses. In order to address this problem, a high level MLI with a low switch configuration has recently been proposed [9]-[12]. The primary advantages of these topologies include a lower number of switches, cost-effectiveness, minimal losses during switching, ease of operation, and high-resolution output voltage [12], [13].

The consideration of power loss is crucial in the design of more efficient inverters, and precise calculation directly affects both the technical and economic evaluation [14], [15]. The power losses in a converter circuit include switching loss, gate loss, snubber loss, conduction loss, and off-state loss [14]. For the purpose of enhancing the efficiency and size of MLIs in the future, it is imperative to analyze the power losses [15]. This paper examines and highlights the differences in performance between a newly proposed reduced switch topology and the standard 9-level cascaded H-bridge (CHB) MLI architecture. The recommended evaluations include power losses and total harmonic distortion (THD) analysis.

2. CASCADED H-BRIDGE MULTILEVEL INVERTER TOPOLOGY

A 9-level output voltage is generated by cascading four standard H-bridge modules in a CHB MLI [16]-[18]. The topology referred to as standard or conventional topology consists of 16 switches and 4 DC sources, as depicted in Figure 1(a). Meanwhile, the proposed circuit modification in [19], depicted in Figure 1(b), showcases a switch reduction technique. It effectively reduces the number of switches by 5. This research suggests an alternative structure, depicted in Figure 1(c), that utilizes only 8 switches to achieve a further reduction in the number of switches. The switching pattern for the suggested topology is provided in Table 1. Table 2 presents a concise overview of the variations in component requirements among the three topologies of the single-phase 9-level CHB MLI.

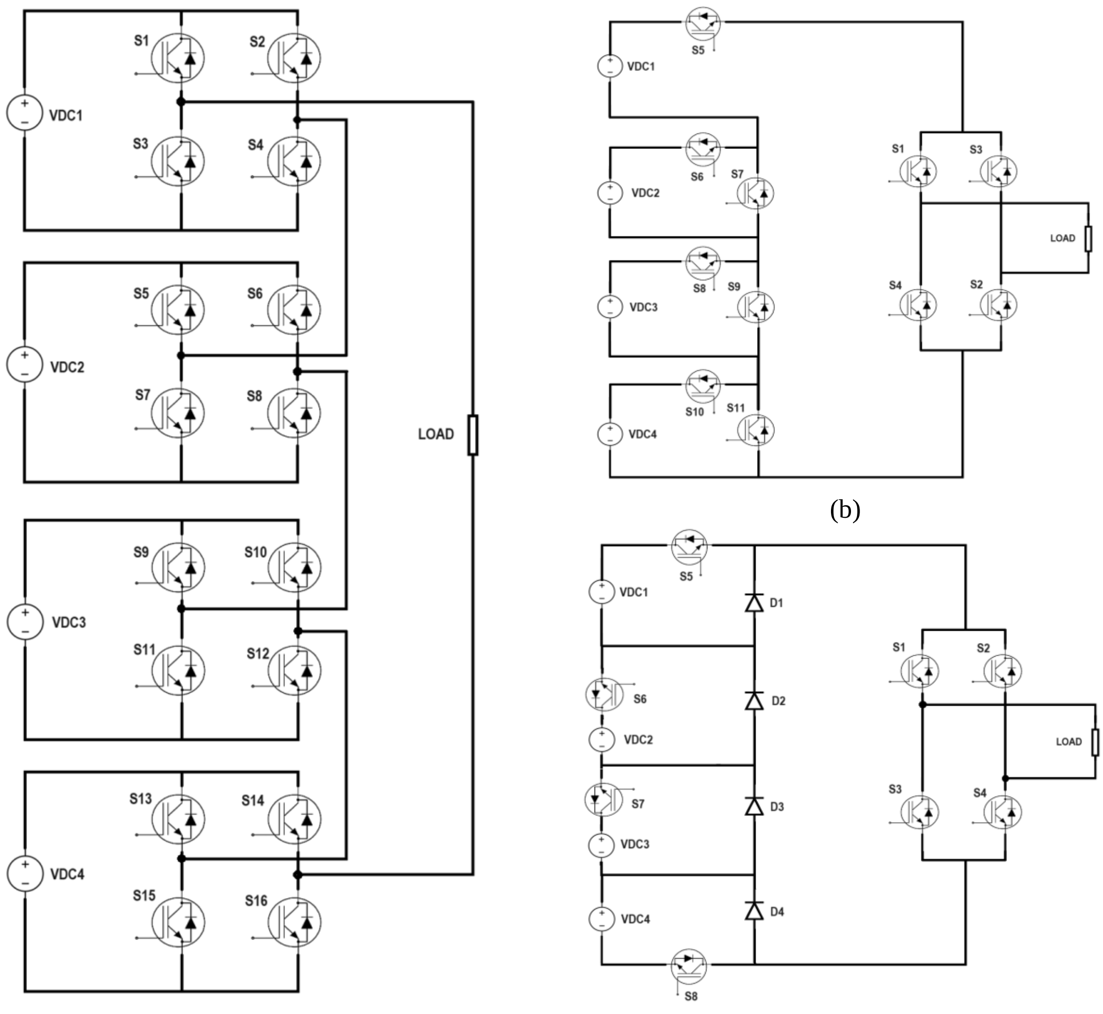

Figure 1. 9-level CHB MLI topologies (a) conventional, (b) 11-switch, and (c) proposed 8-switch

Table 1. Proposed 8-switch CHB MLI switching patterns

Output voltage	Switch status (1 – ON)							
	S1	S2	S3	S4	S5	S6	S7	S8
+4 VDC	1	1	1	1	1	1	1	1
+3 VDC	1	0	0	1	1	1	1	0
+2 VDC	1	0	0	1	1	1	0	0
+1 VDC	1	0	0	1	1	0	0	0
0 VDC	0	0	1	1	0	0	0	0
-1 VDC	0	1	1	0	1	0	0	0
-2 VDC	0	1	1	0	1	1	0	0
-3 VDC	0	1	1	0	1	1	1	0
-4 VDC	0	1	1	0	1	1	1	1

Table 2. List of components for conventional and reduced switch topologies

Components	Conventional	11-Switch	8-Switch
Insulated gate bipolar transistor (IGBT)	16	11	8
Gating block	16	11	8
DC voltage source	4	4	4
Number of H-Bridge	4	1	1
Diode	0	0	4

3. SWITCHING ANGLES OPTIMIZATION USING FEED FORWARD METHOD

Switching angle has a substantial impact on the harmonic generated by the output voltage [20]-[22]. Inadequate planning of the switching angle might result in issues related to suboptimal power quality and an increase in overall harmonic distortion [22], [23]. The total switching angles required for the output voltage can be determined using (1) based on the quarter wave symmetry analysis.

$$SA = \frac{(m-1)}{2} \tag{1}$$

Where SA is the total switching angles required for quarter wave symmetry and m is the CHB MLI level number.

The utilization of a feed-forward method (FFM) allows for the generation of switching angles and high-quality output voltage waveforms, hence circumventing the limitations [23], [24]. The primary objective of this technique is to reduce the disparities between waveforms with negative and positive polarity, as well as the overall contour of the waveform [24]. The FFM exhibits a THD percentage when compared to other methods for computing switching angles. The mathematical expression used to calculate the switching angle is presented in (2) [23].

$$a_i = \frac{1}{2}\left[sin^{-1}\left(\frac{2i-1}{m-1}\right)\right] \tag{2}$$

Where i is the angle numbers. Table 3 summarizes the value of the main switching angles of the CHB MLI obtained by FFM.

Table 3. Switching angles value

Switching angle	Value
α_1	3.59
α_2	11.01
α_3	19.34
α_4	30.52

4. POWER LOSSES FORMULATION

The four fundamental types of power losses that occur during the operation and switching of power components in a power circuit are conduction loss, off-state loss, switching loss, and gate loss [25]. The negligible value of off-state loss and gate loss is commonly overlooked [15]. Conduction loss pertains to the energy losses that occur when a device is in its active or conducting condition [14]. The cumulative conduction loss of an MLI is the aggregate of the individual losses incurred by its components during the conduction period. Thus, the multiplication of the on-state saturation voltage (V_{on}) and the on-state current (I_{on}) can be employed to indicate the power loss [14].

$$P_{conduction} = P_{cond(IGBT)} + P_{cond(Diode)} \tag{3}$$

$$P_{conduction} = (V_{CE} \times I_C) + (V_D \times I_D) \tag{4}$$

Switching loss occurs due to sluggishness in transitioning from the off state to the on state and vice versa. Switching loss is the result of combining the average IGBT turn-off loss, IGBT turn-on loss, and diode reverse recovery loss. The losses can be computed using the switching energy equations, which are dependent on the switch current [14].

$$P_{switching} = P_{turn-ON} + P_{turn-OFF} + P_{r\,ec.diode} \tag{5}$$

$$P_{switching} = \left[(E_{turn-ON} + E_{turn-OFF}) \times f_{sw(IGBT)}\right] + \left[E_{rect.diode} \times f_{sw(diode)}\right] \tag{6}$$

Figure 2 illustrates the schematic representation of the process for calculating the overall power losses associated with each switch. The simulation result can immediately provide all the power loss information from the switch. The losses in the IGBT module can be categorized into two primary components: the IGBT itself and the diode. During circuit operation, both the IGBT and diode will produce conduction and switching losses. To account for the entire power losses of each switch, the combined losses in both the IGBT and diode can be summed together [25].

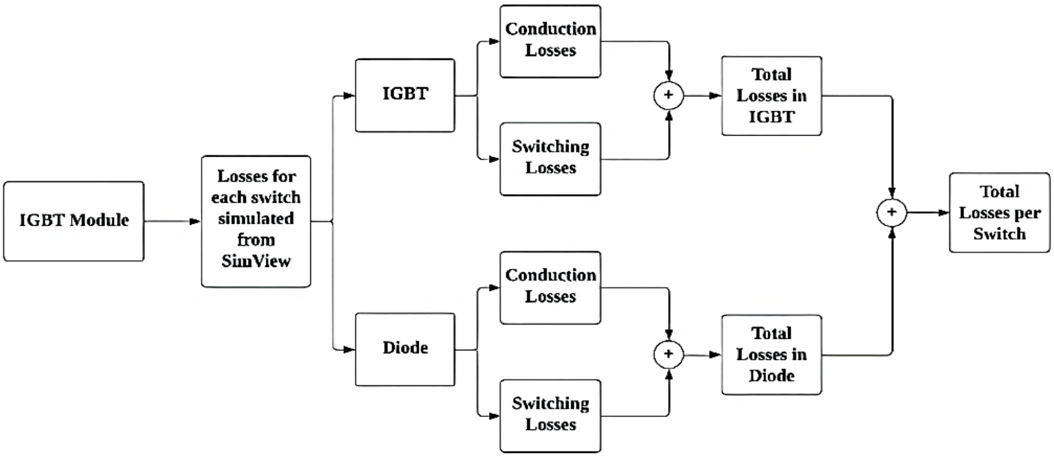

Figure 2. Flow model for the loss’s calculation [14]

5. RESULTS AND DISCUSSION

By incorporating the switching angles derived from the FFM approach in Table 3 into the simulation circuit for all topologies, all the required data such as THD and power losses are obtained. Two distinct loads are being tested, first with a resistive (R) load and subsequently with a resistive-inductive (RL) load. The parameters used in the simulation are listed in Table 4.

Table 4. Simulation parameters

Parameter	Value/model
IGBT	FZ825R33HE4D.
IGBT thermal resistance	0.007 ℃/W
Diode	150EBU04
Ambient temperature	30 ℃
R-load	60 Ω
L-load	20 mH

Figure 3 displays the THD values acquired for all circuit configurations under No load, R load, and R-L load circumstances. Examined this figure, it becomes evident that the pattern of THD values is nearly the same. The typical cascaded CHB MLI exhibits the lowest THD for both load circumstances, with the 11-switch design ranking second. The proposed architecture exhibits the largest THD throughout all load conditions, despite having the lowest THD value when there is no load. Nevertheless, the disparity in value is between 0.24% and 1.01% between the standard methods, which is not particularly significant.

Figure 4 displays the simulated losses for all topologies under load circumstances. The impact of switching losses on overall losses is reduced due to the smaller number of switching transitions required to achieve the output voltage. The total power losses of the suggested 8-switch design were 11.8 W in the R-L load configuration and 12 W in the R load configuration. Both numbers are the lowest compared to the other two topologies, where the conventional topology resulted in the highest total losses of 17.1 W and 17 W for the R-L and R loads configurations, respectively. The increased number of losses can be attributed to the utilization of a greater quantity of active components during the circuit's development, as indicated in Table 2.

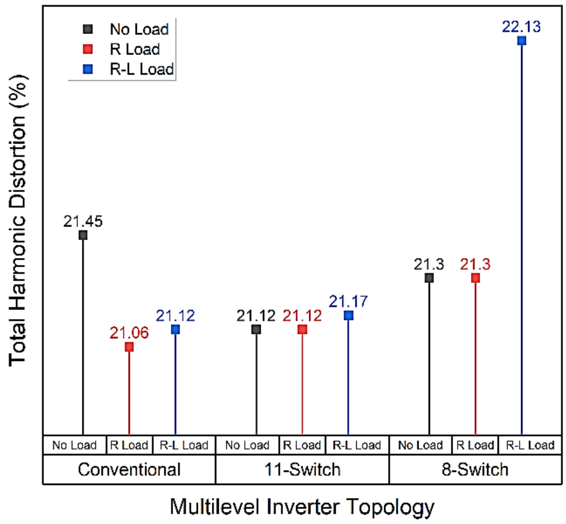

Figure 3. THD values

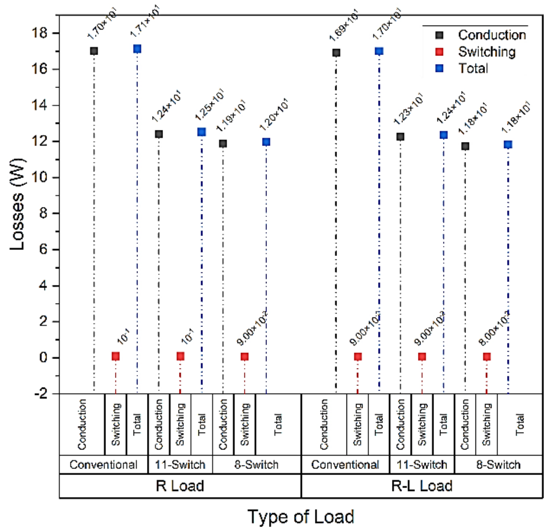

Figure 4. Analysis of losses

6. CONCLUSION

This work presents a simulation of three different CHB MLI topologies: conventional, 11-switch, and 8-switch. The THD and power losses are recorded and compared. When evaluating the load circuits (R and RL loads) in THD analysis, the conventional switch topology demonstrates superior performance compared to the reduced switch topologies (11-switch and 8-switch). Regarding power losses, the proposed 8-switch architecture outperforms the other two topologies. In general, both reduced switch topologies effectively minimize power dissipation, hence enhancing system efficiency.

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