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RESEARCH ARTICLE

Thermal Analysis and Switching Performance of a 1.7 kV SiC Power MOSFET Under High-Frequency Operation and Double Pulse Testing

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ABSTRACT This study presents a comprehensive simulation analysis of 1.7 kV SiC Power MOSFETs (SiC) compared to conventional Si power MOSFETs (Si1 and Si2) focusing on thermal behavior, switching performance, and efficiency under various operating conditions. LTspice simulations over 5000 switching cycles revealed that the SiC MOSFET exhibited lower conduction losses and superior thermal stability, with higher thermal fluctuations at 50 kHz (0.32664 °C per cycle) due to prolonged on-times, while higher frequencies at 200 kHz reduced fluctuations to 0.13397 °C per cycle. Meanwhile, under the same conditions, Si MOSFETs experience higher power dissipation and poorer thermal management. Double pulse testing at varying temperatures demonstrated the SiC MOSFET has superior efficiency, peaking as high as 99.61 %, 99.55 %, and 99.44 % at 500 V, 1000 V, and 1500 V, respectively, at 150 °C. A boost converter test using a 0.5 mH inductor and 200 μF capacitor further evaluated energy conversion performance, showing minimal voltage deviation in SiC MOSFETs, with outputs of 1359.32 V, 1360.57 V, and 1358.56 V at 25 °C, 100 °C, and 150 °C, respectively, compared to the theoretical 1360 V, while Si MOSFETs displayed greater voltage drops and efficiency losses. These results confirm that SiC Power MOSFETs provide significantly higher efficiency, lower thermal resistance, and superior performance in high-voltage, high-power applications compared to conventional Si MOSFETs.

INDEX TERMS $R_{DS(ON)}$, SiC power MOSFETs, thermal fluctuation, switching energy, double pulse test, boost converter.

I. INTRODUCTION

Innovation in power electronics is driven by the need for more efficient and reliable devices. Silicon carbide (SiC) power MOSFETs, with superior material properties, are ideal for high-voltage, high-frequency, and high-temperature applications such as electric vehicles, renewable energy, and industrial systems. Commercialize SiC power MOSFETs has demonstrated blocking voltages exceeding 15 kV, with commercially available devices operating between 650 V and 1.7 kV, handling currents up to 125 A and sustaining maximum junction temperatures at 175 °C [1]. Their advantages over silicon devices, such as lower on-resistance and faster switching, allow them to be a key technology in modern power electronics. However, thermal effects remain a major challenge, as high temperatures and self-heating increase electro-thermal stress, thus leading to degradation mechanisms such as, metallization defects and bonding wire lift [2], [3].

To address these issues, this study uses LTspice simulator software to simulate the thermal and electrical behavior of 1.7 kV SiC MOSFETs. The simulations are validated against datasheet specifications to ensure accuracy. The key aspects of the research include an in-depth analysis of the switching

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characteristics and thermal impact of the SiC MOSFET, highlighting its efficiency and robustness in high-performance applications. Furthermore, the study compares the SiC MOSFET's performance with that of a Silicon power device, offering insights into their relative advantages and trade-offs. The research also includes comprehensive documentation and reporting of findings to contribute to the understanding and advancement of energy-efficient and thermally optimized electronic systems.

Additionally, the large bandgap of SiC contributes to its exceptional high-temperature stability, enables it to be an ideal choice for applications unlike conventional semiconductor materials such as silicon (Si) and gallium arsenide (GaAs) which suffer from performance degradation at elevated temperatures [2], [4], [5]. These advantages, combined with lower on-resistance, make SiC a preferred material for high-power and high-frequency applications, enabling advancements in energy-efficient systems, automotive powertrains [6], [7].

Over the past few years, numerous simulations on SiC power MOSFETs have been carried out. Simulation is one of the most widely used operations research and management science techniques [8]. Alhalabi et al. [9] uses LTspice to generate I-V characteristics for the MOSFET. They report that at low VGS values, the drain current increases as the temperature rises because the threshold voltage in this area controls the current, which has a negative proportionality to temperature and a positive proportionality to it. Similarly, a comparison between the power losses of a commercial SiC MOSFET device to a conventional Si IGBT module with a similar power rating is conducted by [10]. The results show the SiC MOSFET circuit demonstrated better performance due to its smaller size, increased efficiency, and reduced power loss. The findings illustrate the possible uses of SiC technology in high-voltage direct current applications.

Herein, we study the electro-thermal behavior of a 1.7 kV SiC power MOSFET through LTspice simulations, analyzing its switching characteristics, thermal stress, and efficiency in high-voltage applications. By varying junction temperature, switching frequency, and gate drive conditions, we assess self-heating effects and temperature-dependent variations in key parameters such as on-resistance ($R_{DS(ON)}$), threshold voltage (V_{TH}), and switching losses.

II. SIMULATION METHOD

Utilizing the advantages of both simulation tools, the study seeks to offer a thorough analysis of the device's functionality and thermal behavior from a theoretical and practical standpoint. Taking into consideration actual conditions as well as the intricate relationships between electrical and thermal effects, the simulations are made to reproduce the electrical and thermal responses of the device. Accurate thermal and electrical evaluations of the SiC device depend on the data collection procedure, which includes exhaustive virtual testing via simulations. Table 1 shows the device parameters used in this simulation setup.

TABLE 1. Device parameter.

Material	Device (DESIGNATION)	$V_{DS(max)}$ (V)	I_{DS} (A)	$R_{DS(ON)}$ (mΩ)
SiC	C2M0045170P (SiC)	1700	75	40
Si	STW11NM80 (Si1)	800	11	400
	BSZ42DN25NS 3 (Si2)	250	5	425

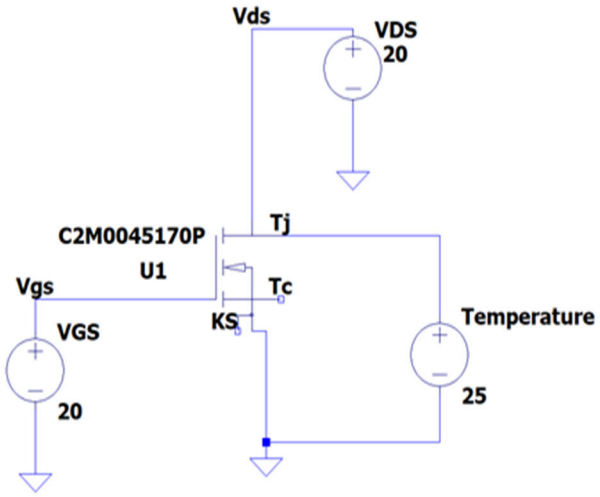

FIGURE 1. Power MOSFET I-V curve circuit in LTSPICE.

The simulation setup includes a DC sweep of the SiC gate-source voltage (V_{GS}) and drain-source voltage (V_{DS}) to extract its output (I_{DS} vs. V_{DS}) and transfer (I_{DS} vs. V_{GS}) characteristics under varying junction temperatures (Tj) as shown in Fig. 1. Stepping Tj from −40 °C to 150 °C provides an in-depth evaluation of its thermal performance. The transfer characteristics are analyzed by sweeping VGS from 0 V to 14 V in 10 mV steps, while output characteristics are obtained by sweeping V_{DS} from 0 V to 100 V for V_{GS} values between 7 V and 15 V. This allows a detailed study of the MOSFET's linear and saturation regions and temperature effects on key parameters like on-resistance and threshold voltage.

Beyond IV characterization, simulations assess switching behavior during turn-on/off transients to evaluate thermal stability and switching efficiency. The same test setup is repurposed to observe thermal fluctuations across switching frequencies, ensuring consistency. Key conditions include a fixed V_{GS} of 10 V and V_{DS} of 20 V. Thermal performance is studied across switching frequencies from 50 kHz to 200 kHz over 5000 cycles to detect temperature variations and thermal instabilities. The simulation follows three steps: (1) Initialization, where circuit parameters are set based on IV tests; (2) Frequency Variation, adjusting switching frequency incrementally; and (3) Thermal Analysis, monitoring Tj over extended cycles. This integrated approach provides a

comprehensive understanding of the MOSFET's behavior in high-power applications.

Double pulse testing (DUT) is commonly used to evaluate MOSFET switching characteristics [11], [12], [13], providing insights into efficiency and thermal behavior in power electronics [14]. The setup includes a high-voltage DC source, a power MOSFET as the DUT, a freewheeling diode, an inductor, and a capacitor, replicating a realistic switching environment. During the first pulse (T1), the DUT conducts, allowing current to rise linearly through the inductor. When it turns off, stored inductor energy forces current through the freewheeling diode, revealing turn-off characteristics like voltage overshoot due to inductive energy and parasitic capacitances [15]. In the off period (T2), the current circulates through the diode, ensuring continuous load current while allowing the DUT to stabilize. The second pulse (T3) reactivates the DUT, resuming inductor current flow and assessing turn-on behavior, including switching losses, delays, and overshoots.

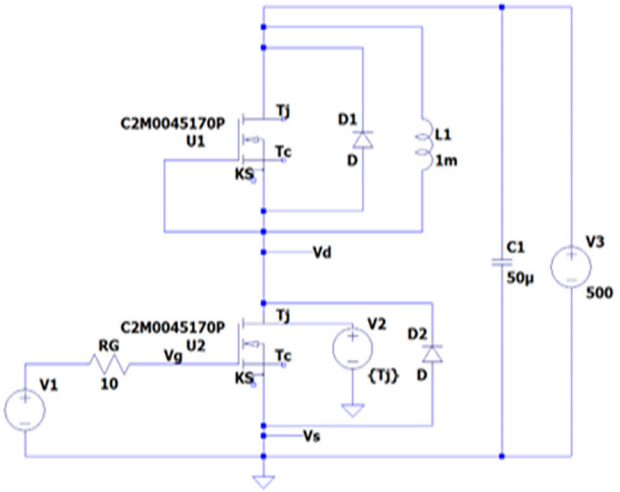

FIGURE 2. Double Pulse Test Circuit Setup with SiC as Device Under Test (DUIT).

The double pulse testing setup as shown in Fig. 2, utilizes the SiC as both the main switch (U1) and for freewheeling (U2). A 1 mH inductor (L1) simulates an inductive load; while freewheeling diodes (D1, D2) enable current flow during switching. A 50 μF decoupling capacitor (C1) stabilizes the DC bus voltage, which varies between 500 V, 1000 V, and 1500 V. The MOSFET operates with a 10 V gate drive voltage (V_{GS}) and a 10 Ω gate resistor (RG) to control switching speed and mitigate ringing. LTspice simulations analyse performance across junction temperatures from 25 °C to 300 °C, focusing on $R_{DS(ON)}$ and switching behaviour.

The boost converter increases input voltage while minimizing energy loss using an inductor, MOSFET switch, diode, and output capacitor, controlled via pulse width modulation (PWM) [16]. During the ON state, the inductor stores energy, while in the OFF state, it releases energy to the load, boosting output voltage. The capacitor smooths voltage ripples for stable DC output. This study compares SiC and Si MOSFET performance by evaluating output voltage stability and accuracy at various temperatures (25 °C, 100 °C, 150 °C). The percentage error between calculated and simulated output voltages assesses thermal resilience and efficiency, particularly in high-temperature environments.

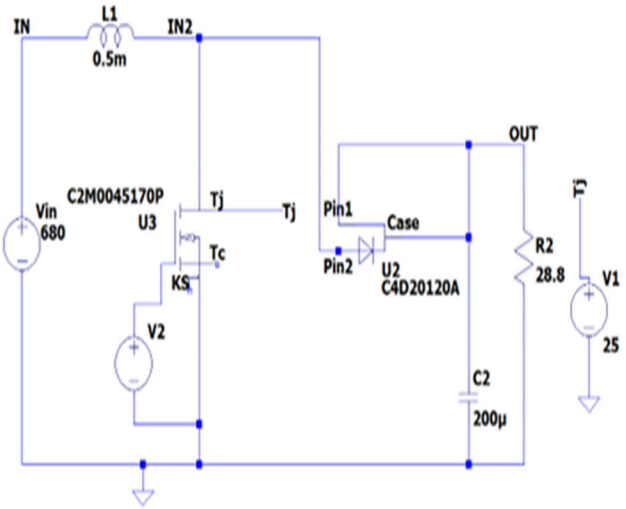

FIGURE 3. Double Pulse Test Circuit Setup with SiC as Device Under Test (DUIT).

Fig. 3 shows the boost converter circuit that includes several key components that work together to step up the input voltage efficiently and achieve a stable, higher output voltage. The input voltage source (Vin) provides the DC input, while the pulse voltage source (V2) controls the switch operation based on a specified duty cycle (D). The inductor (L1) stores energy during the switching cycle and helps boost the voltage. The SiC (U3) serves as the main switching element, and the SiC Schottky diode (C4D20120A, U2) prevents reverse current flow, ensuring energy is properly transferred to the output. The output capacitor (C2) smooths the output voltage, reducing ripple, and the load resistor (R2) represents the connected load. Additionally, a reference temperature source (V1) monitors or manipulates the system's temperature-dependent variations, ensuring stable performance under varying thermal conditions.

Performance comparisons between traditional silicon (Si) power devices and the SiC Power MOSFET are studied in this setup. This comparison will shed light on the potential advantages and disadvantages of SiC technology, particularly concerning general dependability, efficiency, and thermal performance. We can better grasp the trade-offs involved in selecting SiC technology for specific applications by contrasting the SiC MOSFET with conventional Si devices.

III. RESULTS AND DISCUSSION

The transfer characteristic curve, shown in Fig. 4, behaves differently than silicon power MOSFETs. The threshold voltage in silicon devices exhibits a negative temperature dependence, which causes the transfer characteristic curves to

cross over as the temperature rises. With SiC devices, on the other hand, the threshold voltage exhibits a positive temperature dependence, leading to parallel shifts in the transfer characteristics without any crossover.

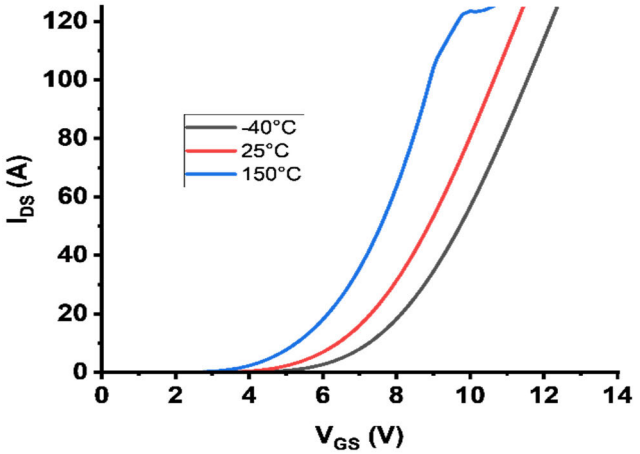

FIGURE 4. Transfer characteristics at different junction temperatures.

This may occur due to the bandgap narrowing effect, resulting in threshold voltage decreased. This is because the thermal energy of the material's electrons increases with temperature, causing them to shift from the valence band to the conduction band. The Fermi level of a MOSFET also fluctuates with temperature due to bandgap variations. The material becomes more conductive as the Fermi level approaches the conduction band at higher temperatures, causing the bandgap to narrow. This increases the number of electrons in the conduction band, causing the bandgap to decrease.

Fig. 5 shows that the on-resistance ($R_{DS(ON)}$) increases steadily with the junction temperature (Tj) [17]. This is explained by basic semiconductor physics, specifically how temperature affects charge carrier behaviour. As the temperature rises, the semiconductor material's lattice vibrations also rise. As a result, charge carriers become more dispersed, which lowers their mobility (μn) [18], [19]. The following equation can be used to express the relationship:

$$R_{DS(ON)} \propto \frac{1}{\mu_n} \tag{1}$$

Conduction losses increase as the MOSFET's temperature rises because $R_{DS(ON)}$ also rises with it. In a later section, this increase in Ploss at different temperatures will be investigated. In high-power applications where the MOSFET is managing high currents, this has a significant impact. The efficiency of the power converter or inverter is limited by increased conduction losses because more energy is lost as heat. The findings of the thermal fluctuation simulations offer important new information about the MOSFET device's switching performance and thermal behaviour at different switching frequencies. The study illustrates the crucial influence of switching frequency on thermal stability and

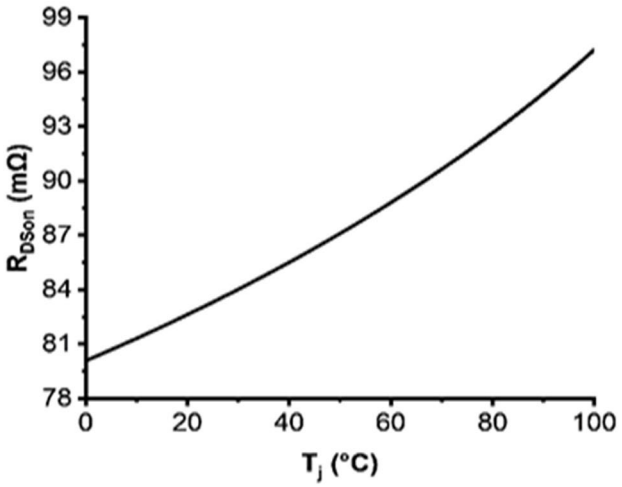

FIGURE 5. Drain-source on resistance, $R_{DS(ON)}$ increase as junction temperature, Tj increase.

energy dissipation by analysing the junction temperature over 5000 cycles.

According to Fig. 6, higher switching frequencies demonstrate better thermal stability with fewer fluctuations, while lower frequencies show higher junction temperatures and more noticeable thermal fluctuations, which are ascribed to longer on-times.

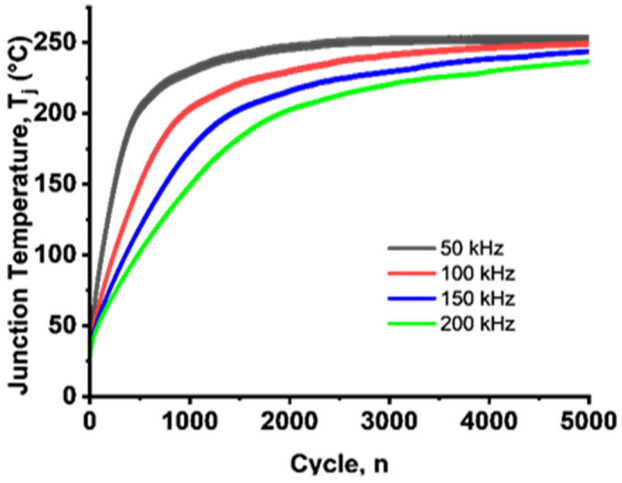

FIGURE 6. Thermal Fluctuation at 5000 cycles.

TABLE 2. Junction temperature slope.

Frequency (kHz)	$\frac{dT_j}{cycle}$ $\frac{°C}{cycle}$	Error
50	0.32664	± 0. 733 m
100	0.22327	± 0.300 m
150	0.16505	± 0.223 m
200	0.13397	± 0.221 m

Higher switching frequencies reduce the rate of temperature increase per cycle (dTj/cycle), enhancing thermal stability by minimizing heat accumulation. This inverse relationship between frequency and thermal buildup highlights

the efficiency of operating the MOSFET at higher frequencies. Longer cycles allow more heat accumulation, increasing peak-to-peak thermal fluctuations, as seen in lower-frequency results. The small error values further validate the simulation's accuracy and reliability. Both material properties and operating conditions influence SiC MOSFET thermal behavior. 4H-SiC's high thermal conductivity (3.7 W/cm°C) and diffusivity (1.7 cm^2/s) enable efficient heat dissipation [20], making it ideal for high-performance applications.

However, this isn't always enough to control thermal performance. In this context, the power loss mechanisms are important. Depending on the $R_{DS(ON)}$, conduction losses happen as current passes through the MOSFET's channel and produces heat. As equation (3.2) indicates, any resistance in the current's course causes more power to dissipate and hence, heat up the devices. Switching losses occur during the MOSFET's on/off transitions and can be substantial, particularly at higher switching frequencies where each switching event increases the total power dissipation [14], [21]. Even though they are often lower, gate-drive losses also add to the total heat produced by charging and discharging the gate capacitance.

$$P_{conduction} = R_{DS(ON)} \times I_D^2 \propto \frac{1}{\mu_n} \tag{2}$$

Additionally, the possibility of current spikes should be considered. Brief current spikes can occur as a result of switching events, even in cases where early observations reveal no spikes. Despite their potential short duration and lack of visibility in the averaged drain current measurements, these spikes can result in localized heating and increased thermal fluctuation [22]. The circuit's parasitic capacitances and inductances are usually the source of these spikes. The product's thermal resistance and thermal capacitance play a significant role in determining the device's rate of heating and cooling, according to previous research on the dynamic thermal behavior of MOSFETs [23]. To efficiently predict the ΔT, the subsequent formula is employed [23]

$$\Delta T = P_{loss} \times P_{thJC} \tag{3}$$

where Z_{thJC} is the device's transient thermal impedance.

The importance of considering both steady-state and transient thermal reactions is also emphasized in the note. Optimizing heat sink designs and choosing the appropriate thermal interface materials are essential for ensuring efficient heat dissipation. The effects of thermal cycling and the necessity of understanding dynamic thermal behaviour for reliable operation in real-world applications are also discussed in the document.

The results of the double pulse test, which measures turn-off at the end of the first pulse and turn-on at the start of the second, demonstrate the rate of change of VDS and IDS during its switching event. The power loss during the switching event can be estimated from the rate of change, as illustrated in Fig. 8; thus, the device's efficiency can be computed across a range of junction temperatures, Tj and VDD.

Fig. 7 displays the overall double pulse test waveform for VDD of 500 V and 25 °C. The turn-on and turn-off transitions are depicted in Fig. 8(a)–(b), respectively. The voltage and current of the devices are recorded while they are shutting off following the end of the first pulse. The voltage and current of the device during the turn-on transient are also recorded, and the device is turned back on after a short break. The voltage rises at a rate of 6.01 V/ns and the current falls at a rate of 0.054 A/ns during the turn-off transient. The voltage drops at a rate of 7.77 V/ns and the current rises at a rate of 0.052 A/ns during the turn-on transient.

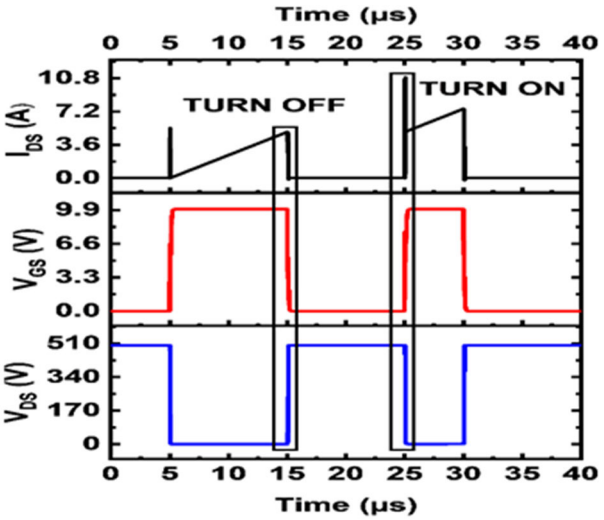

FIGURE 7. Double pulse output during complete one test cycle.

During the MOSFET's turn-on and turn-off transients, the voltage and current waveforms are recorded. The instantaneous power (P=IV) is calculated by multiplying the voltage and current values at each time point. Specifically, during turn-on, V_{DS} drops rapidly while I_{DS} increases sharply, causing a significant transient power spike due to the simultaneous presence of high voltage and current. Additionally, the higher dV_{DS} / dt in turn-on suggests faster switching, which can lead to increased losses from parasitic inductances and capacitances. Conversely, during turn-off, I_{DS} decreases while V_{DS} rises, but the overlap period is shorter and results in lower peak power dissipation compared to turn-on.

To determine the energy dissipation during these transitions, the area under the power curve, which displays the integration of power over time is computed. Since the power function P(t) is continuous, but its exact mathematical expression is typically unknown in simulations, the integration is approximated using the trapezoidal rule. This numerical technique divides the area under the curve into small trapezoids and adds them up to obtain an accurate estimate of the total energy dissipation.

$$E = \int_{t1}^{t2} P(t)\, dt \tag{4}$$

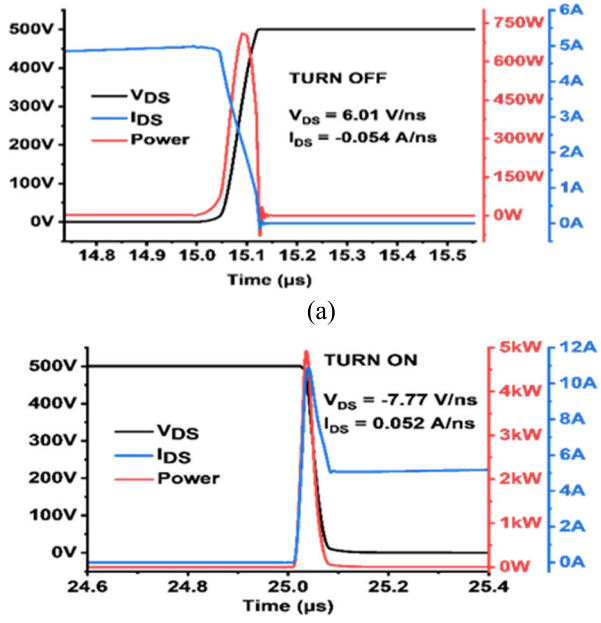

FIGURE 8. Device voltage, current and power during: (a) turn off; (b) turn on.

$$E = \sum_{i=1}^{n-1} \frac{P(t_i) + P(t_{i+1})}{2} \times \Delta t \tag{5}$$

To calculate the power loss from the energy dissipated during switching transitions, the following operation is applied:

$$P_{switch} = E \times f_{sw} \tag{6}$$

The results of this simulation are supported by an observation made by Ganesan et al. in their double-pulse test setup, which shows that switching loss increases as V_{DS} and I_{DS} increase [24]. The impact of junction temperature on switching loss was also discussed by the author, who advised maintaining the device's safe limit to guarantee operation.

The data obtained can be used to compute and tabulate the device's efficiency. The following formulas can be used to determine the MOSFET's overall efficiency under different circumstances:

$$n = 1 - \frac{P_{total\ loss}}{P_{in}} \times 100 \tag{7}$$

where,

$$P_{in} = I_{drms}(V_{DD}) \tag{8}$$

$$P_{total\ loss} = P_{conduction} + P_{switch} \tag{9}$$

And,

$$P_{conduction} = I_{drms}^2 + R_{DS(ON)} \tag{10}$$

By applying this equation, the efficiency of the device at V_{DD} and Tj as mentioned previously, are shown below:

The efficiency graph on Fig. 9 shows the device achieving peak efficiencies of 99.61 %, 99.55 %, and 99.44 % at V_{DD} values of 500 V, 1000 V, and 1500 V, respectively, at 150 °C

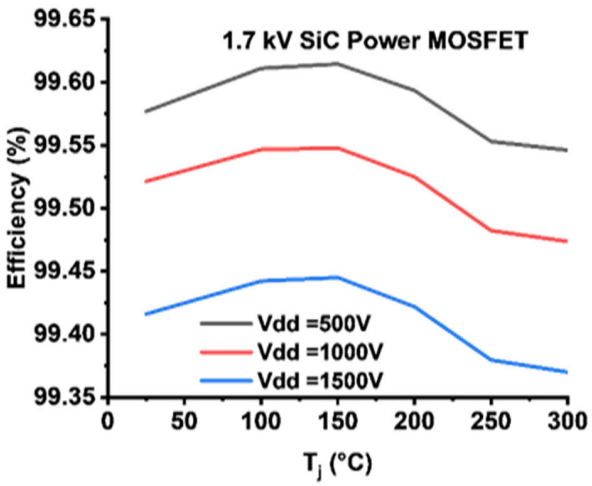

FIGURE 9. 1.7kV Power MOSFET efficiency during double pulse test.

before declining. While $R_{DS(ON)}$ increases with temperature due to reduced carrier mobility, the modest efficiency gain at moderate temperatures suggests sharper reductions in switching losses. Bandgap narrowing at higher temperatures lowers the threshold voltage [25], enhancing turn-on/off dynamics and carrier injection, which reduces transitional energy loss and partially offsets higher conduction losses.

At lower V_{DD}, conduction losses dominate, and efficiency gains from reduced switching losses are less pronounced as $R_{DS(ON)}$ rises. At higher V_{DD}, switching losses become more significant, and efficiency declines more sharply at elevated temperatures as thermal improvements in switching dynamics fail to offset total power losses. The peak efficiency at 150 °C reflects a balance between reduced switching and increased conduction losses, demonstrating the thermal resilience and operational limits of SiC devices in high-performance applications.

Using the double pulse test, a prior test method, this section compares the efficiency and thermal behaviour of SiC and Si devices, emphasizing the variations in how they react to high voltage and temperature. The device under test for SiC power MOSFET is the same device that was used throughout the study, which is SiC while the Si device is Si1 and Si2 as shown in Table 1.

As shown in Fig. 10, the device's efficiency is directly related to its characteristics and operating environment [26]. Because of its low $R_{DS(ON)}$ and thermal resistance, the SiC1 performs better by 0.2 % along with an increased V_{DD} percentage. The slight difference may result in a larger overall energy savings and improved long-term reliability, especially in high-power applications where efficiency losses translate to significant thermal stress. These attributes allow it to handle high voltages and currents with minimal conduction losses and efficient heat dissipation. As a result, the SiC device maintains high efficiency across all V_{DD}. This aligns with the inherent advantages of SiC, such as its wide bandgap, higher breakdown voltage, and lower intrinsic carrier concentration, making it ideal for high-power applications.

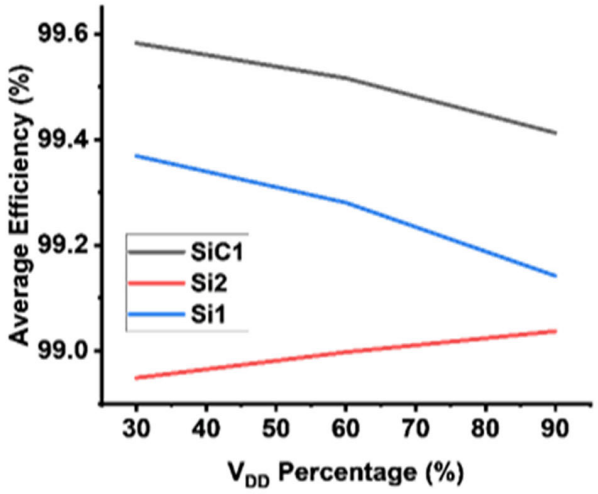

FIGURE 10. Average efficiency between SiC and Si device.

The Si devices, on the other hand, have notable drawbacks. Higher conduction losses and increased thermal stress at higher loads are caused by the Si1 lower $R_{DS(ON)}$ of 0.4 Ω and thermal resistance of 0.83 °C/W. Losses are exacerbated by the Si2 even higher $R_{DS(ON)}$ of 425 mΩ and thermal resistance of 3.7 °C/W. Even though the Si2 efficiency increases as V_{DD} rises, this is probably because higher loads cause it to function closer to its ideal design range. Its limited thermal management capabilities and higher conduction losses, however, continue to limit its overall performance. The disparity in patterns illustrates how the characteristics and design of the device affect its efficiency under different V_{DD} loads. Because of their higher $R_{DS(ON)}$ and thermal resistances, Si devices are more susceptible to thermal and electrical stress, even though SiC devices have lower conduction and switching losses. These findings underscore the advantages of SiC in high-voltage and high-power applications while highlighting the operational constraints of Si devices in such scenarios.

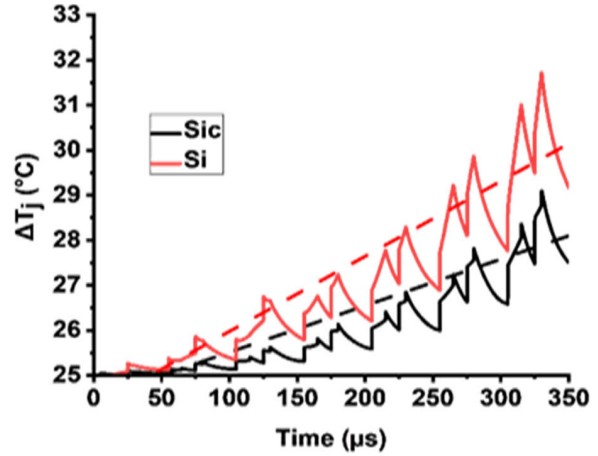

FIGURE 11. Thermal stress of SiC and Si device at 10 double pulse test cycle.

Fig. 11 comparing the thermal stress of SiC and Si devices during the double pulse test cycle demonstrates the notable differences in their thermal performance. The SiC device exhibits a lower and more stable temperature increase of 0.01033 °C/μs in comparison to the Si device, which exhibits larger and more unpredictable temperature changes up to 0.01668 °C/μs. Since the SiC has a higher thermal conductivity of 380 W/m·K compared to Si 131 W/m·K, the heat effectively dissipates during high-power events, according to earlier research. SiC's superior thermal conductivity reduces the device's exposure to thermal stress by making it simpler to control the heat generated during switching operations [27], [28]. The SiC device's improved thermal management capabilities are demonstrated by the slower and more steady temperature rise that was seen during the double pulse test. Because of this, SiC MOSFETs are better suited for high-power and high-temperature applications where reliable and efficient heat dissipation and thermal stability are essential.

The performance of the boost converter was investigated at various temperatures for both SiC and Si-based devices. The converter was designed with a target output voltage (V_{OUT}) of 1360 V and an input voltage (V_{IN}) of 680 V at a duty cycle (D) of 0.5. The following equation was used to determine the output voltage:

$$V_{out} = \frac{V_{in}}{1 - D} \tag{11}$$

Fig. 12 displays the output waveform of the SiC-based boost converter. At a temperature of 25 °C, the simulated output voltage was 1359.32 V. The estimated simulated output voltages at higher temperatures of 100 °C and 150 °C are 1360.57 V and 1358.56 V respectively.

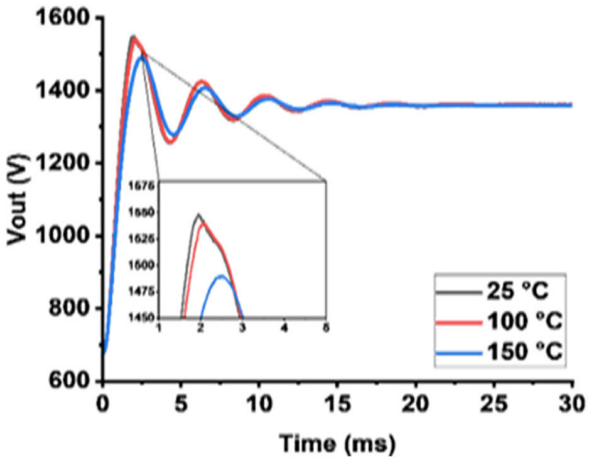

FIGURE 12. SiC performance in a boost converter under different temperature conditions.

Fig. 12 illustrates these findings, which demonstrate the exceptional thermal stability of SiC devices. The low $R_{DS(ON)}$ and lower conduction losses of SiC power MOSFETs are the cause for the output voltage's minimal variation over the temperature range. The output waveform's transient response showed a momentary overshoot before stabilizing at the target voltage level. This performance demonstrates that SiC-based

boost converters are dependable and efficient, which qualifies them for high-voltage and high-temperature applications. The inset graph in Fig. 12 provides a closer view of the transient response, highlighting the overshoot in V_{OUT} during the first few milliseconds. The curves at different temperatures which is 25 °C, 100 °C, and 150 °C show minimal deviation, demonstrating the excellent thermal stability of SiC MOSFETs. The overshoot is slightly higher at lower temperatures, but the differences are marginal, indicating that SiC devices maintain stable operation across a wide temperature range.

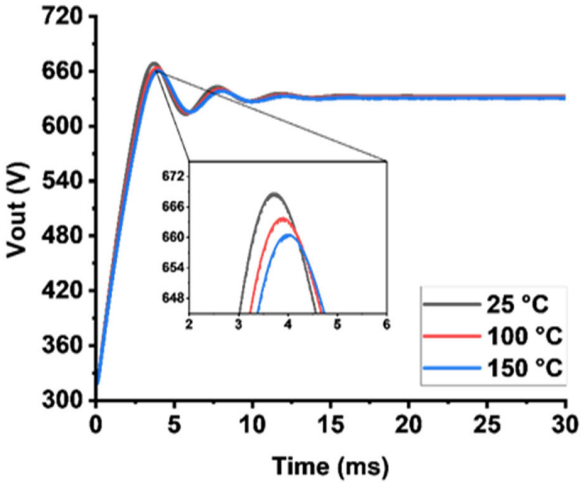

FIGURE 13. Si1 performance in boost converter under different temperature conditions.

Fig. 13 displays the Si-based boost converter's results. There was a deviation between the calculated output voltage of 640 V and the simulated value of 632.76 V at 25 °C. The simulated output voltages at 100 °C and 150 °C were 631.61 V and 630.74 V, respectively. The higher $R_{DS(ON)}$ and switching losses in Si MOSFETs, which are more noticeable at higher temperatures, are the cause of the larger output voltage deviation when compared to the SiC device. The inset graph in Fig. 13 provides further insight into the transient response, showing a more pronounced variation in overshoot and settling behavior across different temperatures. The output voltage at 25 °C is visibly higher than at 100 °C and 150 °C, illustrating the impact of increased RDS(ON) and conduction losses at elevated temperatures.

The settling time is also longer compared to the SiC-based converter, reflecting the inherent thermal instability and higher switching losses of Si MOSFETs. In contrast to the SiC-based converter, the transient behavior of Si1, as shown in Fig. 13, demonstrated a slower stabilization. This illustrates how Si-based devices' inherent higher losses and thermal instability lower their dependability and efficiency in demanding applications. The results demonstrate that SiC-based boost converters outperform Si-based converters in terms of output voltage stability, efficiency, and thermal resilience. Using the theoretical formula for V_{OUT}, the SiC-based converter consistently maintained output voltages close to the calculated values with minimal error, even at high temperatures. These findings support the advantages of SiC technology for high-voltage, high-temperature applications where efficiency and dependability are essential.

IV. CONCLUSION

The simulation results establish the 1.7 kV SiC power MOSFET (SiC) from Table 1 as a superior alternative to silicon-based devices, particularly in high-voltage and high-temperature applications. The positive temperature dependence of the threshold voltage mitigated thermal fluctuations, while $R_{DS(ON)}$ increased from 78 mΩ to 99 mΩ as Tj rose from 25 °C to 150 °C, impacting conduction losses. Double pulse testing confirmed that switching losses increased with higher V_{DS} but SiC MOSFETs maintained peak efficiencies of 99.61% at 150 °C, while Si devices exhibited greater power loss and thermal stress. Thermal stress analysis over 10 switching cycles revealed that SiC experienced a temperature rise of only 0.01033 °C/μs, compared to Si's higher 0.01668 °C/μs, proving better thermal management and power efficiency. The SiC-based boost converter's deviation remains the lowest, contrasting with the Si-based converter, which showed voltage deviations of 632.76 V at 25 °C, 631.61 V at 100 °C, and 630.74 V at 150 °C from the expected 640 V. These findings reinforce SiC technology's suitability for electric vehicles, renewable energy inverters, and industrial power converters, where thermal resilience and power optimization are critical.

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