SILICON DIE CHIPPING IMPROVEMENT THROUGH FULL SANDWICH DOUBLE-SIDED WAFER MOUNTING TECHNIQUE

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DOCTOR OF PHILOSOPHY

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Faculty of Mechanical Technology and Engineering

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A thesis submitted
in fulfillment of the requirements for the degree of
Doctor of Philosophy

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UNIVERSITI TEKNIKAL MALAYSIA MELAKA

2025

DECLARATION

I declare that this thesis entitled "Silicon Die Chipping Improvement Through Full Sandwich Double-Sided Wafer Mounting Technique" is the result of my own research except as cited in the references. The thesis has not been accepted for any degree and is not concurrently submitted in candidature of any other degree.

Signature :..

Name : Mohd Syahrin Amri Bin Mohd Noh

Date : 17 / 10 / 2025

APPROVAL

I hereby declare that I have read this thesis and in my opinion this thesis is sufficient in terms of scope and quality for the award of Doctor of Philosophy.

Signature : ....

Supervisor Name : Prof. Ir. Ts. Dr. Ghazali bin Omar

Date : 17 / 10 / 2025

DEDICATION

"In The Name of Allah, The Most Gracious, The Most Merciful"

This thesis is dedicated to God Almighty, my originator, my source of inspiration, wisdom, knowledge, and comprehension, and my pillar of fortitude. To my wife, Halimah binti Sulaiman, who has been an unwavering source of encouragement and support. I am extremely grateful for your presence in my daily life. To my children, Nurul Fatihah, Muhammad Syahmi, Nurul Faqihah, and Nurul Firzanah, who have been significantly affected by this endeavour. This work is also dedicated to my parent, Mohd Noh Bin Abd Razak and Rohana Binti Chik, who have always loved me unconditionally and whose exemplary behaviour has inspired me to work assiduously towards my goals. I am extremely grateful. There is no way to quantify my love for each of you.

ABSTRACT

This study investigates the development and evaluation of new wafer mounting techniques designed to enhance wafer holding capability, with the primary objective of minimizing chipping and improving the flexural strength of silicon dies by reducing vibration during the wafer dicing process. The conventional single-sided wafer mounting approach was found to be inadequate, particularly in stabilizing non-polished wafers with backgrinding marks, which resulted in insufficient tape adhesion, increased vibration, and compromised mechanical stability during dicing. Chipping was identified as the most critical defect, accounting for 15% of failures within the 23% defect rate related to wafer dicing processes. To address these limitations, double-sided semi-sandwich and full-sandwich wafer mounting configurations were developed and evaluated using UV Tape A, UV Tape B, and non-UV tape. A key focus of the study was the optimisation of UV curing parameters, particularly curing speed, to enable the automatic removal of surface UV mounting tape after dicing, ensuring a seamless transition to subsequent processing steps. Experimental findings showed that UV tape with an adhesive strength of 30 mN/25 mm achieved complete detachment when cured at an optimized speed of 10 mm/s.To assess the impact of this optimization, a comprehensive comparative analysis was performed between the conventional single-sided wafer mounting technique and the proposed double-sided configurations, namely the semi sandwich and full sandwich wafer mounting techniques. Comparative analysis revealed that the full sandwich configuration significantly outperformed the conventional single-sided method, achieving an 84% reduction in topside chipping, a 40% enhancement in die flexural strength, and a 26% reduction in vibration amplitude during dicing. These results validate the double-sided full sandwich wafer mounting technique as a novel and practical solution for improving wafer dicing performance in semiconductor manufacturing applications.

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PENINGKATAN ACUAN SERPIHAN SILIKON MELALUI TEKNIK PELEKATAN WAFER TERAPIT SISI BERKEMBAR PENUH

ABSTRAK

Kajian ini menyiasat pembangunan dan penilaian terhadap teknik pemasangan wafer baharu yang direka bentuk untuk meningkatkan keupayaan pegangan wafer, dengan objektif utama untuk meminimumkan kecacatan serpihan dan meningkatkan kekuatan lenturan acuan silikon melalui pengurangan getaran semasa proses pemotongan wafer. Kaedah pemasangan wafer satu sisi yang konvensional didapati tidak mencukupi, khususnya dalam menstabilkan wafer yang tidak digilap dan mempunyai kesan pencanaian belakang , yang mengakibatkan lekatan pita yang tidak memadai, peningkatan getaran, serta kestabilan mekanikal yang terganggu semasa proses pemotongan. Serpihan dikenal pasti sebagai kecacatan paling kritikal, yang menyumbang sebanyak 15% daripada jumlah kadar kecacatan 23% berkaitan dengan proses pemotongan wafer. Bagi menangani kekangan ini, konfigurasi teknik pelekatan wafer terapit sisi berkembar separuh dan penuh telah dibangunkan dan dinilai menggunakan Pita UV A, Pita UV B, serta pita bukan UV. Tumpuan utama kajian ini adalah pengoptimuman parameter penyinaran UV, terutamanya kelajuan penyinaran, untuk membolehkan penanggalan automatik pita pelekat UV bahagian permukaan selepas pemotongan, bagi memastikan kelancaran peralihan ke langkah pemprosesan seterusnya. Dapatan eksperimen menunjukkan bahawa pita UV dengan kekuatan lekatan 30 mN/25 mm berjaya ditanggalkan sepenuhnya apabila disinar pada kelajuan optimum 10 mm/s. Untuk menilai kesan pengoptimuman ini, satu analisis perbandingan menyeluruh telah dijalankan antara teknik pelekatan wafer satu sisi konvensional dan konfigurasi pelekatan wafer terapit sisi berkembar yang dicadangkan, iaitu teknik separuh dan penuh. Hasil analisis menunjukkan bahawa konfigurasi penuh sandwich menunjukkan prestasi jauh lebih baik berbanding kaedah sebelah tunggal konvensional, dengan pengurangan sebanyak 84% dalam serpihan permukaan atas, peningkatan 40% dalam kekuatan lenturan die, dan pengurangan 26% dalam amplitud getaran semasa proses pemotongan. Keputusan ini mengesahkan bahawa teknik pelekatan wafer terapit sisi penuh merupakan pendekatan baharu yang praktikal dan berkesan dalam meningkatkan prestasi pemotongan wafer dalam aplikasi pembuatan semikonduktor.

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ABS	-	Anti-lock braking systems
AOI	-	Automated optical inspection
BE	-	Back End
BGA	-	Ball Grid Array
CZ	-	Czochralski
DAG	-	Dicing After Grinding
DAF	-	Die Attach Film
DDAF	-	Dicing Die Attach Film
DGB	-	Dicing Before Grinding
EOL	-	End of line
FE	-	Front End
FOL	-	Front of line
FVI	-	Final visual inspection
IC	-	Integrated Circuits
PMC	-	Post Mold Cure
PSA	-	Pressure-sensitive adhesive
RPM	-	Rotation per minute
Sdn Bhd	-	A private limited company
SEM	-	Scanning electron microscope
Si	-	Silicon
SiC	-	Silicon Carbide

UPH	-	Unit Per Hour
UTeM	-	Universiti Teknikal Malaysia Melaka
UV	-	Ultra Violet

LIST OF SYMBOLS

$\sigma_{3\ point}$	-	3-points bending test
α	-	significant test probability
Ra	-	arithmetical mean roughness value

LIST OF PUBLICATIONS

Journal Articles

Mohd Syahrin Amri, Ghazali Omar, Mohd Syafiq Mispan, Fuaida Harun, Zaleha Mustafa, 2024. Semiconductor Chipping Improvement via a Full Sandwich Wafer Mounting Technique. *Majlesi Journal of Electrical Engineering Vol. 18, No. 1, March 2024 Semiconductor*, 10(2), pp. 743-758. (Scopus)

Mohd Syahrin Amri, Ghazali Omar, Mohd Syafiq Mispan, Fuaida Harun, MNB. Othman, and N.A. Ngatiman, 2024, Wafer Dicing Vibration Investigation on Novel Wafer Mounting Techniques, *IEEE Transactions on Semiconductor Manufacturing*. pp. 1312–1319. (WoS)

Mohd Syahrin Amri, Ghazali Omar, Mohd Syafiq Mispan, Fuaida Harun, Abdul Halim Dahalan, 2024, IJIE The Effects of Novel Sandwich Wafer Mounting Technique on Silicon Wafer Chipping Performance, *International Journal of Integrated Engineering*, vol. 16, no. 9, pp. 314–325. (WoS)

AWARDS AND SCHOLARSHIPS

Awards:

2023

1) ON Semi special award – Novel full sandwich wafer mounting technique for chipping and flexural strength improvement, Innovation Showcase 2023, UTeM - 26 October 2023.

2) 3rd prize award – Novel full sandwich wafer mounting technique for chipping and flexural strength improvement, Innovation Showcase 2023, UTeM - 26 October 2023.

2024

1)2nd place in the 3 Minutes Thesis Competition organized School of Graduates Studies UTeM.

2025

1) Appointed as Board of Study (BOS) for the Bachelor of Technology in Industrial Electronics (Semiconductor) with Honours program for Universiti Malaysia Perlis (UniMAP)

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CHAPTER 1

INTRODUCTION

1.1 Background

The demand for integrated circuits (ICs) has been experiencing a significant increasing trend, driven by the rapid expansion of various industries, including consumer electronics, telecommunications, automotive, and artificial intelligence. Silicon wafers play a crucial role in the industry as the primary material for semiconductor device fabrication. Due to their inherent brittleness, silicon wafers are highly susceptible to chipping and cracking during manufacturing, necessitating stringent quality control measures to ensure product reliability and performance.

One of the critical challenges in semiconductor manufacturing is the mechanical stress applied to silicon wafers during processes such as back grinding, wafer mounting, wafer dicing, and wafer handling. Excessive stress can lead to high chipping rates and, more critically, induce cracks in the wafer structure. While a silicon die with microcracks may initially pass electrical testing, these latent defects pose a significant reliability risk when the IC is deployed in real-world applications. Over time, factors such as thermal cycling, mechanical shock, and operational stress may exacerbate these cracks, leading to device failure in customer applications. Such failures can have severe consequences, not only resulting in financial losses for semiconductor manufacturers but also damaging the company's reputation and customer trust.

Silicon wafers are heavily used in the semiconductor manufacturing industry due to their remarkable characteristics and extensive utilization (Lindroos et al., 2010). These wafers function as the fundamental component in the fabrication of integrated circuits (ICs), offering an immaculate surface for the placement and arrangement of semiconductor materials. Silicon is the preferred choice for wafer manufacture due to its abundant presence on Earth (Croissant et al., 2020), ensuring a consistent and reliable supply for this process. Due to their exceptional electrical conductivity, mechanical resilience, and compatibility with microfabrication methodologies, these components are essential in fabricating high-performance integrated circuits. Furthermore, silicon is preferred because of its higher melting point (Control and July, 2016) and it has an additional advantage since it can withstand high temperatures (Zhao et al., 2017) throughout the fabrication process. This property is crucial in the fabrication of integrated circuits, where silicon wafers are subjected to a high-temperature environment.

However, the brittle nature of silicon (Inoue et al., 2020) (Inoue et al., 2017) makes it prone to chipping or cracking (Shen et al., 2019) under mechanical stress or pressure. A major problem in silicon wafer production is that it can potentially reduce die strength (Takyu et al., 2016) and cause yield loss. Chipping is the term used to describe the region removed off the edge of a silicon die (Xue et al., 2018) during the wafer dicing process as seen in Figure 1.1. Since chipping is unavoidable (D. Xue et al., 2021) due to its nature and might cause cracks when stress applied, it was the key concern throughout the wafer dicing process. The use of diamond blades to cut the wafer becomes a huge challenge since the hard diamond with the brittle silicon combination requires lots of work to produce good results.

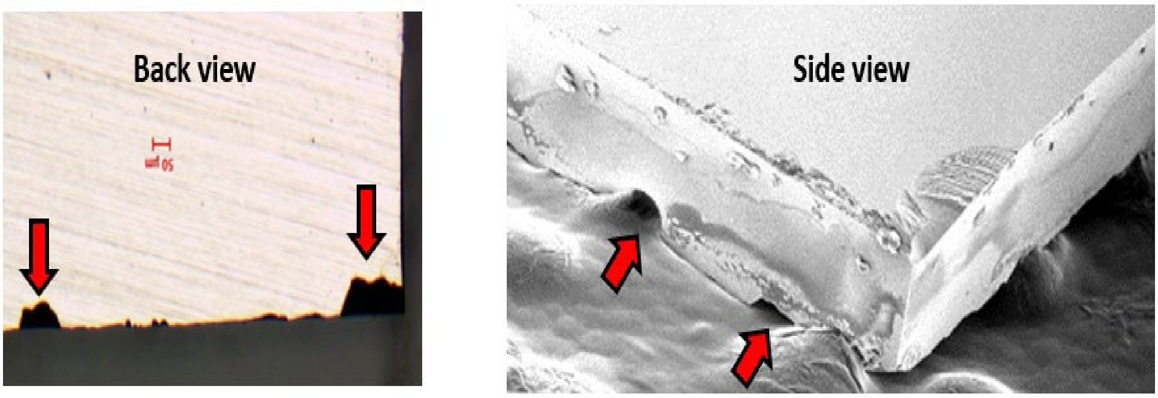


Figure 1.1: Chipping definition

Quality control in silicon wafer production is crucial because any defects or inconsistencies in wafer properties can significantly impact the functionality and yield of semiconductor devices. Defects such as chipping that contribute to cracks can compromise the electrical performance of ICs, leading to device failure or reduced efficiency. Moreover, as semiconductor technology progresses towards smaller node sizes and higher transistor densities, the tolerance for defects has become increasingly stringent. This necessitates enhanced monitoring and control over wafer manufacturing processes, including crystal growth, wafer slicing, back grinding, cleaning, and dicing.

Furthermore, wafer dicing plays a critical role in determining the final die quality in this research. Factors such as dicing blade condition, spindle speed, mounting techniques, and cutting methods must be optimized to minimize chipping and eliminate cracking. Vibrations during wafer dicing, which caused instability during the cutting process, have been raised as a concern by researchers towards achieving higher quality products. This important factor requires further analysis and improvements to minimize the vibration factor especially during the wafer dicing process. It could be seen that the current wafer holding condition during wafer mounting was at the wafer backside only and depends solely on the wafer mounting adhesion gripping performance to adapt the vibration caused during the dicing process.

In modern automobiles, the application of integrated circuits (ICs) has grown significantly, transforming vehicle functionalities and enabling advanced technological integration. A wide range of vehicle systems now rely on integrated circuits (ICs) for regulation and optimisation, including navigation, entertainment, and safety features like airbags and anti-lock braking systems (ABS). They also play a pivotal role in engine management, climate control, and driver assistance technologies, as depicted in Figure 1.2.

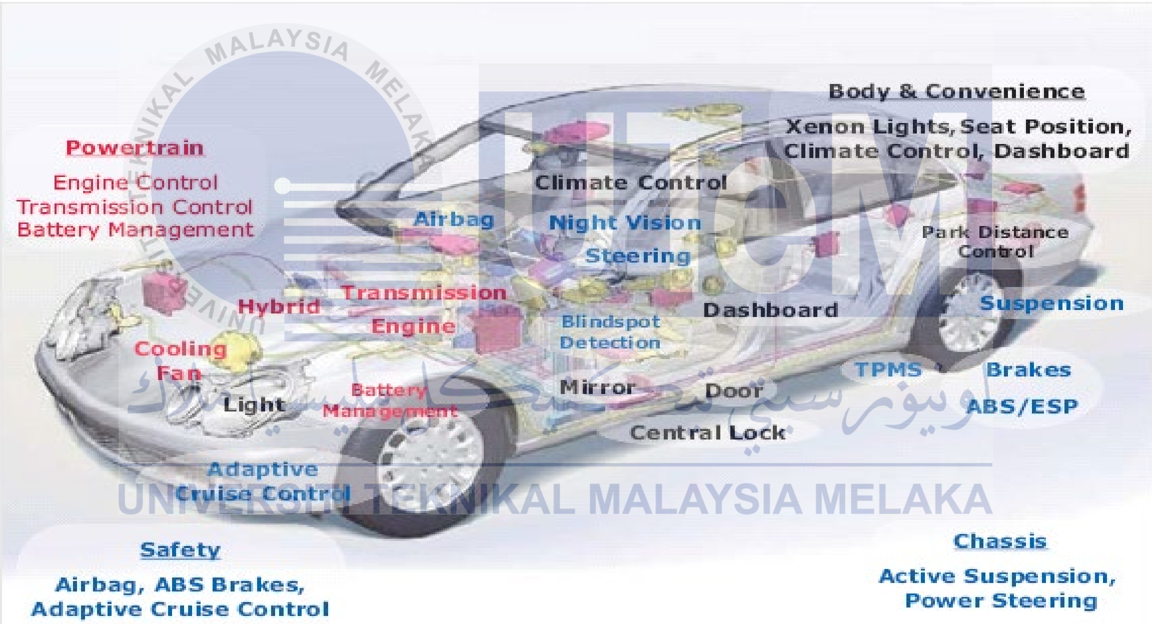


Figure 1.2: IC components in cars today (Source: Infineon Technologies)

These advancements have redefined the automobile interior, providing a seamless and enhanced driving experience while ensuring safety, efficiency, and convenience. For instance, ICs in powertrain systems enable efficient engine control, battery management, and transmission optimization, contributing to reduced emissions and improved fuel economy.

In safety systems, ICs are employed for real-time monitoring and response in airbags, ABS brakes, and adaptive cruise control, ensuring driver and passenger protection. Similarly, ICs in body and convenience systems manage climate control, xenon lights, and dashboard functionalities, offering greater comfort and usability.

Given the critical role ICs play in these essential systems, which are majority using the silicon wafers inside it, their quality and reliability are of paramount importance. Failures in ICs can compromise system performance, leading to safety risks, inefficiencies, or even complete system malfunctions in the consumer's application. Thus, stringent manufacturing standards and rigorous quality control measures are necessary to ensure that automotive ICs meet the industry's high-performance requirements. The increasing dependence on ICs underscores the need for continuous advancements in semiconductor manufacturing. Research and development aimed at enhancing the durability and performance of ICs directly contribute to the overall reliability and longevity of modern automobiles. As automotive technologies evolve, the demand for high-quality ICs will remain central to supporting innovative functionalities and maintaining consumer confidence in vehicle performance.

Wafer dicing represents a critical stage in semiconductor device fabrication; however, it frequently induces chipping and cracking at the die edges. These defects are well-recognized contributors to reliability degradation, as they may propagate during downstream processes or during field operation, ultimately resulting in device failure. During the wafer dicing process, chipping and micro-crack formation are frequently observed along the scribe lines, particularly in brittle materials such as silicon. These defects typically originate at the wafer surface or subsurface due to mechanical stresses imposed by the dicing blade. Over time, the presence of these microstructural imperfections can act as stress concentration points, which, under operational thermal cycling or mechanical loading, may facilitate crack propagation into the active regions of the die (Lee et al., 2024). This crack extension can result in dielectric delamination, metallization layer damage, or even complete fracture of the die, ultimately leading to latent device failure and compromised reliability in the field. The presence of small-scale defects and complex functional failure modes, which are characteristic of thin-film failures, combined with material degradation-induced cracking, presents significant difficulties for accurate failure analysis (Cheng et al., 2023).

The increasing complexity of semiconductor devices, driven by advancements in technology and the demand for higher performance, narrow saw street, smaller sizes, and greater functionality, underscores the critical importance of rigorous quality control in semiconductor manufacturing. Modern semiconductor devices integrate billions of transistors and multiple layers of intricate circuitry on a single chip, making the manufacturing process highly sensitive to variations and defects, which the cracks may propagate from the silicon backside chipping up to the circuitry area. As a result, each step in the process, from wafer fabrication and lithography to chip assembly and packaging, must adhere to stringent quality protocols to ensure the production of reliable and defect-free devices.

Thus, continuous improvement in quality control methodologies, alongside advancements in manufacturing technologies, is vital to meet the stringent demands of modern semiconductor applications. By minimizing defects and ensuring consistent performance, effective quality control safeguards the integrity of semiconductor devices and sustains the competitiveness of manufacturers in an increasingly demanding global market.

At the same time, cost reduction is vital for maintaining profitability in an industry characterized by rapid technological advancements and short product life cycles.

Semiconductor manufacturing involves complex processes with high capital and operational expenditures, such as equipment, materials, and labour. Companies that can streamline production, optimize supply chains, and reduce waste are better positioned to offer competitive pricing while preserving profit margins. Achieving the right balance between quality and cost is crucial for staying competitive in a market where customer demands are constantly evolving, and profit margins are under pressure. Continuous improvement in both areas enables semiconductor companies to innovate while maintaining a strong market presence.

Improvement activities and cost-saving initiatives are crucial in semiconductor manufacturing due to the industry's high operational costs, competitive nature, and rapidly evolving technological landscape. The manufacturing process for semiconductors involves complex procedures, expensive equipment, and advanced materials, all of which contribute to high production costs. By continuously improving production methods and implementing cost-saving strategies, companies can enhance efficiency, reduce waste, and lower overall expenses, which is critical for maintaining profitability in a competitive market. Ultimately, the ability to balance cost-saving measures with quality and innovation is essential for semiconductor manufacturers. By prioritizing improvement activities and cost-efficiency, companies can maintain profitability, meet customer demands, and remain competitive in an increasingly dynamic global market.

In semiconductor manufacturing, the choice of wafer material significantly affects device performance, production cost, and the range of potential applications. Several types of materials are used for wafers, each with unique properties that make them suitable for specific purposes. The primary materials include silicon (Si), gallium arsenide (GaAs), silicon carbide (SiC), and indium phosphide (InP). Silicon wafers are the most commonly used due to their favourable properties and established manufacturing processes. Table 1.1 displays an overview of each material, along with its advantages and disadvantages.

Table 1.1: Available wafer material in semiconductor manufacturing including the advantages and disadvantages

Wafer's material	Advantages	Disadvantages
1) Silicon (Si) Silicon is the most prevalent material used in wafer manufacturing. It is preferred due to its semiconductor properties, cost-effectiveness, and natural abundance.	• 50% lower production cost (Mierlo et al., 2017) and abundant supply (Ballif et al., 2022)(Rojas et al., 2014). • Mature and well-established manufacturing processes (M. Garfn et al., 2023). • Excellent mechanical strength and stability (Kozlov et al., 2023). • Compatible with a wide range of electronic applications (Soref et al., 2023).	• Brittle material and easily crack (Yin et al., 2018)(Yin, Bai and Zhang, 2019)(Budiman et al., 2021). • Lower electron mobility compared to some compound semiconductors (Geum et al., 2016), limiting its use in high-speed and high-frequency applications.

2) Gallium Arsenide (GaAs) Gallium arsenide is commonly used in high-speed devices and optoelectronic applications like LEDs and laser diodes.	• Higher electron mobility than silicon (Boland et al., 2017), making it suitable for high-speed and high-frequency devices. • Direct bandgap allows for efficient light emission, which is ideal for optoelectronic applications (GaAs and Nanowires, 2020).	• More expensive to produce than silicon (Lee at al. 2020)(Duan and Liu, 2022). • More brittle, making it more challenging to handle during manufacturing (Duan and Liu, 2022). • Toxicity concerns associated with arsenic content (Liu et al., 2024)(Blanco et al., 2024).
3) Silicon Carbide (SiC) Silicon carbide is utilized in power electronics and applications with high thermal conductivity and voltage resistance.	• High thermal conductivity, making it suitable for high-power applications (Cheng et al., 2022). • Capable of operating at higher voltages and temperatures compared to silicon (She et al., 2017).	• Higher production costs due to complex manufacturing processes (Blevins, 2020)(Veliadis, 2022).

	• Suitable for harsh environments (Baruah et al., 2021), such as electric vehicles and industrial power systems (Giovanni et al., 2023).	
4) Indium Phosphide (InP) Indium phosphide is used mainly in high-speed telecommunications and optoelectronics.	• High electron mobility, suitable for high-speed applications (Xu et al., 2024). • Ideal for fibre-optic communication due to its efficient light emission (Shi et al., 2024).	• Very expensive to produce, limiting widespread use (Clarke et al., 2023). • More fragile and difficult to handle compared to silicon (Siwak et al., 2015).

From the comparison above, silicon wafers have the lowest production cost among other materials however, the primary concern with the material was levels of chipping and cracking after the dicing process, which has a negative impact on the die strength. These defects, which are often introduced during the wafer dicing stage, serve as stress concentration points that significantly weaken the structural integrity of the die. Larger chips or cracks can amplify localized stresses under mechanical loads, making the die more susceptible to fractures during subsequent manufacturing steps or end-use applications. The presence of such defects poses serious risks to the reliability and durability of semiconductor devices.

Furthermore, the selection of wafers with grinding marks at the backside area produced extra challenges in this research. The wafer back grinding process is a critical step in semiconductor manufacturing, primarily used to reduce wafer thickness according to the device thickness requirement. However, this process leaves behind grinding marks on the wafer's backside as per Figure 1.3, which can influence the overall mechanical integrity of the wafer. The orientation and depth of these grinding marks may contribute to stress concentration points, making the wafer more susceptible to defects such as chipping and cracking during subsequent processing steps.

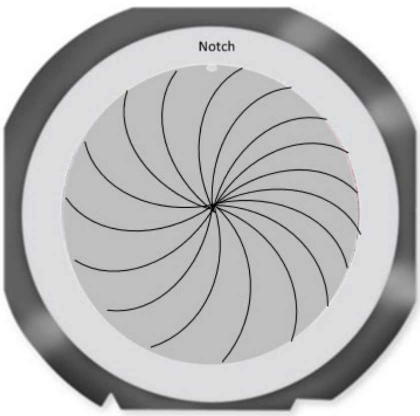


Figure 1.3: Grinding marks at wafer backside

One of the major challenges associated with wafer grinding is surface unlevelness, which can significantly impact dicing performance. Uneven surfaces lead to inconsistent contact between the dicing blade and the wafer, causing variations in cutting force and increasing vibration. These vibrations exacerbate chipping defects, reducing die yield and reliability. Optimizing the back grinding process to achieve a uniform surface finish is crucial to minimize chipping and ensure high-quality semiconductor devices with improved mechanical robustness. Addressing these challenges requires implementing wafer mounting techniques, fixing the dicing parameters, and generating vibration absorption techniques to minimize defects and ensure the production of reliable and high-strength semiconductor dies.

1.2 Problem Statement

The conventional wafer dicing process was based on single-sided wafer mounting application. The current technique had insufficient wafer gripping, especially on the surface area, which caused vibration during the dicing once the diamond blade touched the silicon wafer for the singulation process. The current single-sided wafer mounting process is not able to fully absorb the stress generated during the wafer dicing process, resulting in high chipping occurrence. As described earlier, the silicon wafers are brittle and inclined to chip at the edges during the dicing process, especially when using mechanical methods like diamond blades, which are expected to produce excessive chipping and could generate a crack die issue. High chipping during wafer dicing is a major concern for semiconductor manufacturing industries as it directly impacts semiconductor devices' quality, yield, and reliability (Perminov et al., 2018).

According to Y. M. Hsieh (2020) and Yongbing Wu (2021), chipping can produce cracks (Takyu et al., 2016) and IC functional failures (Hsieh et al., 2020), leading to a decrease in overall yield and potentially compromising the structural integrity and performance of the final products. This leads to higher production costs due to increased scrap and high rework rates, especially for visual inspection. There are a few detection methods for chipping, which consist of normal manual visual inspection, automated optical inspection, and a recent advanced method using AI and deep learning. Traditionally, the identification of defects such as chipping has relied on visual inspection, often supported by high-magnification instrumentation such as high-power scopes and scanning electron microscopy (SEM). However, this method is inherently labour-intensive, susceptible to human error, and influenced by operator fatigue, which may result in inconsistent assessments, misclassification of defects, and increased personnel-related costs.

To overcome the limitations of chipping manual inspection, automated image analysis and optical detection systems have been developed for the evaluation of wafer chipping, including the characterization of chip size and morphology. These systems employ advanced image processing algorithms to enable objective, consistent, and repeatable assessments, thereby significantly minimizing the risk of human error and improving overall inspection reliability. While recent advancements have integrated artificial intelligence (AI) technologies, including neural networks and deep learning architectures, to enhance the classification and detection of wafer defects with high accuracy and processing speed (Friedrich, Schlosser and Kowerko, 2024). These AI-driven systems are capable of analyzing images in real time, often achieving processing times of less than one second per die. When trained on a combination of real and synthetically generated defect datasets, these models demonstrate substantial improvements in detection performance, thereby contributing to more reliable and efficient quality control in semiconductor manufacturing.

At STMicroelectronics, A. Sumagpang Jr. et al. (2020) reported that chipping constituted the most significant defect contributor within the wafer dicing process, as illustrated in Figure 1.4. Chipping is regarded as a critical defect in semiconductor manufacturing due to its high occurrence and impact on die quality and yield. The study indicated that chipping accounted for approximately 23% of all wafer dicing defects, with a reported failure rate of 15%, underscoring its prominence as a key reliability concern during the dicing stage.

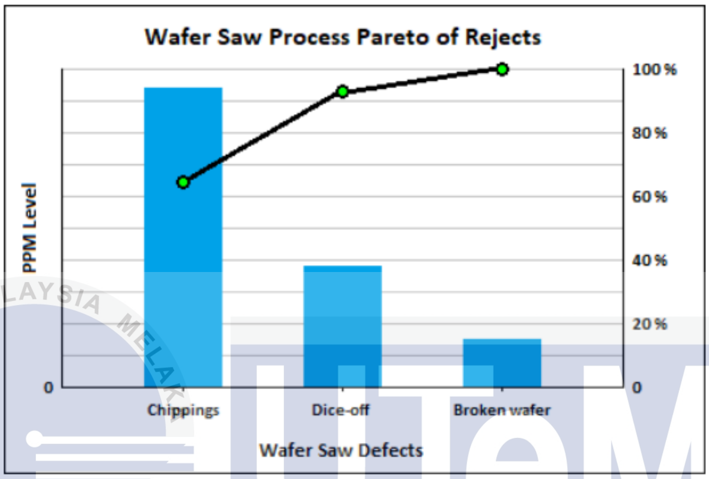


Figure 1.4: Pareto diagram of wafer dicing defects (Sumagpang Jr. et al., 2020)

While using AI inspection, it was found that chipping ≥ 30 µm width is considered a big defect, which has a 0.2% rate (Ackerl et al., 2023). As the assessment of chipping in these activities was based on the total chipping area rather than the chipping width, it is critical to examine the extent of excessive chipping area, which has been identified as a contributing factor to crack initiation and propagation. Understanding this relationship is essential for accurately evaluating the severity of chipping-related defects and their impact on wafer integrity. The appearance of chipping with 90-degree angles produced at the die edges is claimed to have a lateral crack issue, as demonstrated in Figure 1.5. The chipping area was then measured using

ImageJ, which identified a chipping area of 1005 μm^2. The measurement area is one of the early indicators of a potential crack to happen as a reference.

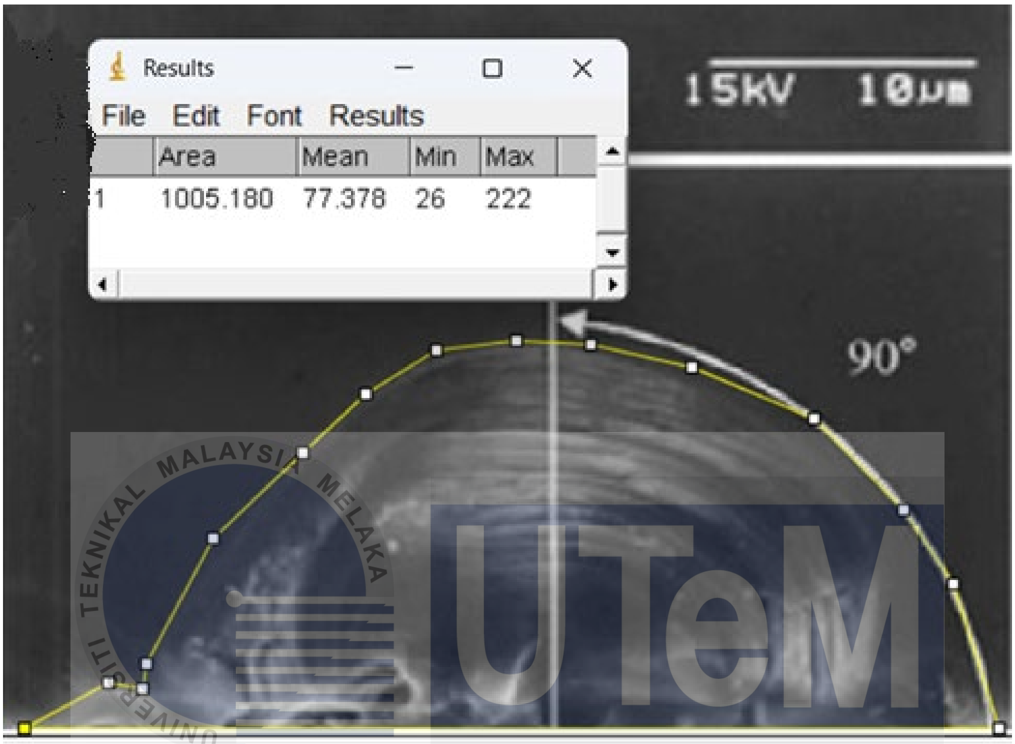


Figure 1.5: 90-degree chipping area (Luo and Wang, 2008)

Chipping was also reported to have a substantial impact on the flexural strength of silicon dies. The higher the chipping, the flexural strength of the silicon die will be reduced (Jiun et al., 2004), and this may affect the overall device quality performance. According to Jefferson Talledo, the majority of research on die strength characterisation predominantly focuses on evaluating the effects of surface damage caused by different manufacturing techniques. The operations encompass back grinding, polishing, wafer mounting and singulation, which can substantially compromise the mechanical integrity of silicon dies by introducing surface defects, micro-cracks, or residual stresses that diminish overall strength.

It was observed that the conventional single-sided wafer mounting technique led to the highest chipping performance during the dicing process, thereby reducing the flexural strength of the silicon die material with the reading of 253 Mpa with a larger chipping behaviour which is consistent with the findings of Shinya Takyu (Takyu et al., 2007) and Oscar Borrero-Lopez (Borrero-López et al., 2009), who also reported a direct proportion with higher levels of chipping or cracking after the wafer dicing process.

Dicing on unpolished wafers with bumpy grinding marks presents several challenges, primarily related to reduced wafer gripping and increased vibration during the dicing process. The uneven surface caused by grinding marks lowers the adhesive tape's ability to securely grip the wafer, resulting in insufficient stability. This lack of stability allows the wafer to vibrate under the mechanical stresses of the dicing blade during the cutting process. When vibrations occur, the dicing blade is subjected to fluctuating forces, leading to uneven cuts and increased edge chipping. Bumpy grinding marks amplify this effect, as the irregular surface creates areas of inconsistent contact between the wafer and the mounting tape, further contributing to instability. The result is reported with a higher incidence of top-side and backside chipping, which compromises the structural integrity of the die and its mechanical properties.

The vibration was initiated because the mounting tape adhesion was insufficient to hold the sawn die during the dicing process, causing the instability during the singulation process. The instability produced higher chipping performance and tends to generate a crack as well. The vibration begins to occur when the blade cuts the wafer from the topside moving to the backside area, whereas wafer gripping performance is dependent solely on the backside of the wafer and is not able to sustain vibration from the surface region. The wafer mounting process needs to provide sufficient wafer holding power (Bandl et al., 2020) so that the wafer can be held firmly so that during dicing, it can produce good dicing quality. Furthermore, unpolished wafers tend to exhibit grinding marks, which has been a major concern when it comes to wafer dicing. When grinding markings were present, the surface became uneven (Wang et al., 2020), and the adhesion of mounting tape became poorer (Chang and Ler, 2022)(Chen et al., 2006). This increased vibration during the wafer dicing and generated higher chipping and potential crack issues as well. It was observed that conventional single-sided mounting has been the method for most wafer mounting procedures in the current semiconductor industries for decades, and researchers are still working to solve the crack issues, and this project aims to minimize the vibration and improve the chipping performance.

The conventional single-cut dicing process has been observed to produce additional stress and introduce potential cracks during the singulation process due to the alternating compression and tensile stresses exerted by the diamond particles on the material. This phenomenon occurs because brittle materials, such as silicon, have threshold load limits that dictate the effectiveness of the cutting process. When the applied force exceeds this threshold, the material is unable to absorb the mechanical stress uniformly, leading to crack propagation and structural defects. (Jiun et al., 2004) highlighted that attempting to dice thick brittle materials in a single pass increases the likelihood of damage, as the cutting force is concentrated in one go, rather than being distributed across multiple controlled passes.

Optimizing dicing parameters, including blade speed, rotational speed, cutting method, and depth of cut, were the previous efforts for minimizing crack formation and achieving optimal chipping performance. Extensive experimentation is required to determine the ideal conditions, necessitating a high number of process runs due to the multiple variables involved. However, the supply of mirror silicon wafers from industry is often limited, posing a challenge for large-scale evaluations. In this context, wafer mounting appears as the most cost-effective approach for assessing chipping performance, particularly in wafers with backgrinding marks.

Since the single-sided wafer mounting does not consistently provide good chipping results, it is best to evaluate the new method of wafer mounting by using the double-sided wafer mounting technique.

1.3 The Objectives of This Thesis

The main objectives of this thesis are as follows:

i. To develop double-sided semi and full-sandwich wafer mounting techniques for topside and backside chipping improvement on non-polish backside silicon wafers.

ii. To determine the flexural strength using a 3-point bending test toward each wafer mounting technique

iii. To analyze the chipping and flexural strength of each mounting technique with vibration analysis

1.4 Scope of Work

The scopes of the research are limited to the below areas of study.

i. Silicon non-circuitry or mirror wafers with 300 µm wafer thickness

- Silicon non-circuitry wafers were used because the industry has its own policy not to share any confidential components or documents with the public. However, the mirror wafers supplied by them can be used to represent the industry material usage since the materials can be used to benchmark the chipping performance.

ii. Non-backside polish and dicing after grind (DAG) wafers process

- Non-backside polished wafers developed grinding marks on the wafer back. These grinding marks developed the worst case chipping conditions for the team to solve the chipping issues. The dicing after grinding (DAG) was the basic dicing feature and used in the current manufacturing line for these improvement activities.

iii. **Process optimization only on the wafer mounting process**

- Wafer mounting process was selected for improvement activities because at this moment, not much improvement was performed towards this process whreby it is an opportunity to evaluate the wafer mounting double-sided wafer mounting techniques.

iv. **Ultra Violet (UV) and Non UV mounting tape only**

- These two types of mounting tapes are the common mounting tapes used in the semiconductor manufacturing line and can be easily provided by the supplier.

v. **Single cut sawing method with fixed dicing parameter and die size of 6 x 6 mm**

- Single cut is the most common cutting method used in the manufacturing line. It provides the highest UPH and the lowest cost towards the operation. However, it has the highest chipping challenge to provide a balanced minimum towards top and backside chipping performance. While 6 x 6 mm is the common die size used in production line.

vi. **Topside and Backside chipping inspection area only.**

- Topside and backside chipping are the common inspection criteria in the production line.

vii. **3-point bending test method for die strength test**

- This is the common method used to check the flexural strength performance. 3- point bending test was selected because the suitable criteria for these activities and machine availability as well.

viii. Vibration analysis

- The new approach to analyze vibration using a piezoelectric film sensor. This is to identify which moutning technique produce the highest and lowest vibration performance.

ix. Do not cover latent failure or any reliability failure

- Chipping or crack assessment is typically conducted based on the immediate post- process inspection, rather than through extended or long-term monitoring. Reliability failure will not be covered in the activities.

1.5 Hypothesis/Research Questions

a. Hypothesis

i. Conventional single-sided wafer mounting technique is not able to hold the wafer firmly when high blade rotation is applied during the cutting process. Additional mounting tape on the wafer surface or a double-sided mounting tape approach will grip the wafer firmly and provide an additional cushioning effect during cutting which minimizes the chipping performance.

ii. The chipping performance results should reflect the flexural strength performance. The double-sided semi and full sandwich wafer mounting technique is expected to produce lower chipping and higher flexural strength compared to the conventional. The die strength using double-sided wafer mounting techniques is expected to be significantly higher compared to the conventional wafer mounting technique.

iii. The lower chipping performance and higher flexural strength from double-sided semi and full sandwich wafer mounting should have lower vibration performance due to the additional surface wafer mounting which holds the wafer firmly resulting in higher stability during dicing and minimizes the wafer vibration during dicing.

b. Research Question

i. Which wafer mounting technique will give the best chipping and flexural strength results?

ii. How the surface mounting tape will be removed after the wafer dicing process?

iii. Will the double-sided mounting technique hold the wafer more firmly compared to the conventional single-sided mounting technique and provide lower vibration performance?

1.6 Thesis outline

This thesis is organized into five (5) chapters under the previously stated goals and approach. Thus, the description of each chapter is supplied as follows:

Chapter 1. Introduction: This chapter provides an overview of the study's background, research challenges, aims, scopes, and research contributions.

Chapter 2. Literature review: This chapter starts with a process flow of semiconductor manufacturing and the chipping challenges in the current process for silicon wafers. This chapter covers the existing method, materials, and the problems encountered by other researchers as well. The research gaps and the novelty were identified and ideas for improvement were discussed as well.

Chapter 3. Methodology: This chapter presents the methodology developed to test the semi and full sandwich wafer mounting techniques, including various wafer mounting tape sample preparation and 3-point bending test characterization. The vibration analysis was included on the dicing machine to understand each wafer mounting technique performance and the types of machines involved including the materials used were shared in this chapter as well.

Chapter 4. Results and discussion. This chapter presents the results of semi and full-sandwich double-sided wafer mounting compared to the conventional wafer mounting technique. Chipping and crack performance, die flexural strength, and vibration analysis were compared and analyzed in this chapter,

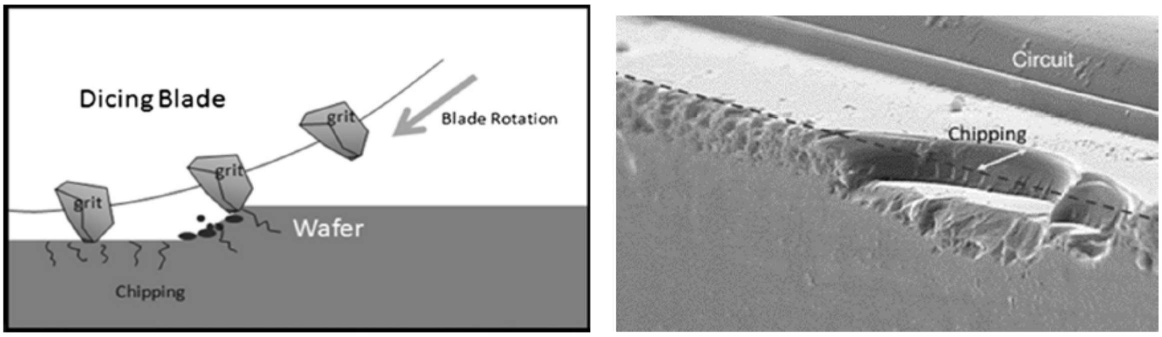
Chapter 5. Conclusion and future works: This chapter summarises the findings and accomplishments of this research. Last but not least, this chapter discusses potential industry uses and offers suggestions for future study and enhancements.

CHAPTER 2

LITERATURE REVIEW

2.1 Overview

This chapter provides a comprehensive review of the existing methodologies documented in the literature aimed at mitigating chipping and eliminating crack die failures in semiconductor manufacturing. Chipping in the wafer dicing process refers to the formation of small fractures or breakouts along the cut edges of a silicon wafer during separation into individual dies as shown in Figure 2.1. The formation of chipping initiates when the rigid and abrasive diamond blade makes contact with the brittle silicon wafer during the dicing process. This interaction induces localized mechanical stresses that exceed the critical fracture threshold of the wafer material, resulting in the generation of microcracks and subsequent chipping along the cut edges.



(a) (b)

Figure 2.1: Chipping formation (a) diamond blade contact with wafer (b) after the wafer dicing process (T.-J. Su et al., 2018)

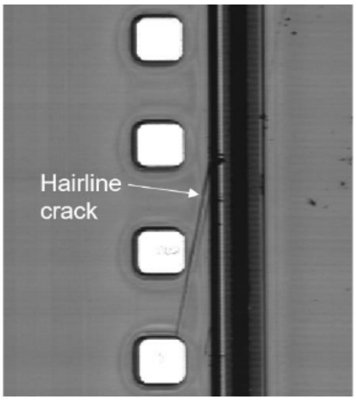
Chipping typically occurs due to several factors such as mechanical stress, vibration, or improper dicing parameters, leading to reduced die strength and potential functional failures. Minimizing chipping is critical to ensuring high-quality semiconductor devices with improved reliability and performance. Excessive chipping may expand and cause cracks which becomes a critical concern in semiconductor manufacturing due to its direct impact on product reliability, yield, and overall manufacturing efficiency. This section presents the process flow of semiconductor pre-assembly areas (backgrinding, wafer mounting and wafer dicing), emphasizing the high susceptibility to chipping and cracking. Furthermore, the review critically examines the significance and limitations of conventional approaches, particularly the single-sided wafer mounting technique, and explores potential improvements. The review is based on an analysis of both recent and past journal articles, as well as reference books.

2.2 High concern on excessive chipping causes crack die in semiconductor manufacturing

Front-end wafer fabrication represents the initial stage of semiconductor manufacturing, during which integrated circuits (ICs) are formed on silicon wafers. Silicon is inherently a brittle material, rendering it highly vulnerable to mechanical damage during the singulation process. Due to its low fracture toughness, the material is prone to crack initiation and propagation when subjected to mechanical stresses, particularly during dicing operations. As a result, chipping becomes an inherent and frequently observed phenomenon in silicon wafer singulation. While complete elimination of chipping is not feasible owing to the material's mechanical limitations, its occurrence can be minimized through the optimization (Zhang et al., 2021) of process parameters, the implementation of protective wafer handling techniques, and the adoption of advanced singulation methods. The inherent brittleness of silicon wafers poses a significant challenge in controlling chipping throughout semiconductor manufacturing. Despite its high hardness, silicon remains fragile and prone to mechanical stress, particularly during pre-assembly processes such as backgrinding, wafer mounting, and wafer dicing. Chipping occurs when excessive force or vibration is applied, leading to small fractures or material loss at the wafer's edges or surface. These defects can compromise die strength, reduce yield, and ultimately impact the reliability of semiconductor devices.

Chipping during the wafer dicing process can occur on both the topside and backside of the wafer, posing a critical challenge in semiconductor manufacturing. Han (2020) emphasizes that excessive chipping from the topside is particularly concerning, as it can generate cracks that extend into the silicon substrate, potentially compromising the integrity of the device. These cracks may further propagate under mechanical or thermal stress during subsequent processing steps, potentially leading to latent failures. Moreover, severe topside chipping can directly impact the active circuit area, rendering the affected dies non-functional, as illustrated in Figure 2.2. Proper dicing techniques, optimized process parameters, and advanced mounting methods are essential to minimize chipping and ensure wafer quality.

(a)

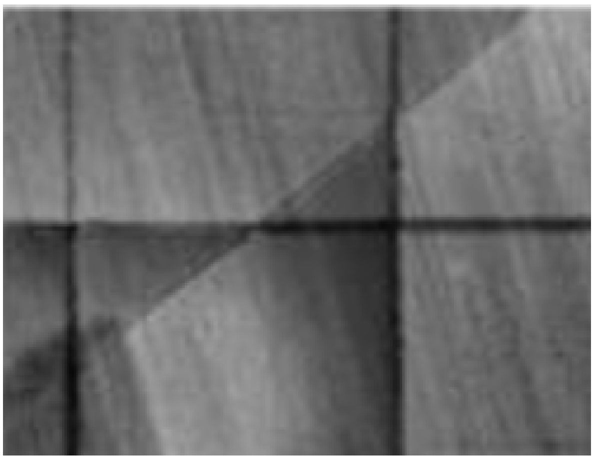


(b)

Figure 2.2: Topside chipping (a) side view (b) top view causing hairline crack (Han, 2020)

Backside chipping during the wafer dicing process can contribute to crack formation, primarily resulting from inadequate wafer stabilization by the mounting tape. This issue arises when the adhesion strength of the mounting tape is insufficient, leading to wafer instability during dicing and increasing mechanical stress on the wafer's backside. Furthermore, maintaining wafer levelness is critical in ensuring uniform contact with the mounting tape, thereby reducing the risk of chipping. The selection of a mounting tape with optimal adhesion properties, in conjunction with well-optimized dicing parameters, is essential for minimizing backside chipping. Implementing these process enhancements effectively mitigates crack propagation, thereby improving overall wafer quality and reliability. Figure 2.3 illustrates an example of backside chipping leading to crack-induced die failures during the wafer dicing process.

(a)



(b)

Figure 2.3: Backside chipping (a) side view (b) top view causing hairline crack (Han, 2020)

Cracks represent a critical challenge in semiconductor manufacturing, as they often remain undetected during standard assembly sampling and have a high propensity to propagate under various stress conditions encountered throughout the fabrication process. Hairline cracks, in particular, are characterized by their microscopic size and low contrast, making them difficult to identify using conventional inspection techniques. The most severe consequence arises when such failures occur in customer applications, which can not only damage the company's reputation but also lead to financial liabilities, including compensation claims. These repercussions ultimately contribute to increased production costs and operational risks, underscoring the necessity for robust crack detection and prevention strategies in semiconductor manufacturing.

For more than a decade, researchers have extensively examined the phenomenon of crack formation in semiconductor dies, as it remains a persistent and critical challenge within the industry. Despite numerous studies and advancements in wafer processing, dicing techniques, and material improvements, the complete elimination of die cracks has not yet been achieved. The inherent brittleness of silicon, coupled with the complex mechanical and thermal stresses encountered throughout semiconductor manufacturing, continues to facilitate crack propagation. Several key factors, including wafer thinning, back grinding, dicing, and packaging, contribute to the accumulation of internal stresses within the semiconductor die, further exacerbating the risk of crack formation.

These stresses can significantly reduce the overall mechanical strength of the die, making it more susceptible to chipping and crack formation. Consequently, the weakened structural integrity of the die facilitates crack initiation and propagation, posing a considerable challenge in ensuring product reliability. Understanding the influence of these process-induced stresses is essential for optimizing manufacturing parameters and mitigating the risk of mechanical failures in semiconductor devices. Although significant progress has been made in optimizing wafer mounting techniques, improving dicing blade materials, and refining process parameters, these measures have only been able to mitigate crack formation rather than fully eliminate it. Cracks that are undetectable during initial testing may worsen over time, leading to latent failures in the final product. This poses a major reliability risk in semiconductor devices, particularly in high-performance and safety-critical applications. Therefore, ongoing research is necessary to develop more robust solutions, such as advanced wafer handling techniques and innovative stress-relief methods, to further minimize the occurrence of crack die and enhance semiconductor manufacturing yield and reliability.

2.3 Process flow of IC manufacturing and potential stress area

Take note that the silicon wafer itself has its intrinsic and extrinsic pressure during manufacturing based on its manufacturing process flow. Figure 2.4 illustrates the fundamental semiconductor manufacturing process, outlining the key stages involved in the fabrication of an Integrated Circuit (IC). This process encompasses multiple critical steps, from wafer fabrication to the final testing process. However, for the scope of this study, the discussion will be focused specifically on the pre-assembly process. This stage is crucial as it involves wafer back grinding, wafer mounting and die singulation, all of which significantly influence the chipping behaviour and the reliability of the final IC.

A comprehensive analysis of the pre-assembly process will provide insights into defect prevention strategies and process optimization in semiconductor manufacturing. The next chapter will discuss the factors of each pre-assembly process (highlighted in red box) to understand the types of stress involved and what previous activities were performed to minimize stress occurrence and chipping performance as well.

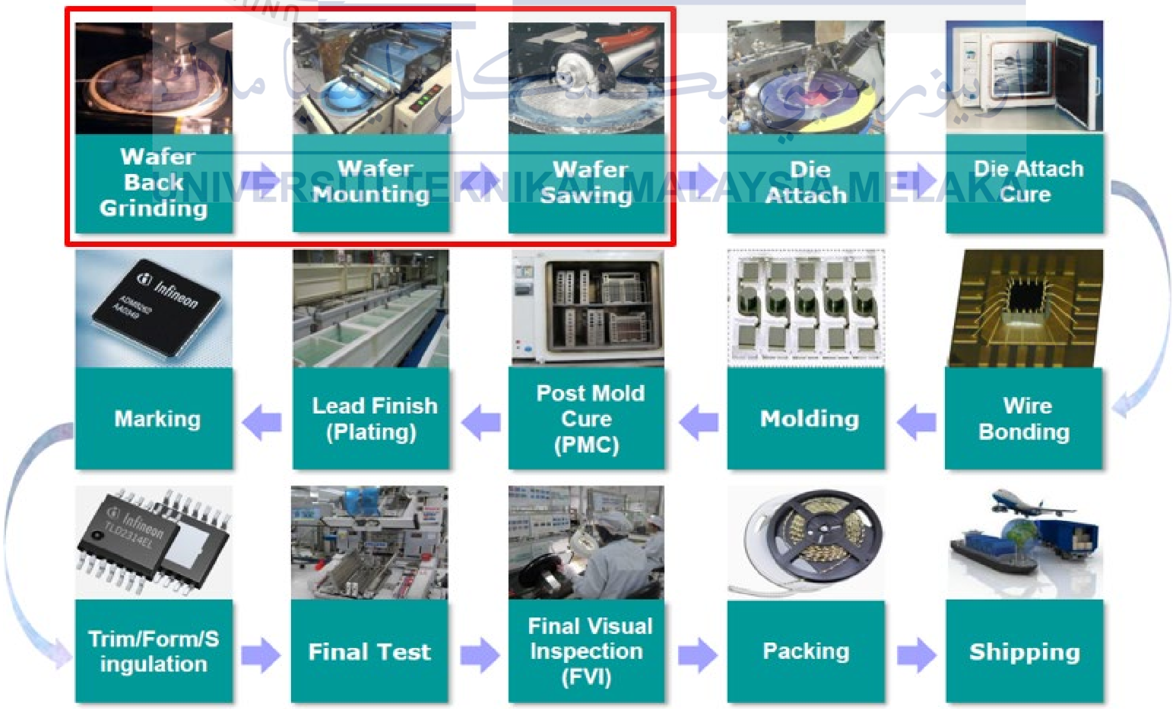


Figure 2.4: Assembly IC manufacturing process flow (Source: Infineon)

2.3.1 Wafer Backgrinding

The semiconductor backgrinding process is a critical step in the manufacturing of semiconductor devices, aimed at reducing the thickness of silicon wafers to meet the demands for miniaturization following the IC packaging requirements. This process involves grinding the backside of the wafer to achieve the desired thickness as illustrated in Figure 2.5, which is essential for the production of thinner and more efficient electronic packages (B. C. S. Bacquian and Gomez, 2020). However, the mechanical forces applied during back grinding introduce significant stresses within the wafer, which can lead to defects such as chipping, cracking, and warpages. These mechanical stresses are categorized as intrinsic and extrinsic stresses. Intrinsic stress originates from the wafer's internal structure, while extrinsic stress arises from external mechanical forces during processing.

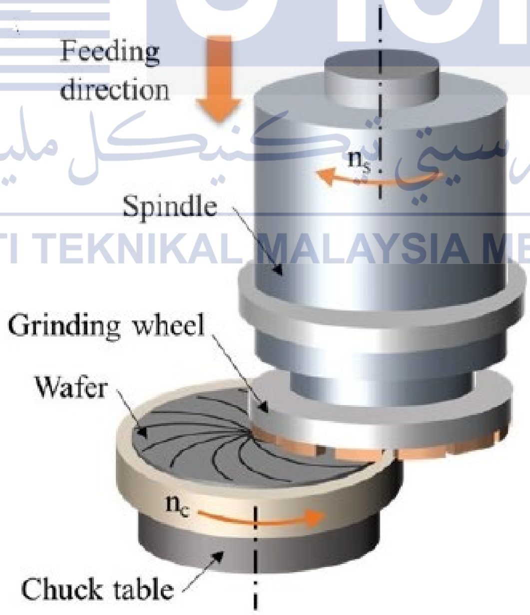


Figure 2.5: Illustration of wafer backgrinding process (Y. Liu et al., 2022)

As the wafer gets thinner during the grinding process, its susceptibility to mechanical stress and vibrations significantly rises, thereby exacerbating the risk of backside chipping and crack formation(Bryan Christian S Bacquian, 2020). Thinner wafers also exhibit greater warpage and structural fragility, making them more prone to breakage, which can ultimately lead to increased production costs. However, the determination of wafer thickness is primarily dictated by the specific device application and customer requirements, necessitating a balance between manufacturability and functional performance.

In the semiconductor industry, three primary backgrinding processes are commonly utilized, each exhibiting distinct stress characteristics that can be systematically analyzed and quantified.

2.3.1.1 Coarse grinding

The basic method for the back grinding process is coarse grinding, which is designed for rapid material removal. This method utilizes a grinding wheel with large abrasive particles, allowing for high-speed thinning of the wafer. For this reason, a coarse-grit grinding wheel is used, which results in a rough surface roughness. The grinding wheel utilized grit sizes ranging from 120 to 600 to allow faster removal of the silicon wafer backside. Coarse grinding is a fundamental stage in semiconductor wafer processing that comes before fine grinding and polishing. In order to attain the proper thickness and flatness, large amounts of material are removed from the backside of silicon wafers. However, due to the aggressive nature of the process, coarse grinding typically leaves behind deep grinding marks and introduces significant residual stress (Du et al., 2021)(Kohls et al., 2021). These grinding marks, if not properly managed, can act as crack initiation sites (Tao et al., 2023), leading to chipping and potential die failure in later processing stages.

Coarse grinding is an efficient technique for removing material from silicon wafers, it frequently results in prominent backside grinding marks. These backside grinding marks represent a critical challenge for semiconductor manufacturers as they create surface irregularities that act as stress concentration points during the wafer dicing process. Such conditions lead to the potential of higher chipping during dicing due to unlevel backside surface, which causes instability during dicing in addition to significantly impacting both the yield and performance of the resulting semiconductor devices. High chipping rates compromise the structural integrity of the dies, increasing the likelihood of mechanical failures such as cracks during subsequent manufacturing steps or in final applications.

Although coarse grinding results in the formation of backgrinding marks, it remains a favourable approach due to its high material removal rate, which enhances overall productivity and significantly reduces the grinding time. Furthermore, coarse grinding facilitates efficient wafer thinning, thereby improving throughput in semiconductor manufacturing and increasing the units per hour (UPH). To mitigate the impact of backgrinding marks generated during the coarse grinding process, an optimized wafer mounting technique is required. This involves the selection of an adhesive tape with optimal cushioning properties to ensure uniform support, minimize mechanical stress, and enhance wafer stability during the subsequent dicing process.

2.3.1.2 Fine grinding

To enhance the wafer backside condition and mitigate the residual stress induced by the coarse grinding process, a secondary method, fine grinding, is introduced as a subsequent refinement step. This process follows coarse grinding to improve surface quality by employing finer abrasive materials and optimized grinding parameters. Fine grinding effectively reduces the depth of grinding marks, minimizes surface roughness, and refines the wafer's overall texture. It plays a crucial role in alleviating the adverse effects of coarse grinding by eliminating deep scratches that could otherwise lead to mechanical failures. However, despite these improvements, some residual grinding marks may persist, necessitating additional stress-relief measures. The use of a finer grit grinding wheel during fine grinding facilitates precise material removal, ensuring a delicate and controlled thinning of the wafer backside. As an essential stage in the wafer backgrinding process, fine grinding focuses on achieving the target wafer thickness while simultaneously eliminating surface imperfections. Typically, the grinding wheel utilized in this process features fine-grit abrasives with grit sizes ranging from 600 to 2000, ensuring superior surface smoothness and enhanced wafer integrity

Fine grinding is performed to achieve a smoother surface finish (Koeninger et al., 2018) and to reduce the stress introduced during the coarse grinding process. In this stage, a finer grit grinding wheel is used to gently remove a smaller amount of material, ensuring a much smoother and more polished surface. Fine grinding also helps to remove any micro-cracks (Wang et al., 2017) and improve the overall strength of the wafer (Bie et al., 2016). Together, coarse and fine grinding ensures that the wafer meets the required thickness while maintaining its structural integrity, making it suitable for further processing in semiconductor manufacturing.

Fine grinding offers a superior alternative to coarse grinding by producing a smoother backside surface with fewer grinding marks and defects. This process reduces the risk of stress concentration points that can lead to chipping and cracking during the wafer dicing process. The smoother surface achieved through fine grinding contributes to improved wafer stability, enhanced die strength, and better overall yield in semiconductor manufacturing. Additionally, the reduced chipping rate results in higher-quality semiconductor devices, making fine grinding a preferred choice for critical applications requiring reliability and precision.

Fine grinding presents a superior option to coarse grinding by yielding a smoother backside surface with reduced grinding marks and imperfections. This procedure mitigates the risk of stress concentration points that may result in chipping and cracking during the wafer dicing process. The refined surface obtained from fine grinding enhances wafer stability, increases die strength and improves overall yield in semiconductor manufacturing. However, fine grinding has its drawbacks, particularly in terms of cost and process complexity. The equipment required for fine grinding is more advanced and precise, leading to higher capital and operational expenses. Fine grinding also involves multiple stages with finer abrasives, which increases the overall process flow and extends production time. This can result in higher labour costs and lower throughput compared to coarse grinding.

2.3.1.3 Ultra-fine grinding

The best stress release implementation is by using the third method ultra-fine grinding, which is employed in applications that demand extremely smooth and defect-free wafer surfaces. This process uses highly precise grinding techniques with ultra-fine abrasives to achieve minimal surface damage and the least pronounced grinding marks. While ultra-fine grinding significantly reduces surface irregularities, minor marks may still persist, requiring further post-processing treatments such as chemical mechanical polishing (CMP) or wet etching to completely remove surface defects and residual stress.

To mitigate the adverse effects of back grinding, several process optimizations and stress-relief techniques have been implemented. One widely adopted method is the use of a protective grinding tape applied to the wafer's front side to prevent damage to active circuits. Additionally, a multi-step grinding approach, which involves coarse and fine grinding, has been developed to gradually reduce wafer thickness while minimizing stress concentration.

Furthermore, post-grinding stress-relief processes such as chemical mechanical polishing (CMP), wet etching, and plasma treatment have been introduced to smoothen the wafer surface and release residual stress.

Recent advancements also focus on optimizing grinding parameters, such as wheel speed, feed rate, and cooling mechanisms, to minimize stress accumulation. By integrating these stress-reducing techniques, the semiconductor industry continues to enhance wafer reliability, effectively reducing the occurrence of chipping and crack formation in ultra-thin semiconductor wafers. These improvements are crucial in ensuring the durability and functionality of semiconductor devices, particularly in high-performance and safety-critical applications. Towards the backgrinding process, the ultra fine grinding has higher processing cost compared to others due to its complexity, extremely low removal rate and high energy consumption (Tao et al., 2023).

Despite these challenges, coarse grinding remains a commonly used technique due to its speed and effectiveness in material removal. For this evaluation, coarse grinding has been deliberately selected as it represents the most stringent test of chipping performance. Its ability to create extreme conditions highlights the limitations of existing wafer handling and dicing methods, providing a valuable benchmark for assessing improvements introduced by techniques. By focusing on the challenges posed by coarse grinding, this study aims to develop strategies to minimize defects and optimize wafer stability, ultimately contributing to enhanced yield, device reliability, and manufacturing efficiency in the semiconductor industry.

2.3.1.4 Summary of researcher’s activities to minimize wafer stress during backgrinding process

Researchers did many activities to minimize stress on the wafer during the wafer back grinding process to minimize chipping and crack issues during the wafer dicing process. Deng et al. (2025) aims to reduce chipping and crack formation during silicon wafer polishing. A 3D finite element model was developed to simulate thermal fields caused by frictional heat, factoring in polishing pressure and rotation speed. The model identified areas of temperature rise that could lead to thermal stress and microcracks. Experimental tests were conducted to validate the simulation, measuring material removal rate, surface temperature, and wafer quality using different abrasive pads and slurries. Results showed that high localized temperatures increased chipping risk, but lowering speed and pressure effectively reduced thermal gradients and stress as illustrated in Figure 2.6.

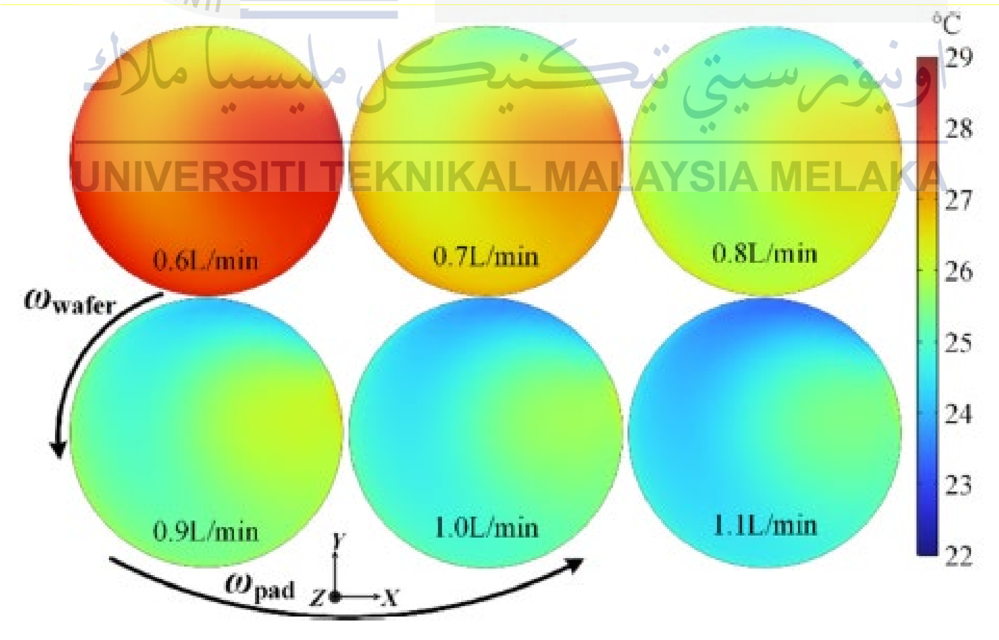


Figure 2.6: Lower slurry flow rate produced higher temperature which increase chipping risk (Deng et al., 2025)

The study found that using fine abrasive pads and optimizing parameters improved surface uniformity and reduced defects. The close match between simulation and experiments confirmed the model's reliability. Controlling thermal conditions is key to minimizing wafer chipping and cracks.

Dong et al. (2021) investigated the influence of laminating tape on the quality and mechanical integrity of silicon wafers during the backgrinding process. The findings demonstrated that the application of laminating tape on wafer surface during backgrinding serves a critical function in mitigating wafer breakage, as illustrated in Figure 2.7. Specifically, the taping provides cushioning and edge sealing effects, which play a significant role in absorbing and distributing the mechanical stress generated during grinding. These protective mechanisms contribute to reducing the incidence of crack initiation and propagation, thereby enhancing wafer strength and overall process reliability.

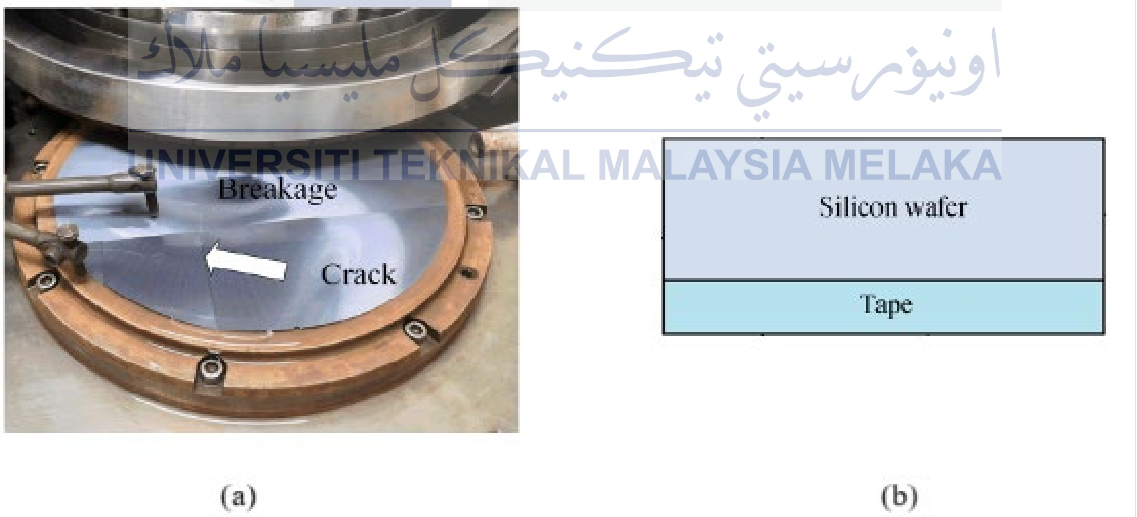


Figure 2.7: Laminate tape function (a) Wafer breakage and crack during grinding (b) Taping on the wafer surface for grinding stress absorbant (Bryan Christian S. Bacquian, 2020)

The laminating tape was then detaped once the grinding activities were completed. The cushioning effects have given some ideas to implement during wafer dicing as a cushioning effect as well. However, unlike backgrinding where the tape must be removed before dicing, the proposed double-sided wafer mounting technique necessitates that the surface mounting tape remains on the wafer during the dicing process. Therefore, further evaluation is required to assess the feasibility of maintaining the tape throughout dicing, as well as to establish effective methods for its removal upon completion of the process.

The conventional mechanical dicing process is known to induce substantial mechanical stress and vibration during the cutting operation, which frequently results in backside chipping and die crack formation (Bryan Christian S. Bacquian, 2020c). These backside chippings act as critical fracture initiation sites on the rear surface of the diced wafers, consequently leading to a significant reduction in die strength and overall structural integrity. To address this limitation, a novel process integration known as Dicing Before Grinding (DBG) has been introduced. This breakthrough technology alters the conventional sequence by performing the dicing process prior to wafer thinning, thereby minimizing the mechanical stress and vibration transmitted to the wafer during singulation.

As a result, DBG effectively mitigates the occurrence of backside chipping and die cracking, offering a promising solution for enhancing die robustness and improving yield in semiconductor manufacturing. From DBG wafer dicing results, using half-cut dicing based on the original wafer thickness using 40K and 50K blade rotation per minute (RPM) showed no significant chipping performance on topside chipping. However, the usage of backgrinding tape with lower adhesion before UV curing manages to eliminate the whisker issue during the process.

In a standard IC manufacturing flow chart, after the wafer back grinding process, the wafer undergoes the wafer mounting process, where the silicon wafer is affixed to an adhesive mounting tape according to the process flow.

2.3.2 Wafer Mounting

The semiconductor wafer mounting process is the second pre-assembly process after the wafer back grinding process. It is a critical step in handling the silicon wafers before the wafer dicing process and back-end semiconductor manufacturing. This is because wafer mounting is the process of handling the wafer after the backgrinding process is completed. If not handled properly, the wafer mounting process can cause a broken wafer, resulting in 0% of assembly yield. By providing stability through higher adhesion tape such as UV tape, good mounting parameters and the correct selection of wafer mounting tape material, wafer mounting can minimize vibrations and movement during wafer dicing (Mohd Khairul et al., 2022), which are key factors in preventing defects such as broken wafers, excessive chipping, cracking, or edge damage. Additionally, it protects the wafer's integrity throughout handling, reducing the risk of mechanical stress and contamination. Overall, wafer mounting is essential for maintaining reliability and efficiency in the manufacturing process.

In the wafer mounting process, air bubbles and foreign particles are the main enemies which should be eliminated during the initial setup. Rahman and Nayan (2018) claimed that air bubbles and foreign particles on the wafer's backside interrupt the adhesion during the wafer mounting process, causing instability and uneven support(Rahman and Nayan, 2018). This increases vibration from high dicing blade rotation during dicing, causing die movement during dicing, including fly die issues, leading to excessive chipping, cracks, and scratches, resulting in reduced die quality. Such defects cause lower yield, compromise reliability, and negatively impact the overall manufacturing process.

In this basic wafer mounting process, the silicon wafer is securely attached to a mounting tape that adheres to the wafer ring, ensuring the silicon wafer sticks well on the wafer mounting tape and remains stable during the cutting and separating of individual semiconductor die. The wafer mounting requires a wafer ring, mounting tape, scrapper (optional for manual process) and the wafer itself to complete the process. For the automatic wafer mounting process, the wafer and wafer ring were picked by the machine pick and place arm and placed it to chuck table area. The vacuum then was turned on to hold the wafer and wafer ring firmly. In this stage, it is important to ensure the wafer mounting chuck table is clean before the wafer mounting process starts to ensure wafer mounting is free from air bubble issues. Figure 2.8 illustrates the materials used during the conventional wafer mounting process.

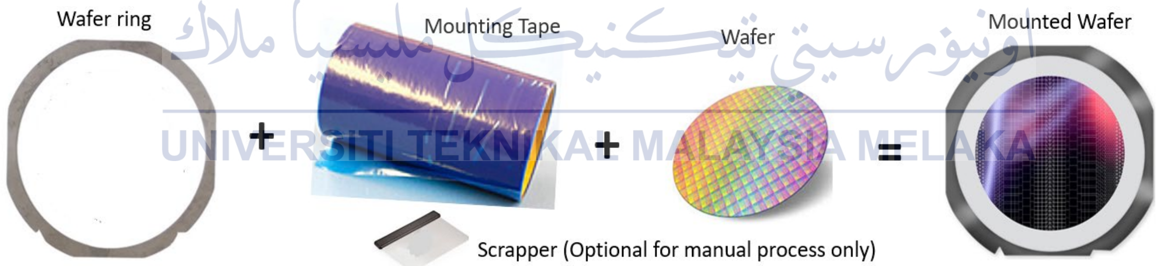


Figure 2.8: Wafer mounting process materials

In the wafer mounting process, besides the wafer mounter parameter, the mounting tape plays a vital role in achieving good chipping performance after the wafer dicing process (Wu et al., 2024). Three types of mounting tapes available in the market and used during semiconductor manufacturing and the behaviour to the wafer mounting process will be explained.

2.3.2.1 Non-UV Tape

Non-UV tape is the standard tape used for the wafer dicing process. It does not require UV curing since the adhesion of the non-UV tape is not high and manageable for the pick-up process. It is normally used for wafer thickness ≥ 300 μm and non-critical devices. The mounting technique involves a single-sided wafer area only at the wafer back area where the contact between mounting tape during the wafer mounting process and the illustration can be referred to Figure 2.9. Take note during the wafer dicing process it was based on the single-sided wafer mounting condition and wafer holding capability is still considered low.

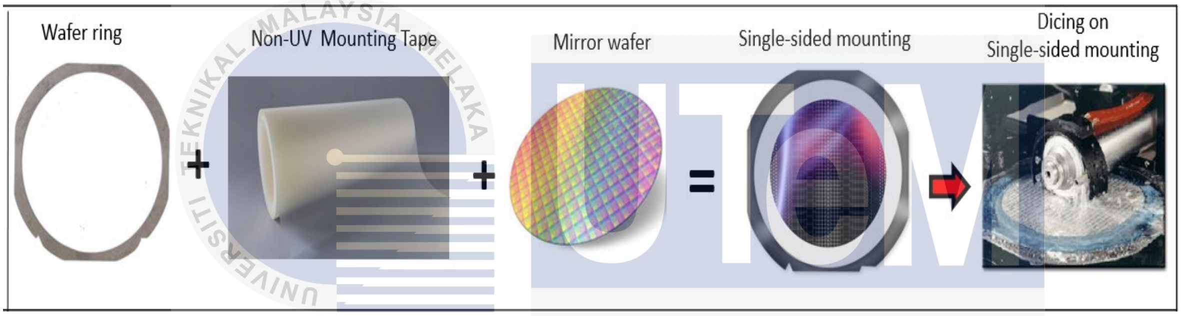


Figure 2.9: Non-UV Tape wafer mounting and wafer dicing process flow

Non-UV mounting tape is commonly used in semiconductor wafer mounting processes. It relies on pressure-sensitive adhesive (PSA) to securely hold the wafer during dicing. Unlike UV tapes, non-UV tapes do not require exposure to ultraviolet light for adhesive weakening. They provide consistent adhesion throughout the process and are designed for straightforward removal. However, the wafer mounting tape adhesion strength may vary with environmental factors like temperature and humidity, which can lead to challenges in certain applications. Non-UV tapes are generally suitable for standard wafers and applications where precision die separation and low adhesion residue are less critical.

Non-UV tapes are more cost-effective compared to UV tapes, making them a preferred choice for low to medium-complexity semiconductor manufacturing processes. Their simpler handling and lack of UV-curing equipment requirements reduce initial capital investment and operational costs. However, their limitations in handling thin or fragile wafers and potential residue issues during die separation may lead to higher indirect costs in specific scenarios, such as increased defect rates or lower yield for high-precision applications. Therefore, the cost-effectiveness of non-UV tapes depends on the specific manufacturing requirements and the balance between upfront tape costs and overall process efficiency.

2.3.2.2 UV Tape

The UV tape possesses superior adhesive properties compared to non-UV tape and necessitates UV curing to reduce the adhesion strength for the die pick-up procedure. UV tape exhibits a higher adhesive strength compared to non-UV tape, resulting in a significant improvement in chipping performance (Mohd Khairul et al., 2022). The higher adhesion specifications contribute to enhanced stability during the dicing process which holds the wafer backside firmly and reduces vibration. UV tape is utilized for the precise pick-up of delicate dies in devices that are prone to chipping. The utilization of UV tape is mostly determined by the die thickness being less than 300 µm, or it may vary to thicker wafer thickness as well depending on the specific applications and the level of criticality for the device. The mounting procedure for UV tape closely resembles that of non-UV tape, with the exception that it necessitates an extra UV curing step following the wafer dicing process. This is done to decrease the tape stickiness and facilitate the delicate removal of individual dies.

Adhesion of UV tape decreases after UV curing due to the chemical changes that occur when the tape is exposed to ultraviolet light during UV curing. UV tapes are typically made with adhesives containing photoinitiators, compounds that react to UV light. When the tape is exposed to UV radiation, the photoinitiators trigger a polymerization or crosslinking process in the adhesive, causing the material to cure (Kim and Lee, 2021). This curing process changes the adhesive's structure from a more flexible, tacky state to a more rigid and less sticky (Hao et al., 2019). As a result, the tape's ability to bond effectively to surfaces decreases because the adhesive becomes less viscous and less able to conform to surface irregularities. This reduction in stickiness and bonding strength is why adhesion decreases after UV cure. The tape is designed to stick well before curing and be easily removed after the curing process, making it ideal for applications like wafer dicing or temporary bonding during manufacturing.

The illustration of wafer mounting, wafer dicing and UV curing for UV mounting tape is illustrated in Figure 2.10. Again, the wafer dicing process was based on the single-sided conventional wafer mounting process, and wafer holding capability is still considered unstable. This research assesses wafer mounting techniques for enhancing wafer gripping performance using higher adhesive UV tape application.

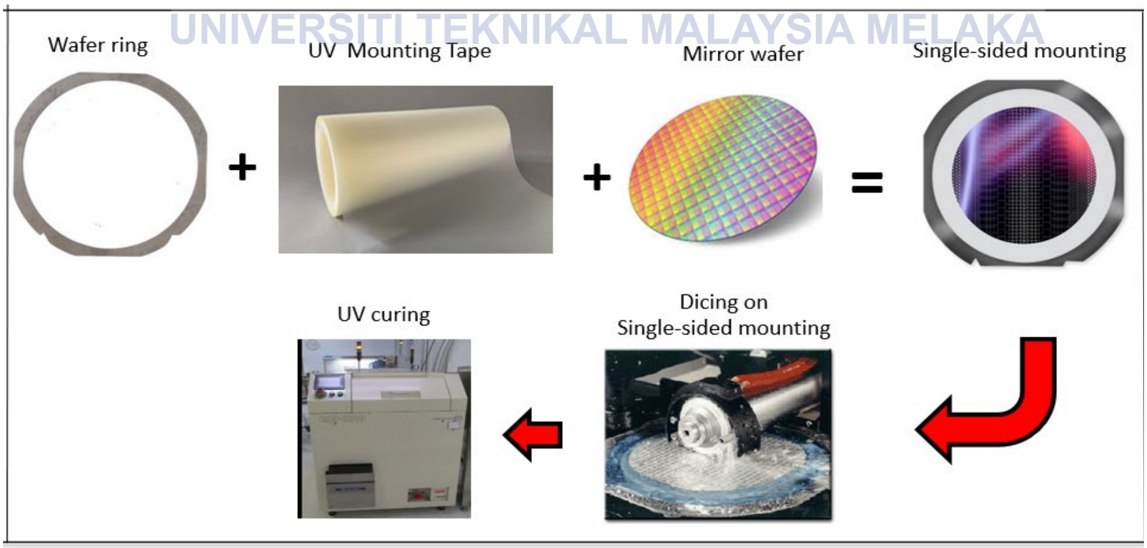


Figure 2.10: UV Tape wafer mounting and wafer dicing process flow

2.3.2.3 Dicing Die Attach Film (DDAF)

Dicing Die Attach Film (DDAF) is an advanced composite material widely utilized in semiconductor manufacturing to enhance both die preparation and bonding efficiency. It integrates a dicing tape with a pre-applied die attach adhesive, enabling it to fulfill two essential functions: providing mechanical support during wafer singulation and facilitating die attachment to substrates during the packaging process. This dual-purpose structure simplifies the overall assembly workflow, reduces material handling, and minimizes potential defects. DDAF is particularly beneficial for handling ultra-thin dies, typically less than 250 µm in thickness, as noted by B. C. Bacquian and Gomez (2020). These thin dies often present challenges when conventional glues are used for attachment to leadframes or in stacked-die configurations. In such cases, DDAF offers a reliable alternative, ensuring uniform adhesive distribution and improved die bonding performance, while maintaining die attach quality and package reliability.

Thin dies will suffer glue-on-die issues on the conventional method as the glue easily climbs on the die surface after pressure is applied to it and DAF acts as a double-sided tape that sticks the die on the leadframe or die surface for stack die application by removing the glue application on the conventional die attach process. DDAF is normally applied on Ball Grid Array (BGA) stacked die application which makes it impossible to use glue for thin dies.

DDAF is particularly beneficial for high-density packaging applications and thin wafer handling, as it provides excellent adhesion while ensuring minimal damage or deformation to the wafer during dicing. The adhesive layer of DDAF is designed to maintain strong adhesion during dicing and allows easy release or curing during die bonding DDAF guarantees the accurate placement of the cut die into the substrate or leadframe, ensuring optimal electrical and thermal connectivity.

The Dicing Die Attach Film (DDAF) process flow begins with the application of a protective tape to the front side of the unthinned wafer. This laminated wafer is then flipped, and the back side undergoes backgrinding to achieve the target thickness as specified in the bonding diagram. Upon completion of the grinding process, the wafer is subjected to a cleaning step to remove particulates and grinding residues. Subsequently, die attach film (DAF) tape is laminated to the back side of the wafer as part of the wafer mounting process. Following this, the front-side lamination tape is carefully removed, and wafer dicing is performed, as illustrated in Figure 2.11 (Fumita et al., 2019). However, DDAF remains using a single layer of wafer mounting tape during the wafer dicing process which is still exposed to vibration during the wafer dicing process and the DAF tape will not be used in this research as it is not in the research scope.

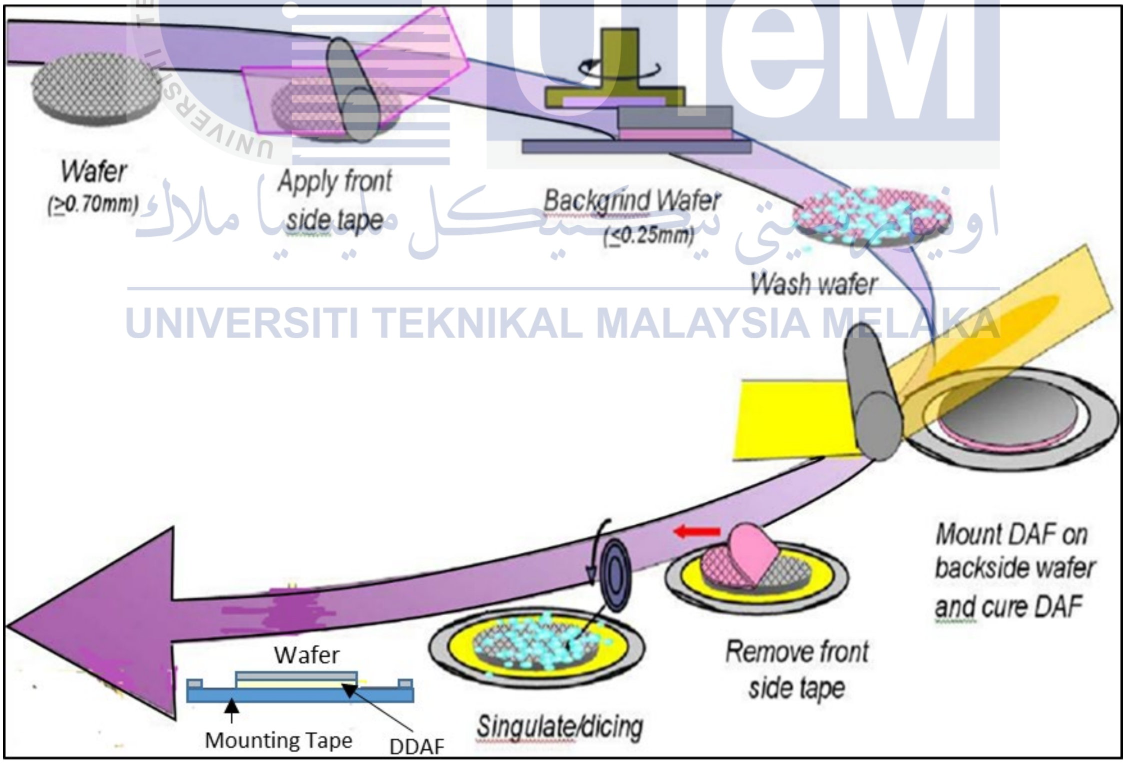


Figure 2.11: Dicing Die Attach Film (DDAF) and wafer dicing process flow

To comprehensively understand the characteristics of each mounting tape and to determine the most suitable option for the evaluation, Table 2.1 presents a detailed comparative analysis. This table serves as a reference to support the selection of mounting tapes based on their material properties, functional performance, and compatibility with the specific requirements of the wafer dicing and mounting processes.

Table 2.1: Comparison of DDAF, Non-UV Tape, and UV Tape

Feature	DDAF	Non-UV Tape	UV Tape
Application	Combines dicing and die attach application. Mainly used for thin wafers.	Wafer dicing only; suitable for low-stress and standard wafer thickness applications.	Wafer dicing only; ideal for thin wafers and any critical device.
Adhesion	Strong adhesion during dicing; adhesive cured during die bonding.	Fixed adhesion level without UV curing.	High adhesion at the initial stage but adhesion reduces upon UV exposure for easy die pickup.
Usage	High-end processes where integration of dicing and bonding is needed.	Basic dicing where UV curing is unnecessary.	Applications requiring UV curing and precise die pickup after dicing.

Cost	Higher due to dual functionality and advanced technology. There is pre cut version at mounting tape.	Lower since no UV curing machine is required and suitable for standard manufacturing	Moderate, balancing functionality and cost. Require UV curing process.

The evaluation necessitates cost-effective approaches and as well enhancing the chipping performance. For this study, only non-UV and UV tapes will be assessed in the context of wafer mounting techniques, as Dicing Die Attach Film (DDAF) is considered unsuitable due to the use of non-critical wafer thicknesses and the non-involvement of die attach processes. Among the three mounting tape types reviewed, each demonstrates specific advantages and limitations. However, a common characteristic across all mounting tapes is the similarity of the single-sided wafer mounting application observed, as illustrated in Figure 2.12. In this conventional technique, despite using high tape adhesion, the wafer is solely secured from the backside area. As noted by Lin and Cheng, (2014) vibration remains a persistent challenge in single-sided mounting configurations, especially on a rough wafer surface. Even with high-adhesion tapes, the inability to constrain the wafer from both top and back surfaces leaves a potential for movement during dicing, indicating a clear opportunity for enhancing wafer stability through mounting strategies.

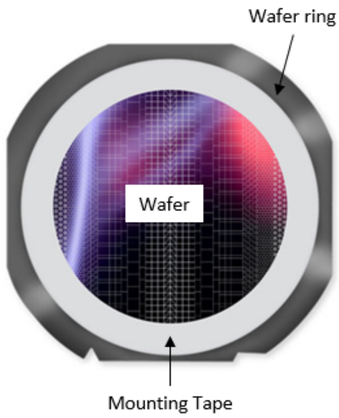
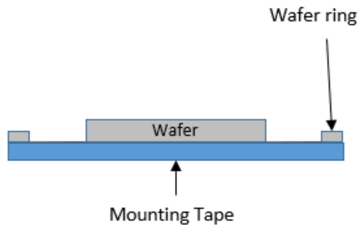
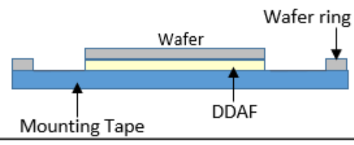
Mounting Tape Type	Conventional single-sided mounting technique	
	(Top view)	(Side view)
1) Non UV-Tape		
1) UV Tape		
1) DDAF		

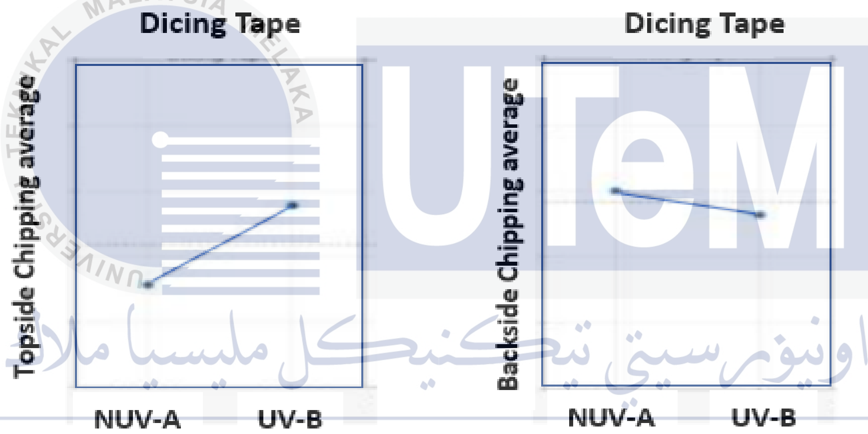
Figure 2.12: All mounting tapes using the conventional single-sided mounting technique

Despite the application of conventional wafer mounting techniques utilizing various mounting tapes, excessive chipping and crack formation persist during the wafer dicing process. Therefore, it is essential to evaluate an alternative approach that provides support on both the front and backside surfaces of the wafer which aims to improve the chipping performance through the wafer mounting technique.

2.3.2.4 Summary of researcher's activities to minimize wafer stress during wafer mounting process

In the context of the wafer mounting process, this chapter presents a summary of various methodologies employed by previous researchers to achieve optimal mounting outcomes. These activities were specifically designed to minimize mechanical stress exerted on the wafer during processing, thereby enhancing chipping performance and overall die integrity. The compiled approaches provide valuable insights into best practices for improving wafer handling and singulation reliability. Yongbing Wu et al. (2024) performed a feasibility study to improve chipping and die crack through UV and non-UV mounting tapes, different cutting methods and dicing blades. Full cut was selected for these activities due to the superior Unit Per Hour (UPH). Full cut is defined as the dicing blade directly cutting through the wafer during the process, and the definition is the same as single cut used towards the project activities.

The result in Figure 2.13 shows the non-UV tape A (NUV-A) and UV Tape B (UV-B) chipping performance with the optimized single-cut method.



(a) (b)

Figure 2.13: Chipping results (a) Topside chipping (b) Backside chipping

Figure 2.13 present the average chipping performance on the topside and backside of the wafer, respectively, for two different types of dicing tapes: NUV-A (non-UV) and UV-B. In Figure 2.13 (a), the topside chipping average shows a noticeable increase when using UV-B tape compared to NUV-A, indicating that the UV-B tape may contribute to slightly higher topside chipping. In contrast, Figure 2.13 (b) demonstrates a reduction in backside chipping average when switching from NUV-A to UV-B tape, suggesting that UV-B performs better in minimizing backside chipping. These results highlight a trade-off between topside and backside chipping performance depending on the dicing tape used.

However, this result contradicts Mohd Khairul et al. (2022), who found that UV Tape had significantly lower chipping compared to non-UV tape as displayed in Figure 2.14. Thus, it is best to evaluate both mounting tapes to understand which is suitable for the double-sided wafer mounting application.

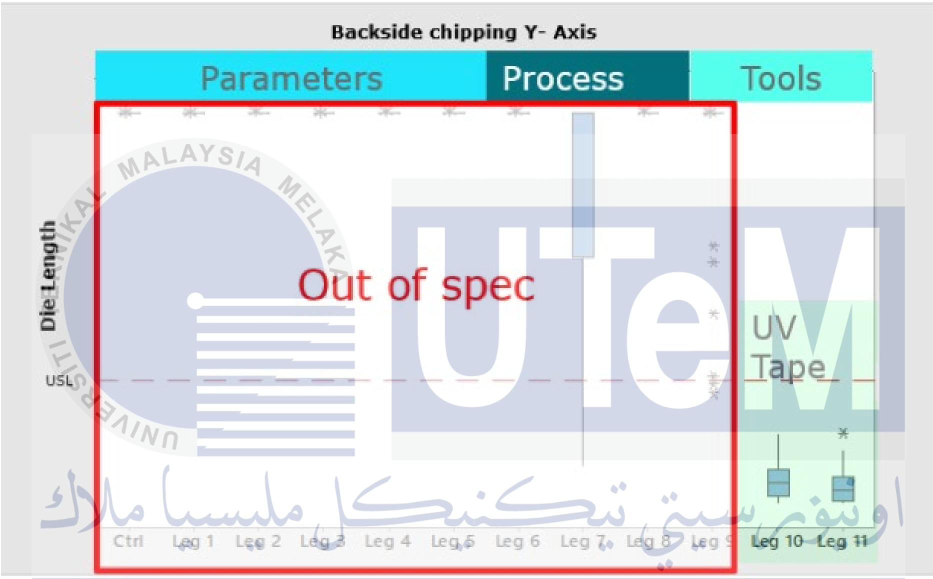
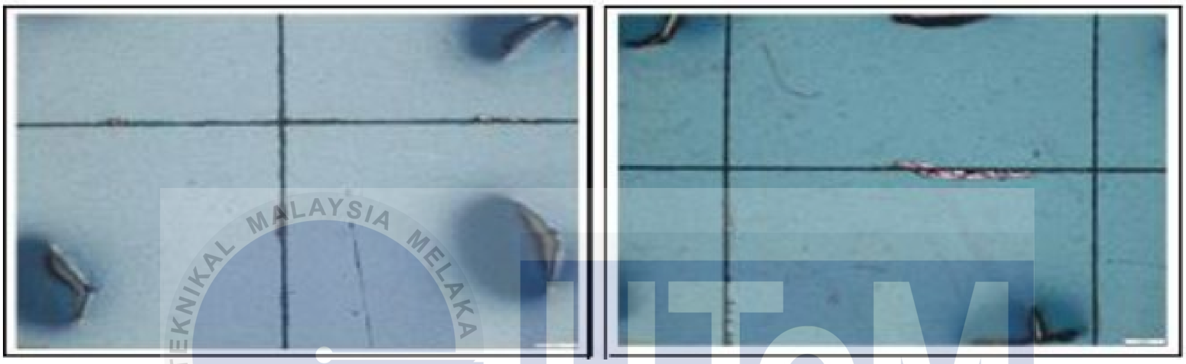


Figure 2.14: Backside chipping length DOE results.

Higher mounting tape adhesion is preferable to researchers due to its holding capability to the wafer, making it stable during dicing, which results in lower chipping performance. However, the wafer backside with TiNiVag metalization have some issues with remnant left on mounting tape after die pick up affects the backside chipping performance, which requires a pre-assembly optimization process. Wafer baking is a critical process step employed to enhance the adhesion between the wafer and the mounting tape. This increased adhesion strength is essential to ensure that the individual diced units remain securely affixed to the tape throughout subsequent processing steps, particularly during wafer sawing and post-dicing cleaning. Sufficient adhesion prevents the detachment or displacement of the dies, thereby eliminating the occurrence of die flying or misalignment, which could otherwise compromise yield and downstream handling reliability.

Vijayakumaran et al. (2022) identified that the single cut method without baking produced a reduction of remnants left on the mounting tape as displayed in Figure 2.15.



(a) (b)

Figure 2.15: Single cut performance (a) reduction of remnants on single cut with no bake method (b) high remnant on single cut with baking method

Alternatively, skipping the baking process offers a more cost-effective and time-efficient approach than conventional AuAs/Ag/Ni/Ag backside metallization, which requires baking. This process simplification reduces overall cycle time and operational costs, making it advantageous for improving throughput in semiconductor manufacturing. This indicates that the single-cut method is still capable of achieving acceptable chipping performance, provided that appropriate optimization is applied to the wafer mounting process to enhance cutting stability and minimize mechanical stress.

Gan et al. (2024) study revealed that mounting tape properties, particularly UV tape thickness and adhesion strength after UV curing (< 300 mN/25 mm), have a significant impact on chipping performance during the dicing of Light Shielding Mask (LSM) glass. Two UV tapes were evaluated: Tape A (thicker adhesive layer) and Tape B (thinner adhesive layer), both with polyolefin (PO) base film and low post-UV adhesion (< 300 mN/25 mm). Tape A, due to its thicker adhesive, caused increased blade clogging, higher spindle current, and frequent interval dressing, which collectively led to greater backside and sidewall chipping.

In contrast, Tape B's thinner adhesive layer minimized blade clogging, required less frequent dressing, and resulted in better chipping performance on all surfaces (top, sidewall, and backside). The lower adhesion after UV curing also reduced the risk of adhesive residue, leading to cleaner die separation.In summary, thinner UV tape with low post-cure adhesion (< 300 mN/25 mm) provides superior support during dicing by ensuring better vibration control, minimizing blade contamination, and significantly reducing chipping defects, thereby improving overall process reliability and yield.

An analysis of previous research activities reveals that all approaches used the conventional single-sided wafer mounting technique. The majority of these studies utilized both UV and non-UV mounting tapes, varying in adhesion strength, to optimize wafer stability during dicing. In certain cases, thermal baking was incorporated as an additional process step to enhance the adhesive performance of the mounting tape, thereby improving wafer grip and preventing die detachment or "flying die" occurrences during singulation.

2.3.3 Wafer Dicing

Wafer dicing, also referred to as wafer sawing, is a critical process within the front-end (FE) assembly area of semiconductor manufacturing. This process involves the separation of a single processed wafer into individual dies, which may range in number from hundreds to several hundred thousand, depending on the specified die dimensions, as illustrated in Figure 2.16. A direct correlation exists between die size and the total quantity of dies per wafer. The smaller die sizes result in a higher number of dies produced per wafer, whereas larger die sizes will reflect lower total dies produced per wafer. This stage is essential for ensuring the dimensional precision and structural integrity of each die, directly influencing downstream packaging and device reliability.

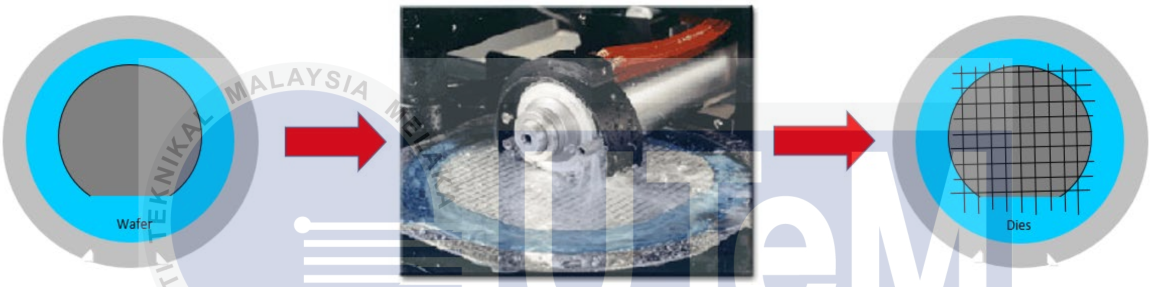


Figure 2.16: Wafer dicing operation

During the wafer dicing process, a high-speed rotating diamond blade is applied to separate the brittle silicon wafer into individual dies. Due to the inherent brittleness of silicon, this mechanical cutting process induces localized stresses, often leading to chipping and the initiation of microcracks at the die edges. The interaction between the diamond blade and the wafer material generates alternating tensile and compressive forces, which can exacerbate defect formation if not properly controlled. Factors such as blade type, feed rate, spindle speed, and water application play a crucial role in determining the extent of chipping and crack propagation. If not mitigated, excessive chipping, which causes cracks as shown in Figure 2.17, can compromise the structural integrity of the dies, leading to latent failures during subsequent semiconductor assembly and field applications.

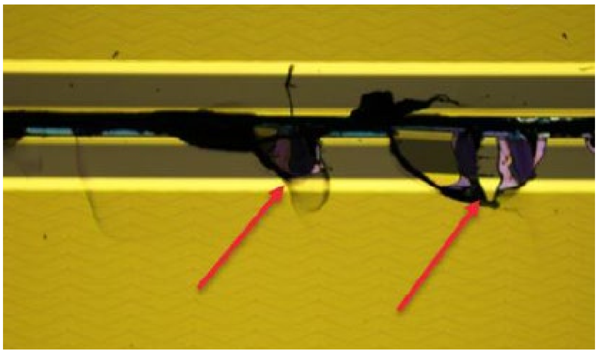


Figure 2.17: Die chipping samples (Xue et al., 2021)

Chipping and crack formation are commonly observed when wafer mounting and dicing parameters are not properly optimized, highlighting the critical importance of this initial stage in the semiconductor manufacturing process. Within the wafer dicing process, precise control of dicing parameters is essential to achieve minimal chipping and ensure overall die quality. According to Zhang et al. (2021), two primary types of chipping such as topside and backside must be inspected after the wafer dicing process as part of quality assurance procedures. Chipping can lead to the initiation of cracks, which represent one of the most detrimental defects in semiconductor fabrication. As noted by Li et al. (2021) such cracks may reduce the device's reliability and later result in field failures at the customer level.

In the wafer dicing process, the selection of the appropriate diamond blade specifically concerning diamond concentration, grit size, and bond type is critical for achieving low chipping performance, as emphasized by Agudon and Bacquian (2021). Additionally, precise control of blade exposure and kerf width is essential for maintaining optimal dicing quality. Blade exposure refers to the length by which the blade extends from the blade hub, as illustrated in Figure 2.18. Excessive blade exposure can result in unstable, wavy cuts and increase the risk of blade breakage, while insufficient exposure may lead to incomplete cuts, as the blade fails to penetrate the entire wafer thickness. Kerf width, defined as the width of the material removed during cutting, must be carefully selected especially for wafers with narrow street widths. Adequate clearance between the kerf and the saw street is necessary to ensure cutting precision and minimize the risk of wafer damage during the dicing process.

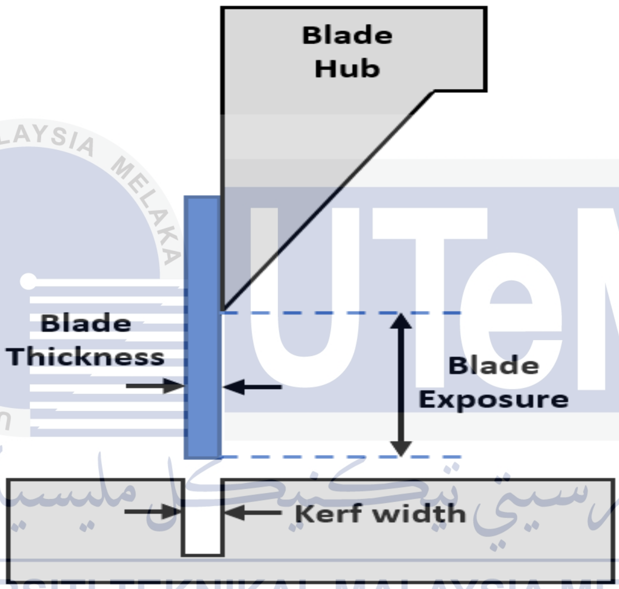


Figure 2.18: Illustration of blade exposure and kerf width

2.3.3.1 Key parameter in wafer dicing

During the wafer dicing process, it is essential for researchers and process engineers to optimize and stabilize key operational parameters to improve chipping performance and ensure consistent die quality. Critical parameters such as blade rotational speed (RPM), feed rate, cutting method, and blade height must be carefully optimized and subsequently fixed throughout the dicing operation. Each wafer possesses unique material and structural characteristics; therefore, parameters must be tailored to the specific requirements of the device.

Once the optimal settings are established, they should be locked into the dicing equipment to maintain process consistency and repeatability, as defined by the engineer following device specifications to ensure acceptable chipping performance during manufacturing.

2.3.3.1.1 Blade Rotation Per Minute (RPM)

Blade Rotation Per Minute (RPM) refers to the rotational speed of the dicing blade during the cutting process and is defined as the number of complete 360-degree rotations the blade performs within a one-minute interval. This parameter plays a critical role in determining the quality of the wafer dicing outcome, particularly concerning chipping performance. Variations in blade RPM can significantly influence both topside and backside chipping. For silicon wafers, higher blade RPM is generally associated with improved topside chipping outcomes, as reported by T.-J. Su et al. (2018), while lower blade RPM has been shown to enhance backside chipping performance (Zhang et al., 2021). Therefore, the optimization of blade RPM must be carefully balanced to meet specific dicing quality requirements. A schematic representation of blade RPM and its relation to the dicing process is illustrated in Figure 2.19.

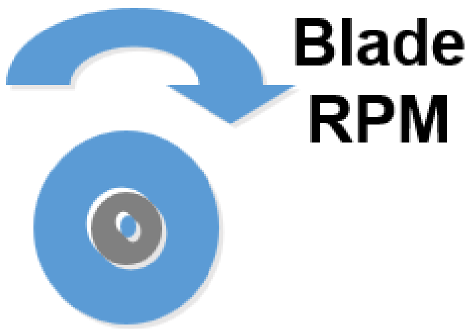


Figure 2.19: Blade RPM illustration

However, Seong-Min Lee (2016) reported that excessively high feed speeds exceeding 60,000 RPM contribute to higher chipping damage, particularly in thinner wafers, thereby compromising die integrity. He further noted that reducing blade thickness can mitigate this effect by minimizing mechanical stress during cutting, which in turn helps preserve device reliability. In alignment with these findings, Zhang et al. (2021) and Wu and Doe (Wu and Doe, 2024) highlighted that elevated blade RPMs are associated with machine-induced vibrations, which can worsen chipping during the wafer dicing process. Nevertheless, these adverse effects can be effectively mitigated through comprehensive process optimization, as blade RPM is only one of several interrelated factors influencing vibration and chipping performance. Therefore, a multi-parameter approach is required to achieve optimal dicing outcomes while maintaining wafer integrity.

2.3.3.1.2 Feed Speed

Feed speed is defined as how fast the wafer moves towards the blade for cutting purposes. The mounted wafer will placed on the wafer-dicing chuck table and the feed speed setting will determine the movement speed towards the fixed rotation blade during the dicing process as illustrated in Figure 2.20. The feed speed setting is important towards the chipping performance and the completion time for the dicing process. Based on Hong Zhang (2022) findings, feed speed and cutting height are significant factors to reduce the risk of chipping and achieve high yield in wafer dicing. The higher the feed speed the faster the dicing process and the higher the machine UPH. To evaluate chipping performance, a design of experiment (DOE) is necessary to comprehend the factors influencing chipping, as it is contingent upon blade specifications and wafer thickness. The feed speed impacts the chipping performance during wafer dicing by affecting the condition of the blade surface and the cut distance (Lin and Cheng, 2014).

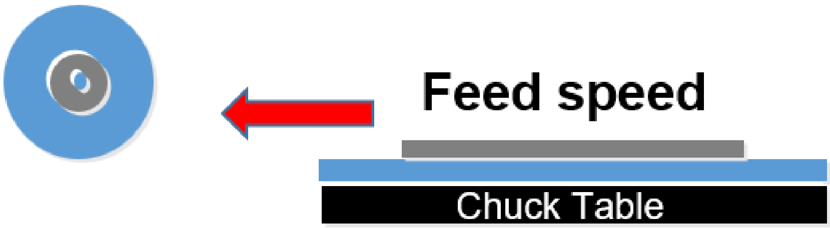


Figure 2.20: Feed speed illustration

2.3.3.1.3 Cutting method

Within the scope of this project, the cutting method was standardised to the single-cut dicing approach. Among the various singulation techniques employed in semiconductor manufacturing, the single-cut method is recognised for its simplicity and efficiency. This technique involves a one-pass cutting process in which the dicing blade penetrates the full thickness of the wafer in a single motion, thereby separating the individual dies in one step. The single-cut method offers operational advantages, such as reduced process time and minimal handling, which are particularly beneficial for comparative evaluations involving mounting techniques.

In semiconductor manufacturing, a single cut is preferable for non-critical devices because of its simplicity and relatively straightforward process that requires only one pass of the dicing blade reducing overall cycle time and suitable for high-volume production environments. Single-cut is also considered cost-effective since it involves only one type of blade (Liu et al., 2016) compared to more complex cutting such as step cut or multi-cut which require multiple passes of the dicing blade and types of blade.

A single-cut dicing approach also referred to as the full-cut method was deliberately chosen due to its challenging nature in balancing topside and backside chipping performance, as highlighted by Sanamthong and Chutima (Sanamthong and Chutima, 2020). Moreover, this method is recognized for its ability to achieve higher units per hour (UPH) compared to the alternative cutting methods (Wu et al., 2024)(Liu et al., 2016).

However, single-cut has its challenges and limitations. The primary challenges of single-cut dicing are higher chipping results (Jiun et al., 2006) with more potential for cracks occurrence (Jiun et al., 2004). This is due to the force exerted during the single cut increasing the blade loading (T. J. Su et al., 2018), which creates stress points at the edges of the cuts and generates higher chipping performance. This is where double-sided wafer mounting was evaluated to see whether the chipping level could be improved.

2.3.3.1.4 Blade height

In the wafer dicing process, the blade height is a crucial parameter that directly affects the quality, precision, and yield of the diced semiconductor dies. Blade height refers to the extent to which the dicing blade penetrates the wafer during the cutting process. Controlling this height is essential to achieve clean and accurate cuts, minimize damage to the wafer and dies, and ensure optimal performance of the final semiconductor products. The blade height must be carefully adjusted according to the wafer's thickness and the mounting tape. Overcutting or undercutting can lead to various issues that compromise the integrity of the semiconductor dies and the overall yield of the process.

2.3.3.1.5 Cooling water

The application of cooling methods, such as the use of deionized (DI) water during wafer dicing, has been shown to significantly reduce thermal stress and the associated risk of cracking. Enhanced water flow within the cooling system, when combined with optimized cutting sequences, effectively minimizes the occurrence of sidewall cracks. Notably, one study reported a decrease in defect rates from 8% to 3% following improvements in the dicing cooling process crack (Sukor, 2022). Cooling not only stabilizes wafer temperature but also helps preserve blade condition and reduces mechanical stress, especially a critical factor when processing wafers with high-density metallization. Consequently, although cooling is generally beneficial in mitigating both thermal and mechanical stresses, comprehensive process optimization encompassing water flow rate, dicing parameters, and material-specific properties is essential to fully prevent cracking and delamination during and after the dicing operation.

2.4 Current wafer singulation techniques in semiconductor industries

Numerous singulation techniques have been developed and implemented within the semiconductor industry to address the increasing demands for high-precision die separation. The primary objective of the singulation process is to produce individual dies that conform to stringent quality standards while ensuring their readiness for downstream assembly, particularly the die attach process. The selection of a suitable singulation method is typically guided by factors such as wafer complexity, device architecture, die size, and optimum yield. Each method presents distinct advantages and limitations in terms of precision, throughput, and chipping performance. The following section outlines the principal wafer singulation techniques currently utilised in semiconductor manufacturing. These approaches are applied strategically to enhance chipping quality, improve edge integrity, and ensure mechanical stability of the diced dies, particularly in advanced packaging applications where minimal defectivity is critical for device reliability and long-term functionality.

2.4.1 Dicing after grinding (Current method)

The Dicing After Grinding (DAG) method, utilized in the current assessment, represents the fundamental singulation approach widely adopted within the semiconductor industry. Its prevalence is attributed to its operational simplicity, characterized by a streamlined process flow and minimal processing steps. DAG offers the advantage of achieving high unit per hour (UPH) throughput, rendering it the most efficient and time-effective technique when compared to alternative singulation methods.

The DAG process initiates with wafer thinning, wherein the wafer's thickness is mechanically reduced through backgrinding to meet the required thickness specifications, followed by wafer dicing to cut the wafer into individual dies (Heidenblut et al., 2024). Within the DAG method, vibration during dicing has been consistently reported as a significant contributor to increased chipping behaviour (Xue et al., 2018)(Liu et al., 2023), making it a representative worst-case scenario in terms of chipping quality. According to Mohd Khairul et al. (2022), sources of vibration stem from various factors including mounting tape properties, dicing parameters, cutting methods, and blade types, all of which can exacerbate chipping and crack formation. To date, only the work of Au-Zou Tai has focused on reducing machine-induced vibration; however, this approach involved redesigning the vibration-resistance base of the dicing machine. While the proposed solution demonstrated improved structural stability through finite element analysis (FEA) no experimental vibration data were provided to validate the vibration reduction performance (Tai and Fang, 2023).

Table 2.2 provides the journal compilation of the researcher's activities to improve chipping and crack issues during the wafer dicing process. The conducted activities demonstrated that the mounting adhered to the established conventional single-sided wafer mounting process. During the wafer dicing process, numerous researchers have emphasised the theoretical concerns related to vibration, which are believed to contribute to increased chipping issues; however, empirical data to substantiate these claims has not been provided. The evaluation was done only based on the wafer dicing parameter, cutting method and various blade types for chipping improvement activities.

UV tapes have demonstrated potential for reducing chipping in comparison to non-UV tapes, as they maintain a higher level of rigidity during the sawing process. Nevertheless, these inconclusive results are not supported by vibration data and all activities were done with the conventional single-sided wafer mounting technique. Additionally, the largely unexplored potential advantages of double-sided wafer mounting techniques present a valuable area for future research to enhance chipping results after the wafer dicing process and overall device reliability.

2.4.1.1 Summary of researcher's activities to minimize wafer stress during wafer dicing after grinding process (DAG)

For the wafer dicing after the grinding process improvement activities, Table 2.2 presents a comprehensive summary of various experimental and process-based activities conducted by previous researchers over the past decade. These studies aimed to minimize wafer stress and enhance chipping performance, with the ultimate objective of eliminating die cracks and improving overall wafer integrity. The methods explored include adjustments in dicing parameters, such as blade type, spindle speed, feed rate, and cooling systems, as well as the adoption of protective films, optimized tape adhesion, and wafer mounting techniques.

Despite the broad range of implemented strategies and the continuous efforts to refine the dicing process, the issue of crack formation has not been entirely resolved. However, the accumulated results across multiple studies demonstrate a positive trend in reducing the severity and frequency of chipping and cracking incidents. This consistent improvement highlights the effectiveness of certain methodologies in mitigating stress concentrations and improving wafer robustness. Nevertheless, residual cracks still occur, particularly in thinner wafers and those with higher fragility, indicating that the problem remains a critical challenge. Therefore, ongoing innovation and refinement in wafer handling and dicing techniques are essential to fully address this long-standing reliability concern in semiconductor manufacturing.

Table 2.2: Compilation of the researcher's activities to improve chipping and crack issues during the wafer dicing process.

No	Journal reference	Back Grinding process		Wafer Mounting Process				Wafer Dicing process			Vibration analysis	Highlights
				Mounting Tape		Mounting Method						
		Non Polish	Polish	Non-UV Tape	UV Tape	Conventional single-sided wafer mounting	Double-sided wafer mounting	Dicing parameter optimization	Single Cut	Step Cut		
1	Khairul et al. (2022)	No info	No info	✓	✓	✓	✗	✓	✓	✓	✗	Researchers claimed a high backside chipping issue due to vibration by dicing force however no vibration verification was performed. Observed the evaluation based on wafer mounting using a conventional single-sided mounting method which tends to have high

												vibration during the dicing process
2	WL Chin et al. (2016)	No info	No info	No info	No info	✓	×	✓	✓	✓	×	Researchers highlighted the crack issue generated from the backside chipping and the root cause is unknown since improvement is based on the combination of wafer dicing, die attach, and wire bonding. It is best to fix all parameters and evaluate the double-sided wafer mounting technique-.to compare the backside chipping performance and look for crack issues again if any.

3	YH Chiew et al. (2018)	No info	No info	✓	✓	✓	×	✓.	×	✓	×	Researchers claimed UV Tape has better chipping results than non-UV tape using conventional single-sided mounting techniques. UV Tape is said to maintain rigidity during sawing but there is no vibration data to support on the lower chipping performance using UV mounting tape. It is best to perform vibration analysis to support the theory towards chipping performance.
4	Qiuchen Zhang et al. (2021)	No info	No info	✓	✓	✓	×	✓	×	✓	×	The evaluation involved High DOE runs with 2000 die samples. The researchers used the same method, UV tape and non-UV tape. However, all mounting tapes

												were evaluated using conventional single-sided mounting techniques based on the conventional single-sided mounting techniques;
5	(Zhang, Wang and Huang, 2022)	No info	No info	No info	No info	√	×	√	×	×	×	Use conventional single-sided mounting, and dicing parameters evaluation, including backside temperature and water pressure during wafer dicing assessment.
6	(Lin and Cheng, 2014)	No info	No info	No info	No info	√	×	√	×	×	×	Use conventional single-sided mounting, dicing blades evaluation. Cooling water temperature, cutting feed speed, and rotational speed were fixed. The correlation between blade

												surface properties and chipping size was investigated.
7	(Tuurnala and Box, 2015)	No info	No info	No info	No info	✓	×	✓.	×	✓	×	Fix dicing parameter, step cut, Z1 RPM 35K, Z2 RPM 27000, Feespeed 7 mm/s and 2 dicing blades were evaluated. The primary objective of this research was to develop and optimize a step-cut chip dicing process to enhance chipping performance.
8	(Tai and Fang, 2023)	No info	No info	No info	No info	✓	×	×	×	×	✓	No dicing parameter or blade evaluation is involved. Only a Vibration resistance base design was developed using finite element analysis to improve vibration issues. However, no chipping assessment was

												performed by the researcher to relate the dicing machine vibration and chipping performance.
9	(Inoue et al. 2020)	✓	×	No info	No info	✓	×	✓	×	✓	×	The die size 10 × 10 mm^2. Use step cut with 45K RPM for both blades. Feed speed 40 mm/s. Blade height 1st cut 20 µm into wafer 2nd cut 20 µm into tape. Die with grinding marks showed significantly lowest die fracture strength compared to non-grinding marks results.

Across all wafer dicing improvement activities, a common factor observed in all evaluations was the consistent use of the conventional single-sided wafer mounting process. This technique served as the baseline for assessing the effectiveness of various optimization strategies, which the double-sided wafer mounting techniques could be explored. Chipping is an important performance parameter in evaluating the effectiveness of wafer singulation techniques, particularly when assessing improvements in die quality. Previous studies, such as that by (Sumagpang et al., 2020), have demonstrated that transitioning from a single-cut to a step cut method can result in a significant reduction in die chipping up to 95%. However, the step cut technique necessitates the use of two different blade types, leading to increased operational complexity and higher costs, which fall beyond the scope of the present study. Therefore, the single-cut method remains the preferred approach due to its cost-effectiveness, operational efficiency, and simplicity in implementation.

2.4.2 Dicing before grinding

Dicing Before Grinding (DBG) is an advanced process used in semiconductor manufacturing to improve the quality, yield, and handling of ultra-thin wafers (Aizawa et al., 2018). In this method, the wafer is partially diced before the grinding step, allowing for controlled die separation after the wafer has been thinned. The process is especially beneficial for achieving precision dicing of thin wafers while minimizing mechanical stress and damage to the semiconductor dies.

The DBG process involves two key steps: partial dicing of the wafer, followed by wafer thinning through grinding. DBG still produced silicon damage during the wafer-cutting process on the partial cut however, the damages were removed during the grinding process (Bryan Christian S. Bacquian, 2020b). This sequence is designed to avoid the mechanical stress and potential damage associated with traditional dicing methods performed after wafer thinning. However, DBG addresses the backside chipping and die crack issues during silicon wafer dicing as well, reducing die strength and this method is not involved during the activities as it is not in the scope area.

2.4.3 Laser cut after grinding

Laser cut after grinding is a process used in semiconductor manufacturing where the wafer undergoes a back-grinding process to achieve the desired thickness before being diced using a laser cutting technique. This method is increasingly favoured for ultra-thin wafers and high-precision applications, where traditional mechanical dicing methods may introduce excessive stress or damage. The Laser cut after the grinding process involves two critical steps: the thinning of the wafer through back grinding, followed by the use of a laser to separate individual dies. This process sequence allows manufacturers to produce ultra-thin semiconductor dies with high precision while minimizing the risks associated with mechanical cutting methods.

Laser cutting after the grinding process will not be utilized during the evaluation due to its significantly higher associated costs compared to conventional methods. While laser cutting offers potential advantages, such as reduced mechanical stress and improved precision, its economic feasibility is a major concern. The objective of the evaluation is to explore cost-effective solutions for minimizing backside chipping and improving die strength. Incorporating laser cutting would deviate from this objective by introducing an expensive alternative that may not align with industry requirements for performance and affordability. Therefore, the focus remains on optimizing the wafer mounting techniques and using the conventional dicing methods for improved performance.

2.4.4 Laser cut before grinding

Laser cut before grinding is an advanced semiconductor fabrication technique that involves using a laser to dice the wafer before subjecting it to back-grinding to reduce its thickness. This process sequence, which is an alternative to the more traditional dicing methods, allows for precise wafer separation with minimal mechanical stress and offers several advantages when handling ultra-thin wafers. This technique is beneficial for delicate semiconductor materials and advanced packaging applications that require ultra-thin and high-quality dies.

The laser cut before grinding process consists of two main steps: precision laser dicing and wafer thinning via back-grinding. In this technique, the wafer is first partially diced by a laser, creating shallow grooves along the scribe lines. The wafer is then subjected to back-grinding to thin it down to the desired thickness. The laser scribing initiates the separation of dies, and the grinding step completes the process by breaking the wafer along the laser-cut grooves, allowing the dies to be fully separated.

The implementation of laser cutting before grinding process will not be considered within the scope of this evaluation due to its elevated cost implications and its exclusion from the defined research objectives. Although this technique may offer advantages such as reduced mechanical stress and improved cutting precision, its integration necessitates substantial financial investment, rendering it impractical for the current study. The primary focus of this investigation lies in the assessment of conventional dicing techniques in conjunction with wafer mounting methods, particularly to address challenges associated with backside chipping and to enhance the mechanical robustness of thinned wafers.

Consequently, the inclusion of laser cutting before grinding extends beyond the intended framework of this research and is therefore excluded from further consideration.

2.4.5 Plasma dicing

Plasma dicing is an advanced and emerging technique for separating semiconductor wafers into individual dies using plasma etching rather than mechanical or laser cutting methods. Plasma dicing offers several significant advantages over conventional mechanical dicing, including the ability to dice wafers with minimal mechanical stress, reduced risk of chipping and cracking, and improved die strength. This method is particularly beneficial for ultra-thin wafers and applications requiring high precision, cleanliness, and yield, such as in advanced packaging technologies.

In the plasma dicing process, the wafer is first masked with a protective layer, and trenches or scribe lines are defined through lithography or other methods where the dies will be separated. Plasma etching is then used to remove material from these areas, effectively "cutting" the wafer into individual dies by chemically etching the silicon or other materials present in the wafer. Unlike mechanical dicing, which relies on physical contact to cut through the wafer, plasma dicing relies on ionized gas (plasma) to etch away material, enabling high-precision die separation without direct mechanical force.

Plasma dicing will not be adopted in this evaluation due to the unavailability of specialized equipment and the significantly higher costs associated with its implementation. While plasma dicing presents notable advantages including reduced mechanical stress, improved die strength, and minimal chipping its application requires advanced machinery and infrastructure that are beyond the scope and resources of this study. Additionally, the high capital and operational expenditures associated with plasma dicing render it economically impractical for the current research objectives. As this investigation is centred on enhancing conventional dicing and wafer mounting techniques through practical and cost-effective means, the inclusion of plasma dicing is deemed unsuitable and has therefore been excluded from this study.

Figure 2.21 demonstrates the comparison between all singulation techniques available in the semiconductor industry. There were two techniques in summary, whether the wafer being singulate after back grinding as normal practice or before back grinding as advance technique. Dicing after grinding is the common technique used for singulation technique in semiconductor manufacturing. Although this conventional dicing method still results in excessive chipping and microcracks, it has undergone significant improvements over time through the optimization of diamond blade selection, cutting techniques, and dicing parameters.

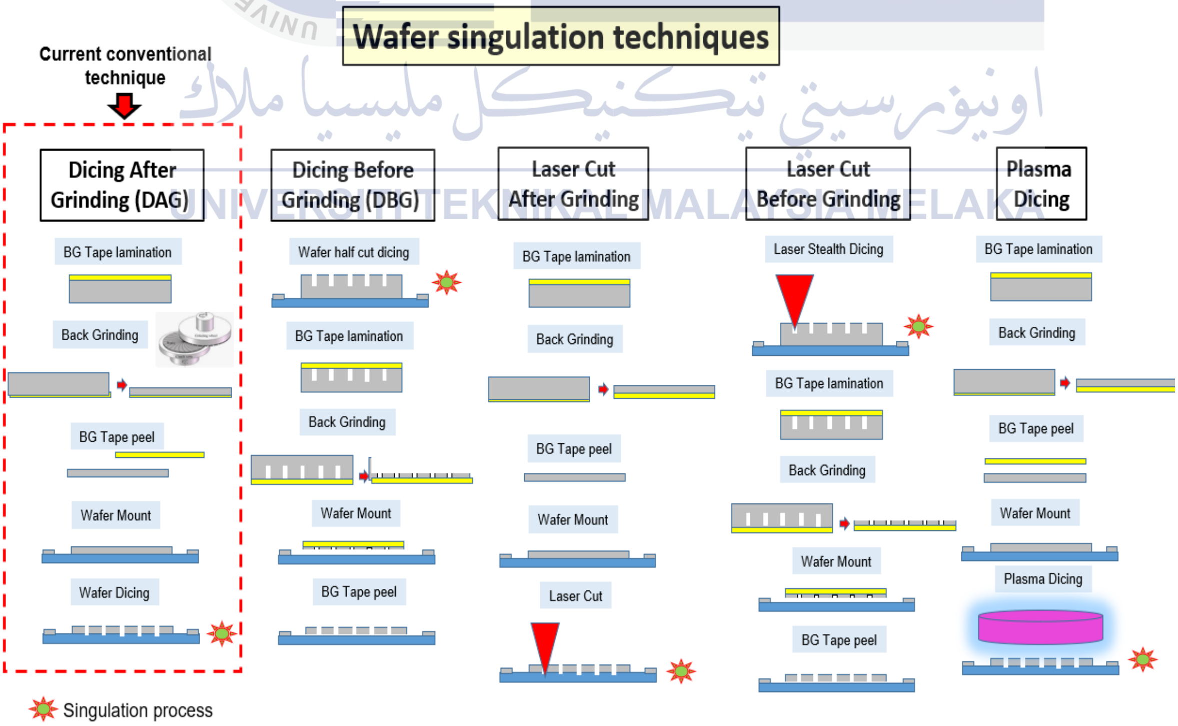


Figure 2.21: Wafer singulation techniques in the semiconductor manufacturing

Among the various singulation techniques, it was observed that all existing methods were based on the conventional single-sided wafer mounting technique, which has been extensively adopted over an extended period. However, the limitations of this approach necessitate the evaluation of double-sided wafer mounting techniques. Implementing and assessing the mounting configurations are crucial for enhancing wafer stability, minimizing chipping, and improving overall singulation performance.

2.4.6 Die strength analysis at wafer dicing process

Die strength is always related to the chipping performance after the wafer dicing process. High chipping is always related to lower die strength. This is because high chipping had caused some silicon area to be removed such as a big area causing the flexural and die strength to become lower. Jefferson Talledo (2021) conducted an in-depth crack die assessment utilizing the three-point bending test method, with the experimental procedure designed in accordance with SEMI G86-0303 standards for a die thickness of 180 µm.

The study demonstrated that the fracture strength of the wafer surface containing active circuitry was significantly lower compared to the die's backside. He further asserted that evaluating die strength exclusively from the backside could lead to an unrealistic representation of the die's mechanical robustness, thereby introducing potential inaccuracies in crack assessment. However, in the present evaluation, no active circuitry wafer is employed; thus, the die strength assessment can be conducted either on the wafer surface or the backside without compromising the reliability of the results.

Oscar (2009) discovered that excessive chipping particularly when it exceeds 90 µm from the die edge substantially reduces the fracture strength of silicon dies. This deterioration in mechanical integrity poses a serious risk to the overall reliability of semiconductor devices, potentially leading to failures during downstream processing or field operation. These findings underscore the critical importance of minimizing chipping defects to ensure die durability and performance.

Gourvest (2018) conducted an evaluation of die strength using the three-point bending test, with a specific focus on the mechanical impact of the wafer backgrinding process. His study revealed that grinding marks remaining on the wafer surface after backgrinding constitute the initial source of mechanical weakness within the die. Nonetheless, he identified edge chipping as the most prevalent cause of die failure, acting as the initiation point for crack propagation. This ultimately compromises the structural integrity and long-term reliability of the device. These observations highlight the necessity of optimizing backgrinding and dicing parameters to minimize physical defects and improve die strength in semiconductor manufacturing processes.

2.4.7 Vibration analysis during wafer dicing process

Vibration during the wafer dicing process is consistently associated with increased chipping occurrences. Elevated vibration levels lead to reduced wafer holding capability and mechanical instability, thereby exacerbating chipping behaviour and increasing the likelihood of crack formation within the dies. This mechanical instability compromises the integrity of the diced wafer, potentially resulting in latent failures during subsequent assembly or field application.

Au-Zou Tai identified that one of the primary sources of vibration originates from the instability of the dicing equipment's base (Tai and Fang, 2023). This instability contributes to the generation of internal stress within the wafer during the dicing operation.

Key factors influencing the machine's stability include high-speed spindle or blade rotation, blade selection, and the optimization of dicing parameters. Tai's study demonstrated that redesigning the dicing equipment base significantly mitigates vibration, thereby enhancing structural stability and improving overall dicing quality.

Kurniawan (2024) outlines that reverse engineering activities incorporate vibration analysis using three primary methods: impedance testing, impulse hammer testing, and vibrational amplitude measurement. However, the study made by him does not address the impact of chipping conditions on vibration analysis. Understanding chipping effects is crucial, as surface defects can influence vibrational response and structural integrity during assessment.

Xue Wang et al. (2021) mentioned vibration during wafer dicing poses a significant challenge when employing the conventional single-sided wafer mounting technique. In response to this issue, the proposed double-sided wafer mounting approach is anticipated to introduce a cushioning effect at the point of blade contact with the wafer surface, while simultaneously providing additional support to the wafer's backside, as illustrated in Figure 2.22. This dual-support mechanism is expected to enhance chipping resistance on both the topside and backside of the wafer, thereby addressing the limitations observed in the conventional mounting method.

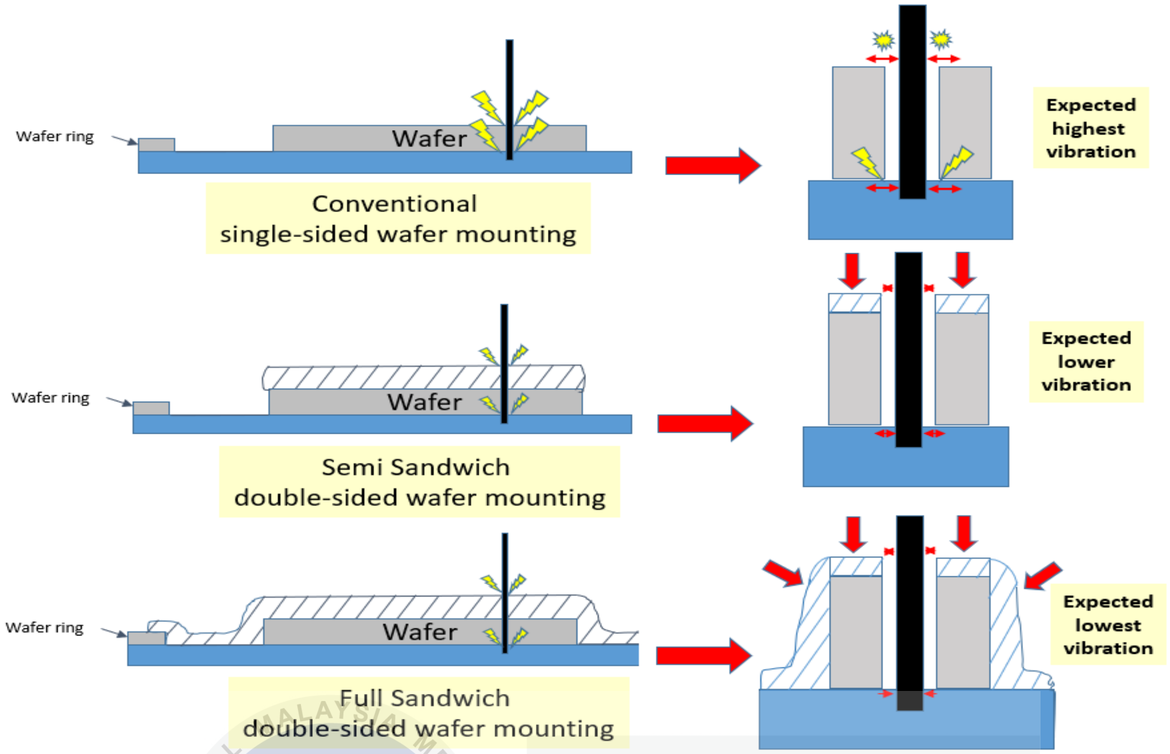


Figure 2.22: Illustration of cushioning effects on the wafer surface and extra gripping at the wafer backside for the wafer mounting techniques

The full-sandwich technique further extends this concept by encapsulating both the top and bottom surfaces of the wafer in a protective medium, thereby creating a symmetric cushioning and gripping system. This full encapsulation is expected to offer the highest level of vibration dampening, as the dicing blade interacts with a more stabilized structure. The primary aim of these comparative investigations is to assess the degree of chipping reduction and die flexural strength improvement achievable through double-sided mounting configurations. To achieve this, a combination of vibration analysis and mechanical die strength testing was conducted across all three mounting techniques. The subsequent sections of this chapter detail the experimental setup, materials used, procedures followed, and data analysis methods employed to evaluate the efficacy of each technique.

2.4.8 Research gap

Among the various singulation techniques, it can be observed that during the singulation process, the wafer mounting tape is secured solely at the backside of the wafer. Table 2.3 summarizes the research gaps identified during the compilation process and outlines potential methods for evaluating improvements.

Table 2.3: Summary of the research gap from the singulation process and idea for improvement

	Dicing After Grinding (DAG)	Dicing Before Grinding (DBG)	Laser Cut After Grinding	Laser Cut Before Grinding	Plasma Dicing	Proposal: Novel Sandwich mounting for Dicing After Grinding (DAG)
Wafer Mounting	Single-sided mounting tape	Single-sided mounting tape + Backgrinding tape	Single-sided mounting tape	Single-sided mounting tape + Backgrinding tape	Single-sided mounting tape	Double-sided mounting tape
Wafer Dicing	Single-sided mounting tape	Single-sided mounting tape	Single-sided mounting tape	Single-sided mounting tape	Single-sided mounting tape	Double-sided mounting tape

Research gap   Novelty

From the identified research gap, it was observed that all existing processes rely exclusively on the conventional single-sided wafer mounting technique. To further identify the limitations within current wafer dicing practices, a detailed analysis was conducted to identify the missing process steps required for the implementation of double-sided wafer mounting techniques. These gaps were systematically mapped across various wafer singulation methods and presented in Table 2.4. This comparative analysis is intended to provide a comprehensive understanding of the procedural deficiencies associated with single-sided mounting and to highlight the specific steps necessary for transitioning to a double-sided mounting approach for process enhancement.

Table 2.4: Process gap for each conventional wafer singulation technique

Techniques	Backgrinding process	Wafer mounting process at wafer backside	Wafer mounting process at wafer surface	Wafer Dicing Process without surface mounting tape	Wafer Dicing Process with surface mounting tape	Surface mounting removal after wafer dicing by cleaning process
Dicing After Grinding (DAG)	✓	✓	✗	✓	✗	✗
Dicing Before Grinding (DBG)	✓	✓	✗	✓	✗	✗
Laser Cut After Grinding	✓	✓	✗	✓	✗	✗

Laser Cut Before Grinding	✓	✓	✗	✓	✗	✗
Plasma Dicing	✓	✓	✗	✓	✗	✗

The double-sided sandwich wafer mounting technique is anticipated to provide secure wafer gripping during the dicing process, thereby reducing vibration and enhancing both chipping resistance and die strength. It identifies several research gaps in the current methods employed for the wafer mounting and dicing process, specifically across techniques such as Dicing After Grinding (DAG), Dicing Before Grinding (DBG), Laser Cut After Grinding, Laser Cut Before Grinding, and Plasma Dicing. A significant research gap is observed in the universal use of single-sided mounting tape for the wafer mounting and dicing process.

The novelty towards the process is to implement a mounting tape on the wafer surface during mounting and remain during wafer dicing to provide extra gripping during dicing and provide higher stability, with the expectation to have lower vibration and improve the chipping and crack performance. This study highlights that at this stage, no wafer dicing process was performed with mounting tape on the wafer surface for chipping improvement activities. The only tape used previously was the laminate tape during the wafer grinding process. It was used to eliminate the scratch issue during its operation; however, the grinding tape was peeled off before the wafer dicing process (Dong et al., 2021).

A similar conceptual approach was applied during the wafer mounting process, wherein UV tape was applied directly to the wafer surface; however, unlike conventional methods, the surface mounting tape was intentionally retained during the wafer dicing stage. This strategy not only protects the wafer surface from potential scratch-induced defects but also serves a dual function by providing a cushioning effect and stabilizing the wafer during the dicing process. The added mechanical support from the surface tape helps to suppress excessive vibration and mechanical stress, thereby contributing to improved chipping performance and overall die reliability performance.

Figure 2.21 summarizes the overall project through each of the processes involved in these activities. The theoretical aspect, research gap and the novelty of the project will be identified towards evaluating the double-sided wafer mounting technique. The project starts with the backgrinding process with 3 types of backgrinding methods. The first backgrinding method using Z1 and Z2, with no polishing that produced a wafer backside with grinding marks and the highest wafer roughness. To remove the backgrinding marks on the wafer back the application of poligrind and polishing can be conducted.

However, to subject the wafer to the highest stress and worst conditions, the backgrinding process was conducted using the coarse grinding method, which results in the formation of pronounced backgrinding marks on the wafer's backside. These grinding marks introduce surface irregularities, leading to non-uniform stress distribution across the wafer. Furthermore, this condition presents a significant challenge for the subsequent wafer mounting process, as the uneven wafer surface may compromise the adhesion and gripping performance of the mounting tape. The presence of uneven grinding marks can reduce the overall stability of the wafer during dicing, potentially increasing the risk of chipping and crack propagation. Therefore, optimizing the wafer mounting process to accommodate the surface roughness introduced by coarse grinding is critical in ensuring minimal defects and maintaining die integrity throughout evaluation activities. Once chipping is successfully mitigated through this optimization, the improved mounting approach may be applicable across various wafer singulation methods, thereby enhancing overall process versatility and reliability.

Next is the wafer mounting process. In wafer mounting, the conventional process was based on a single-sided wafer mounting technique. The common improvement activities in wafer mounting are the usage of UV and non-UV mounting tapes. The UV mounting tape normally has higher adhesion compared to the non-UV tape however, UV tape requires a UV curing process to reduce the tape adhesion for areas at the wafer backside for easy pick up during the die attach process. The higher the adhesion value on the specification, the stronger the adhesion strength between the mounting tape and the wafer contact area. Mounting tapes with higher adhesion properties ensures more stable and secure fixation of the wafer or individual dies, which is essential for maintaining mechanical stability during the dicing process (Yu Zhang et al., 2024).

While higher adhesion levels generally correlate with improved chipping performance, lower adhesion ultraviolet (UV) mounting tapes were also evaluated to assess their suitability in surface peeling tests and their impact on chipping behavior. This evaluation is particularly relevant in the context of double-sided wafer mounting applications, where mounting tapes are simultaneously applied to both the wafer surface and backside during process improvement activities. In the case of surface-applied UV tapes, the UV curing process necessitates precise parameter optimization to ensure that the cured tape can be effectively removed during the post-dicing wafer cleaning stage without compromising die quality or structural integrity.

Next is the wafer dicing process, which has five methods for the singulation process involving dicing after grinding, dicing before grinding, laser cut after grinding, laser cut before grinding, and plasma. However, the team has decided to select the standard dicing after grinding for the singulation method by fixing the dicing parameter and the dicing blade for all the improvement activities. The only difference in the wafer dicing process is adding vibration analysis for the single and double-sided wafer mounting techniques during the singulation process. Once the chipping measurement had been completed for both mounting techniques then the 3-point bending test was conducted to correlate the flexural strength towards the chipping performance.

To summarize the theoretical aspects derived from the overall activities illustrated in Figure 2.23, the conventional single-sided wafer mounting technique provides support exclusively from the wafer's backside, resulting in limited wafer gripping during the dicing process. With the low gripping on the existing conventional single-sided wafer mounting technique, it generates higher chipping during wafer dicing and at the same time develops low die strength performance during the 3-point bending test. The single-sided wafer mounting technique also generates higher vibration during dicing in theory due to insufficient support from the conventional method.

A research gap had been identified, which the conventional mounting method always in single-sided technique in the manufacturing line. Towards this situation, the novelty of this project is to evaluate the double-sided wafer mounting technique, which the technique haven't been explored by researchers to understand whether it can improve the chipping performance. In theory, the double-sided wafer mounting provides a cushioning effect on the wafer surface during cutting, which may improve the topside chipping. The surface mounting tape may increase the gripping since it is holding from the top to the back, which manages to hold the wafer firmly and improve the backside chipping as well.

The second research gap identified pertains to the current lack of flexural strength testing conducted on double-sided wafer mounting applications. At present, no empirical data is available to evaluate the mechanical integrity of dies subjected to this alternative mounting configuration. To address this gap, it is necessary to perform comprehensive flexural strength assessments on both semi-sandwich and full-sandwich double-sided wafer mounting techniques. Such testing will enable a comparative analysis to determine whether the implementation of these methods leads to an improvement or degradation in die strength, thereby providing valuable insight into their suitability for advanced singulation processes.

The final research gap identified is the absence of vibration analysis comparing the performance of single-sided and double-sided wafer mounting techniques during the wafer dicing process. Understanding this relationship is crucial, as vibration levels are known to directly influence chipping behavior, which in turn affects die quality and yield. To address this gap, a vibration analysis was conducted to evaluate and compare the dynamic responses of both mounting techniques during dicing. This analysis aimed to establish a correlation between vibration magnitude and chipping severity, thereby providing a deeper understanding of how mounting configurations impact wafer singulation outcomes.

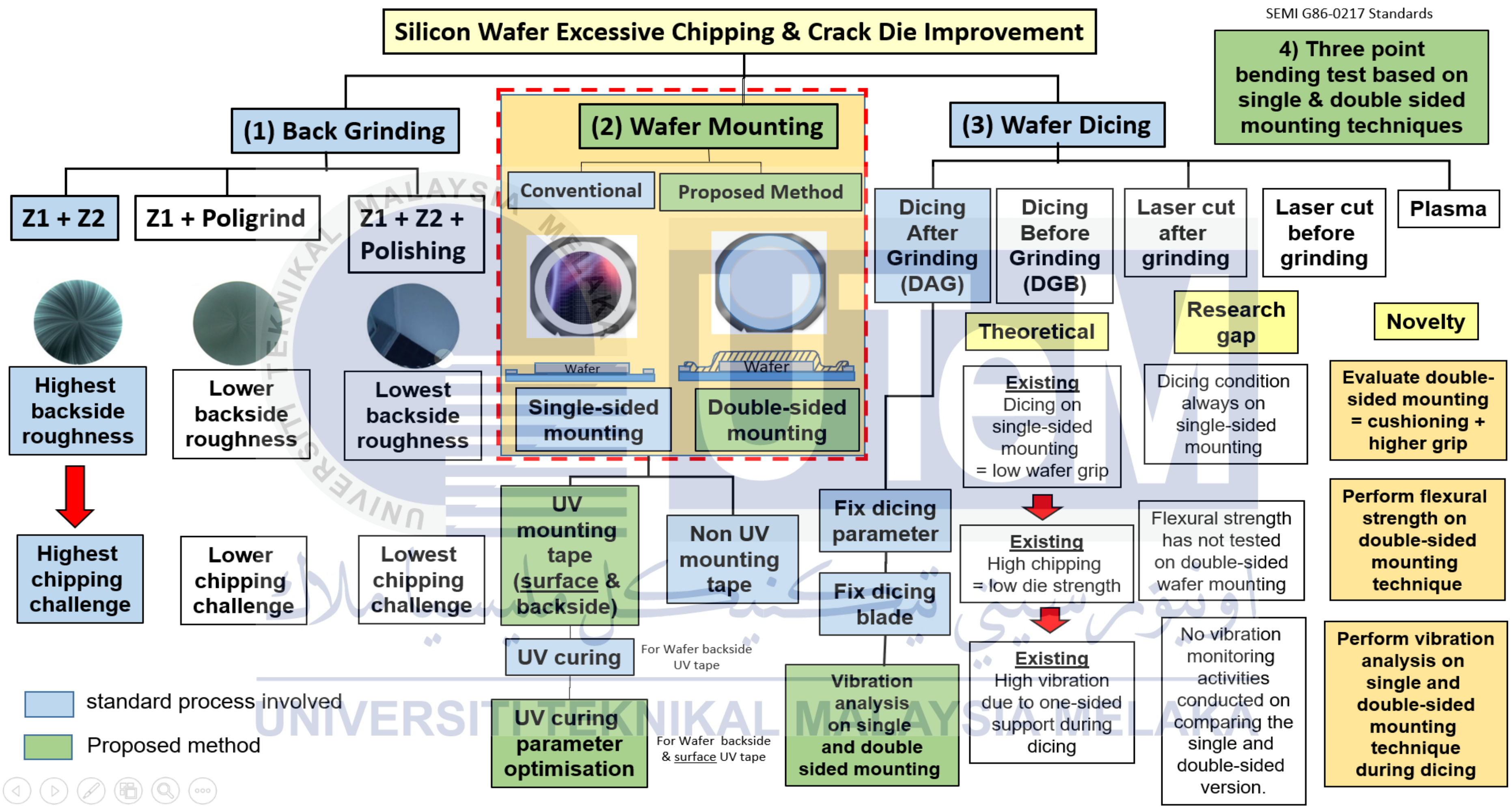


Figure 2.23: Summary of research gap and novelty on the overall project

Table 2.5 presents a comprehensive comparison of the advantages and disadvantages of conventional backgrinding, wafer mounting, and wafer dicing processes, providing a deeper understanding of the overall front-end semiconductor manufacturing process. Among these three processes, wafer mounting stands out as the most cost-effective solution for chipping improvement activities. This is primarily due to its direct role in stabilizing the wafer during the dicing process, which significantly reduces the likelihood of chipping.

Additionally, wafer mounting is favoured for its simplicity, lower equipment costs, and minimal material expenses. The process involves the application of adhesive tapes, such as UV or non-UV tapes, to provide mechanical support and stability during subsequent processing steps. The equipment required for wafer mounting is relatively inexpensive when compared to the high-precision machinery necessary for backgrinding and wafer dicing. Moreover, the consumables, particularly mounting tapes, are cost-effective and readily available, making wafer mounting both an economical and practical choice in semiconductor manufacturing.

In the implementation of the double-sided wafer mounting technique utilizing the single-cut dicing method, the primary target is to achieve a minimum of 50% improvement in both topside and backside chipping performance when compared to the conventional single-sided wafer mounting technique. The rationale behind this target is grounded in the hypothesis that significant chipping reduction will directly contribute to improved mechanical integrity of the diced dies, particularly in terms of flexural strength. Enhanced flexural strength not only indicates superior die robustness but also translates into better resistance to mechanical stress during downstream assembly and packaging processes. Furthermore, by reducing the extent of wafer chipping, the likelihood of defect propagation and die fracture is minimized, thereby leading to increased product reliability and overall manufacturing yield.

Table 2.5: The advantages and disadvantages for the conventional backgrinding, wafer mounting and wafer dicing process.

Process	Advantages	Disadvantage
1) Backgrinding Backgrinding is used to grind the wafer until the desired thickness, making it suitable for packaging. However, it can create micro-cracks on the wafer's backside, contributing to chipping occurrence.	• Thinning the wafer allows for more flexible according to device packaging and better thermal performance. • Backgrinding with optimized parameters, such as reduced grinding force and the use of finer grit sizes, can minimize surface damage and reduce the risk of chipping. • Post-backgrinding treatments like chemical mechanical polishing (CMP) can help smooth the wafer surface and reduce micro-crack formation.	• Aggressive grinding can still lead to significant surface damage, increasing the risk of chipping during dicing. • Additional backgrinding treatments (e.g., CMP) can increase processing time and cost. • Back grinding involves precise mechanical grinding of the wafer's backside to reduce thickness, requiring specialized equipment, consumables (grinding wheels, slurries), and skilled operation. This makes it more expensive.

		• Backgrinding utilizes consumables like grinding wheels and cleaning solutions, which add to operational costs. • Back grinding machines are costly to purchase, maintain, and operate due to their high precision parts. • **Cost:** High.
2) Wafer mounting Wafer mounting involves attaching the wafer to a tape for support during the wafer dicing process. The quality of wafer mounting significantly affects wafer stability and chipping.	• Wafer mounting primarily uses adhesive tapes, which are inexpensive and available in various types (UV or Non-UV). • Wafer mounting equipment, such as tape applicators, is more affordable and requires less frequent maintenance.	• Advanced wafer mounting techniques, like double-sided mounting, may require specialized tapes and equipment, leading to higher material and tooling costs. • Improper tape adhesion or mounting techniques can cause wafer slippage or

	• Techniques such as UV-curable mounting tapes offer easy removal without damaging the wafer, helping maintain die quality. • **Cost:** Low.	detachment during dicing, leading to increased chipping or wafer breakage. • Some mounting tapes may leave residues that need to be cleaned, adding extra processing steps.
3) Wafer dicing Wafer dicing involves cutting the wafer into individual dies. The dicing process can generate stress and vibrations that contribute to chipping. Chipping has always been measured after the wafer dicing process even if the improvement was executed at	• Optimizing dicing parameters (e.g., blade speed, feed rate) can minimize mechanical stress and reduce chipping. • Using advanced dicing techniques, such as laser dicing or plasma dicing, can achieve cleaner cuts with chipping improvement. • Implementation of vibration-damping systems (Tai and Fang, 2023) and improved cooling	• Advanced dicing techniques (e.g., plasma and laser dicing) require specialized equipment, increasing capital investment and maintenance costs (Zhang et al., 2021). • Fine-tuning dicing parameters can be challenging, especially with variations in wafer thickness, material properties, or mounting

back grinding, wafer mounting or wafer dicing itself.	methods during dicing can further reduce the likelihood of chipping.	methods and require lots of wafer samples which increase the cost. • Wafer dicing involves using advanced dicing saws, blades, and optimized parameters (e.g., spindle speed, cut depth). Equipment and consumables are costly, and frequent blade replacements add to expenses. Additionally, using an automatic blade changer feature to eliminate blade damage during blade changing results to high equipment cost. • **Cost:** Moderate to High.

2.5 Summary

Towards wafer mounting and dicing processes, there is currently no technique employing a double-sided wafer mounting method, which involves adding mounting tape on the wafer surface to provide cushioning and hold the wafer firmly during the dicing process. The current single-sided wafer mounting process has been widely used in wafer dicing applications for decades, but has demonstrated significant drawbacks, including high backside chipping and crack formation. These issues are primarily attributed to uneven support and increased vibration during the dicing process, leading to mechanical stress that propagates from the backside of the wafer to its surface. Excessive chipping during wafer dicing affects the die strength, which will impact the overall yield and reliability of semiconductor components.

The conventional single-sided wafer mounting technique has been consistently identified as inadequate in mitigating vibration-related issues during the wafer dicing process, particularly for wafers exhibiting backgrind marks. These backgrinding marks contribute to surface unevenness and increased roughness, leading to mechanical instability during dicing. As a result, elevated vibration levels are induced, which in turn exacerbate chipping and crack formation along the wafer edges and die corners. Given that improvements in the wafer mounting process generally involve relatively low implementation costs, the potential return on investment is considered favourable, thereby justifying further evaluation and optimization of alternative mounting approaches.

CHAPTER 3

RESEARCH METHODOLOGY

3.1 Overview

This chapter presents the methodologies implemented in the development of a double-sided wafer mounting technique, designed to reduce silicon die chipping and enhance die strength. The objective of this research activity is to evaluate the performance of the proposed double-sided mounting approaches in comparison to the conventional single-sided mounting method, which has been widely adopted for over a decade, as illustrated in Figure 3.1. The mounting technique aims to optimize wafer handling during the dicing process, thereby improving chipping resistance. To gain a comprehensive understanding of the mechanical integrity imparted by each mounting approach, vibration analysis was conducted to assess their respective impacts on chipping behavior and flexural strength.

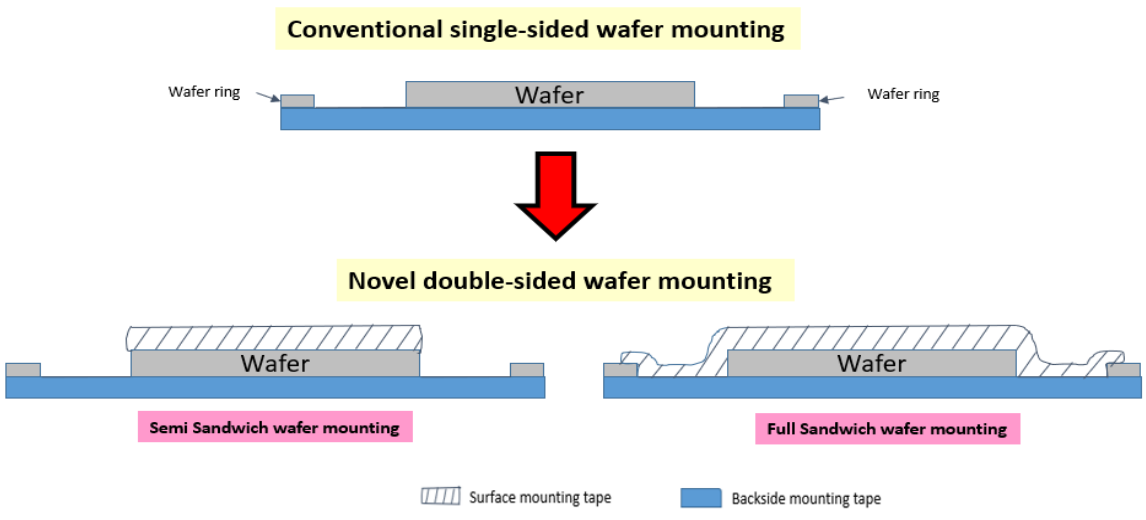


Figure 3.1: Double-sided wafer mounting techniques

The conventional single-sided wafer mounting technique, which has been the industry standard for over a decade, supports the wafer only on its backside using a mounting tape attached to a dicing frame. This configuration often results in insufficient cushioning and gripping during blade contact, leading to increased vibration transmission and, consequently, higher chipping risk, particularly at the surface and wafer's backside.

To address this limitation, two wafer mounting configurations were developed: the semi-sandwich and full-sandwich double-sided wafer mounting techniques. The semi-sandwich approach introduces an upper protective layer, partially covering the topside of the wafer, while maintaining the conventional adhesive film underneath. This arrangement is hypothesized to provide moderate vibration suppression by distributing the mechanical load more evenly during dicing.

3.2 Flow Chart of the Research

The flowchart in Figure 3.2 depicts the overall picture of the research works based on the activities involved in order to achieve all the defined objectives. The research work has been divided into three major stages, which consist of:

Stage 1: Evaluating semi and full sandwich wafer mounting techniques

Stage 2: Monitoring die flexural strength vs each wafer mounting technique

Stage 3: Analyzing of chipping and flexural strength performance using vibration analysis

(a) Stage 1: Evaluating semi and full sandwich wafer mounting techniques

In the development of the wafer mounting techniques, the overall process stages can be categorized into the 4M (Man, Machine, Material, and Method) methodology as follows:

1. Man (Researchers and Expertise)

- Brainstorming on double-sided wafer mounting techniques implementation on wafer mounting machine
- Identification of the surface peeling test method with the highest peeling yield performance.
- Identification of UV curing parameters for all the UV mounting tape removal process
- Execution of chipping and crack monitoring by trained personnel to assess defect trends.

2. Machine (Equipment and Tools)

- Setting up the wafer mounting machine to evaluate wafer mounting techniques.
- Optimization of the UV curing parameter for surface peeling removal during the wafer cleaning process.
- Identify the jig design and optimum test speed according to the SEMI G86-0217 standards for the best die flexural strength performance.
- Vibration analysis setup on wafer dicing machine for achieving the optimum vibration data on all wafer mounting techniques.

3. Material (Consumables and Components)

- Determination of the mounting tape selection to ensure proper adhesion and stress absorption.

4. Method (Processes and Techniques)

- Identify the double-sided wafer mounting techniques for the new setup according to semi and full sandwich wafer mounting approaches.

- Identifying surface topography vs. chipping performance to establish a correlation between wafer mounting and defect rates.
- Performing statistical analysis to define the best wafer mounting technique based on experimental data.

This structured 4M approach ensures a systematic evaluation and optimization of the wafer mounting process to achieve minimal chipping after the wafer dicing process.

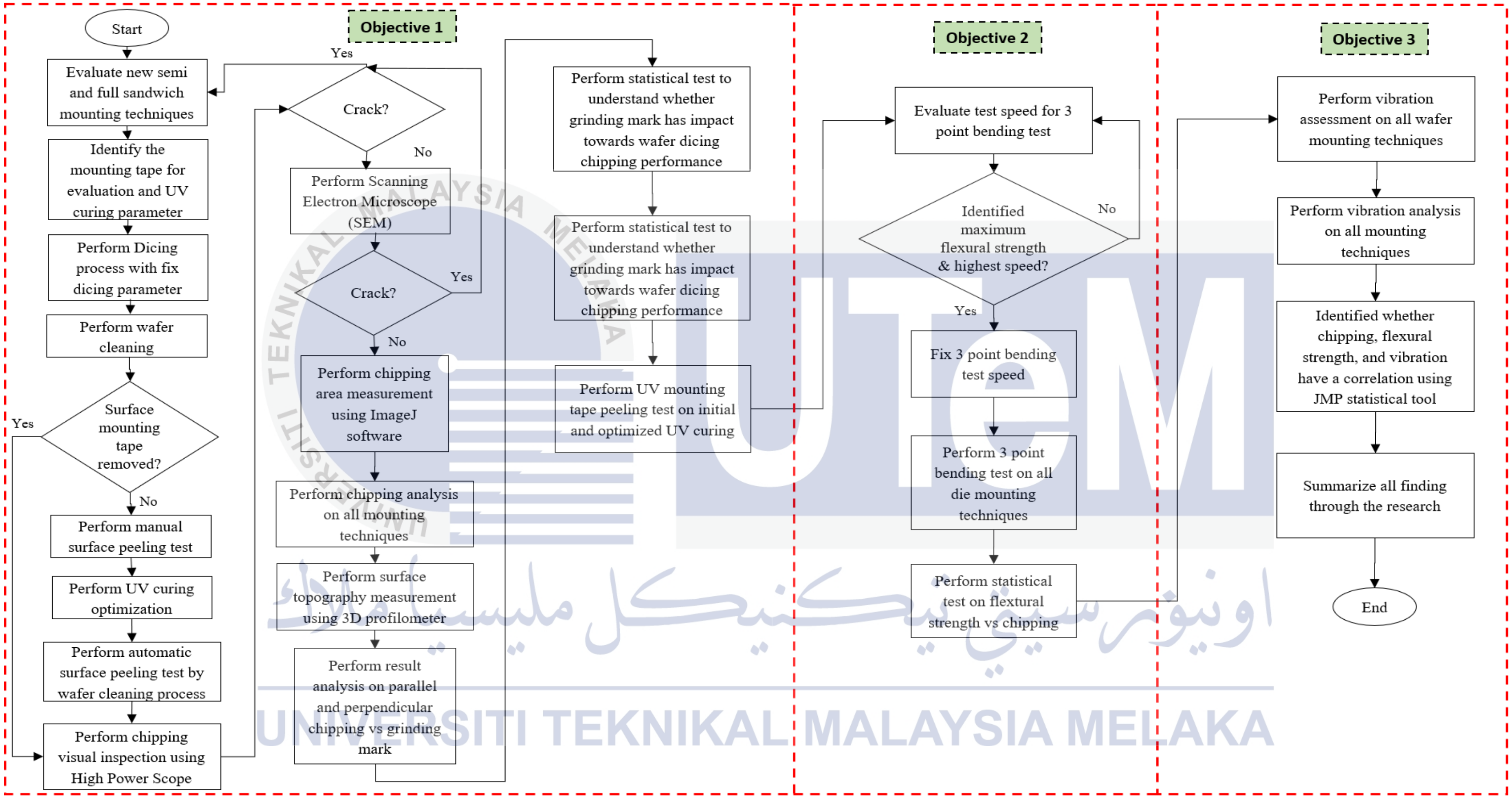


Figure 3.2: Flow chart on research activities

(b) Stage 2: Monitoring die flexural strength vs each wafer mounting technique

Stage 2 involved the monitoring of the die flexural strength performance based on chipping results from each wafer mounting technique and performing statistical tests to find the correlation between chipping and flexural strength performance. The jig had been fabricated and verified through the design made earlier according to SEMI G86-0217 standards.

(c) Stage 3: Verification of chipping and flexural strength performance using vibration analysis

The third stage of this investigation includes vibration analysis of each mounting approach to verify the performance of both double-sided and conventional single-sided wafer mounting procedures. The vibration findings were then summarised to better understand the relationship with the wafer mounting techniques that resulted in the lowest chipping and the maximum flexural strength performance.

3.3 Research materials

This section outlines the materials employed throughout the research activities. All materials were provided by semiconductor manufacturing companies and are representative of those used in actual production environments.

3.3.1 Wafer

The research activities involved non-circuitry silicon wafers, commonly referred to as mirror wafers supplied by STMicroelectronics, Muar which can be referred to in Figure 3.3. The non-circuitry silicon wafers were used to represent the usage of silicon wafers used by semiconductor manufacturing practices and the limitations imposed by the semiconductor company to protect the integrity of the design architecture from the public view. This is achieved by putting constraints on the provision of production circuitry wafers which cause the limitation for the industries to provide the circuitry wafers for experimenting purposes. However, the non-circuitry silicon wafers provided by the semiconductor manufacturer were made from the same substance as the production wafers, which made them appropriate for reference purposes. The silicon wafers for the research utilized an 8-inch wafer size with a 300 μm wafer thickness.

Figure 3.3: Mirror wafer

3.3.2 Mounting tape

The investigation conducted in this research involves the evaluation of two categories of industrial-grade mounting tapes: Ultraviolet (UV) and non-UV mounting tapes. All tape materials used in this study were supplied by Lintec Advanced Technologies (M) Sdn Bhd, a leading provider of semiconductor mounting tape materials and equipment. The research specifically focused on assessing several types of UV mounting tapes for their suitability in developing both semi-sandwich and full sandwich wafer mounting techniques. The primary objective was to analyze and compare the chipping performance of these UV tapes against a standard non-UV tape, which serves as the baseline reference typically used in conventional manufacturing for wafers with a thickness of 300 µm.

The specification details of all the tapes used in this study are clearly outlined in Table 3.1 to facilitate technical comparison. Among the UV mounting tapes evaluated, two variants, UV Tape A and UV Tape B, were selected based on their different adhesion strengths to examine how adhesion properties affect wafer stability and chipping behaviour during dicing. In contrast, the non-UV tape used in this research represents the industry's current standard mounting approach. This comparative analysis provides a foundation for identifying improved tape performance that may contribute to reducing wafer chipping and enhancing die reliability.

Table 3.1: Evaluated mounting tape specifications

Info		**UV Tape A**	**UV Tape B**	**Non-UV Tape**
Overall Mounting Tape Thickness (µm)		85	85	80
Base film thickness (µm)		80	80	70
Adhesive layers thickness (µm)		5	5	10
Mounting Tape base material		Polyolefin	Polyolefin	Polyvinylchloride
Adhesion (mN/25mm)	Before UV	4900	3100	940
	After UV	80	30	

Table 3.1 compares the properties of three types of mounting tapes: UV Tape A, UV Tape B, and Non-UV Tape. All three tapes have similar overall thicknesses, with UV Tape A and B at 85 µm and Non-UV Tape at 80 µm. The base film thickness is 80 µm for both

UV tapes and 70 µm for the Non-UV Tape, while the adhesive layers are thinner in the UV tapes (5 µm each) compared to the Non-UV Tape (10 µm). The base materials also differ, with the UV tapes using polyolefin and the Non-UV Tape using polyvinylchloride. Adhesion strength before UV exposure is highest for UV Tape A (4900 mN/25mm), followed by UV Tape B (3100 mN/25mm), and significantly lower for the Non-UV Tape (940 mN/25mm).

UV Tape A and B are designed for applications where strong initial adhesion is required, but the bond must be easily removable after UV exposure. Their polyolefin base material and thin adhesive layers (5 µm) contribute to their high initial adhesion (4900 mN/25mm for Tape A and 3100 mN/25mm for Tape B), which drops significantly after UV exposure (to 80 mN/25mm and 30 mN/25mm, respectively). This makes them suitable for temporary bonding in processes like semiconductor or display manufacturing, where surface wafer mounting detachment is needed.

The Non-UV Tape, with its polyvinylchloride base and thicker adhesive layer (10 µm), provides lower but more stable adhesion (940 mN/25mm) and lacks UV responsiveness. This makes it suitable for permanent or long-term bonding where UV-triggered release is unnecessary. Its thinner overall profile (80 µm) could be advantageous in space-constrained applications. The choice between these tapes depends on the need for UV debonding capability versus consistent adhesion performance.

In the initial phase of the study, UV Tape A was used for all evaluation activities. However, due to unsatisfactory outcomes observed during the preliminary surface peeling tests, UV Tape B was subsequently introduced by the industry for further investigation. Both UV Tape A and UV Tape B were systematically assessed to enhance chipping resistance and flexural strength performance and were benchmarked against the conventional single-sided mounting approach through the evaluation of the semi- and full-sandwich double-sided mounting techniques. Importantly, the diced wafers were also required to pass the newly developed surface peeling test to validate the feasibility of the double-sided mounting method within the research framework. The surface mounting tapes were critically evaluated for their ability to securely hold the wafer in place and absorb vibrations during the dicing process, which was anticipated to result in improved chipping and flexural strength characteristics.

3.3.3 Dicing blade

Disco Hi-Tec (Malaysia) Sdn. Bhd. supplied the diamond dicing blades utilized in the research activities. To ensure consistency and eliminate variability, identical dicing blades were employed across all wafer mounting techniques evaluated in this study. The specific diamond blade used during the dicing process is illustrated in Figure 3.4.

Figure 3.4: Diamond dicing blade

The ZH05 blade series is engineered to minimize the number of precut passes required during the dicing process while maintaining high operational stability. This design enhancement significantly reduces the likelihood of blade breakage, which is often induced by the impact of dislodged dies during high-speed rotation. The SD4000 designation corresponds to a #4000 grit size, combined with the N1 which refer to the bond type. The numeral '50' indicates a lower diamond concentration within the blade matrix, whereas the 'BB' specification refers to the blade exposure length ranging from 0.51 mm to 0.64 mm. The kerf width of the blade is specified as 22.5 ± 2.5 µm, which refers to the width of the cutting line generated following the dicing process. Further information regarding the blade coding specifications is available in the DISCO catalogue, as illustrated in Figure 3.5.

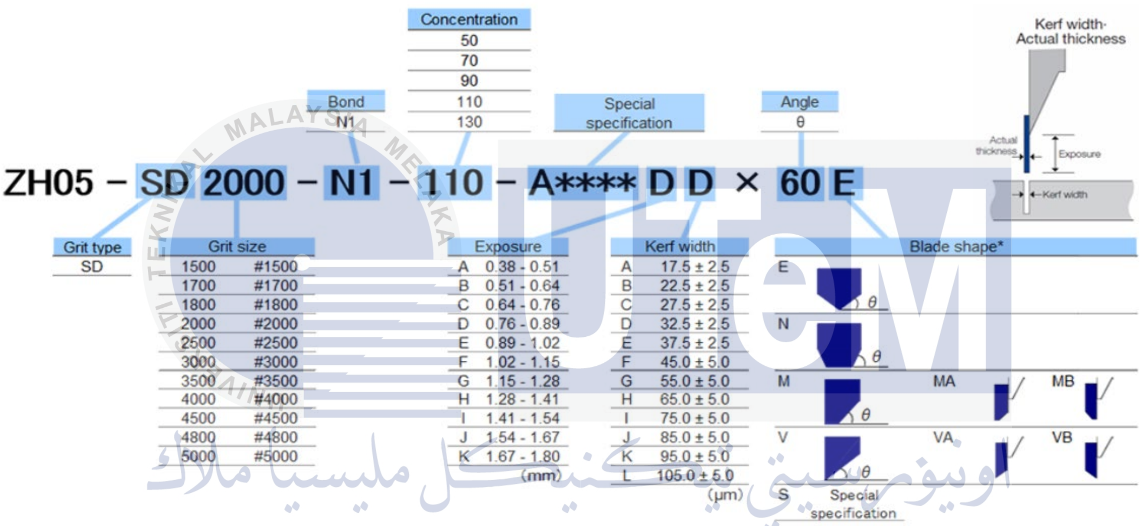


Figure 3.5: Disco blade specification code

3.4 Samples preparation

At this stage, all the samples were utilized in the semiconductor manufacturing process flow, specifically in the pre-assembly process. This process included wafer back grinding, wafer mounting, wafer dicing, UV curing and the new surface mounting tape peeling process. This section provides a detailed explanation of how the samples were prepared during the research.

3.4.1 Wafer back grinding

In this study, 8-inch mirror wafers were employed and subsequently subjected to a back-grinding process utilizing STMicroelectronics' proprietary backgrinding system within a cleanroom manufacturing environment. To ensure consistency and reliability across all samples, equipment parameters were standardized throughout the entire backgrinding operation. The backgrinding procedure commenced with a Z1 coarse grinding step using a 360-grit wheel, followed by a Z2 fine grinding stage employing a 2000-grit wheel. As no polishing step was incorporated post-grinding, the wafer surfaces retained visible grinding marks, indicative of mechanical abrasion, as shown in Figure 3.6. The process was fixed to a final thickness of 300 µm throughout for all wafer samples.

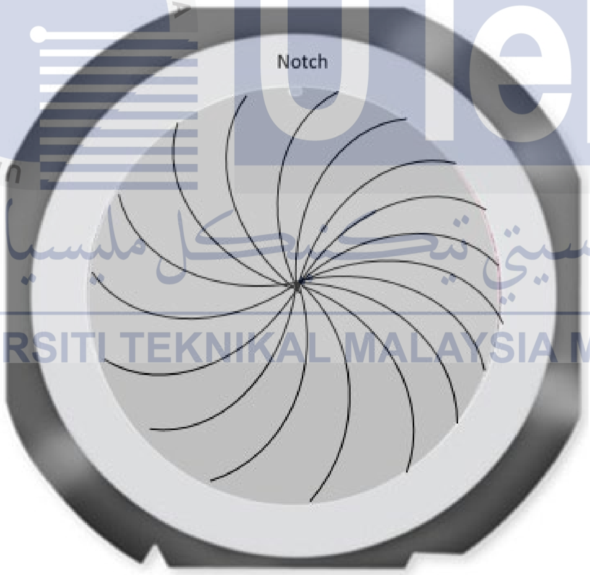


Figure 3.6: Grinding marks at wafer back surface

Given that the back-grinding process introduces initial stress on the silicon wafer (H. Liu et al., 2022), it was determined that the wafer's backside would remain unpolished to preserve the most critical condition for the subsequent dicing process. This decision was primarily motivated by the observed non-uniformity of the grinding marks on the wafer’s rear surface. Such non-uniformity results in inconsistent adhesion of the mounting tape, particularly in areas with pronounced grinding marks, which in turn weakens the bond between the mounting tape and the wafer (Chang and Ler, 2022).

This compromised adhesion presents significant challenges during the manufacturing process, exacerbating difficulties encountered in wafer handling. The unevenness of the wafer's backside is a critical factor influencing the overall stability of the silicon wafer during dicing. Moreover, this unevenness can have a direct impact on the chipping performance, necessitating careful optimization of the wafer mounting process. Proper optimization is essential to secure the wafer firmly, thereby reducing the likelihood of chipping and enhancing die strength (Sekhar et al., 2020).

3.5 Wafer mounting

Wafer mounting constitutes a critical process step within the scope of this experimental study, serving as the primary focus of the improvement activities undertaken. The research predominantly focused on optimizing the wafer mounting process using the Lintec RAD-2500 wafer mounter, as illustrated in Figure 3.7. The effects of the mounting process were subsequently evaluated following wafer dicing, wherein a fixed set of dicing parameters was maintained to ensure consistency in comparative analysis.

To facilitate a comprehensive evaluation of silicon wafer behaviour, both ultraviolet (UV) and non-UV mounting tapes were employed across each of the proposed wafer mounting techniques. Before the commencement of the experimental runs, the Lintec RAD-2500 wafer mounter was subjected to a thorough calibration procedure to ensure optimal operating conditions. The calibration details are documented in Appendix B. In alignment with the research objective of minimizing silicon die chipping, the conventional mounting method was implemented using UV mounting tape. This decision was informed by prior findings indicating that UV tapes exhibit stronger adhesion properties, thereby contributing to significantly reduced chipping rates when compared to non-UV tapes (Khairul et al., 2022b). Additionally, to eliminate extraneous sources of variation and ensure consistency across experiments, the wafer mounter was meticulously levelled, cleaned, and calibrated prior to each evaluation. Furthermore, the wafer mounting orientation was standardized for all mounting techniques, thereby reducing process variability and enhancing the reliability of comparative results.

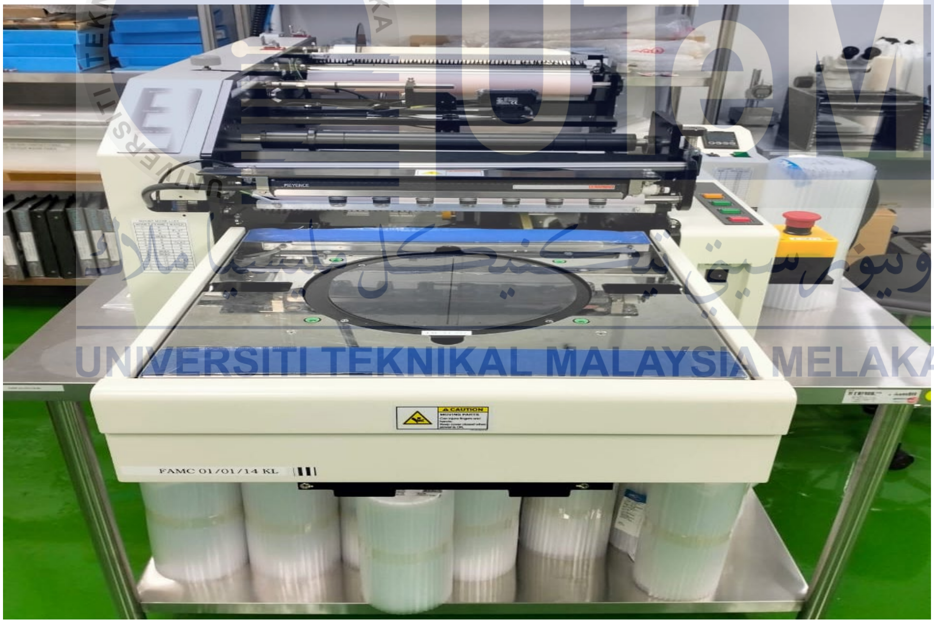


Figure 3.7: Lintec RAD-2500 wafer mounter machine

Figure 3.8 presents a detailed comparison of the wafer mounting techniques employed throughout the research activities. It is evident that the process flows associated with the double-sided semi-sandwich and full-sandwich wafer mounting techniques are more extensive than those of the conventional single-sided wafer mounting method. This increased complexity is attributed to the additional mounting steps required on both sides of the wafer surface. The purpose of placing wafer mounting tape on the surface of the wafer for the semi-sandwich wafer mounting technique is to provide a cushioning effect for the wafer dicing process, which induces high vibration caused by the high blade rotation per minute (RPM) during the cutting process. This cushioning is intended to mitigate mechanical stress and potential chipping during the cutting operation.

For the full-sandwich wafer mounting technique, the surface mounting tape was further extended to cover the wafer ring area. This extension was implemented to investigate the combined effects of enhanced cushioning and improved gripping, both of which are hypothesized to contribute to greater wafer stability during the dicing process. The selection of mounting tape is crucial, especially for the tape used for surface application which must be easily peeled off during the wafer cleaning process or the surface peeling test and chipping monitoring as well. This study examined the use of non-UV tape and two different types of UV tape in double-sided mounting processes. A UV tape was used in conventional mounting as a benchmark for comparison and standardization. However, the non-UV tape was assessed towards the double-sided wafer mounting techniques to see the effectiveness and compare with the UV mounting tape performance in the initial phase.

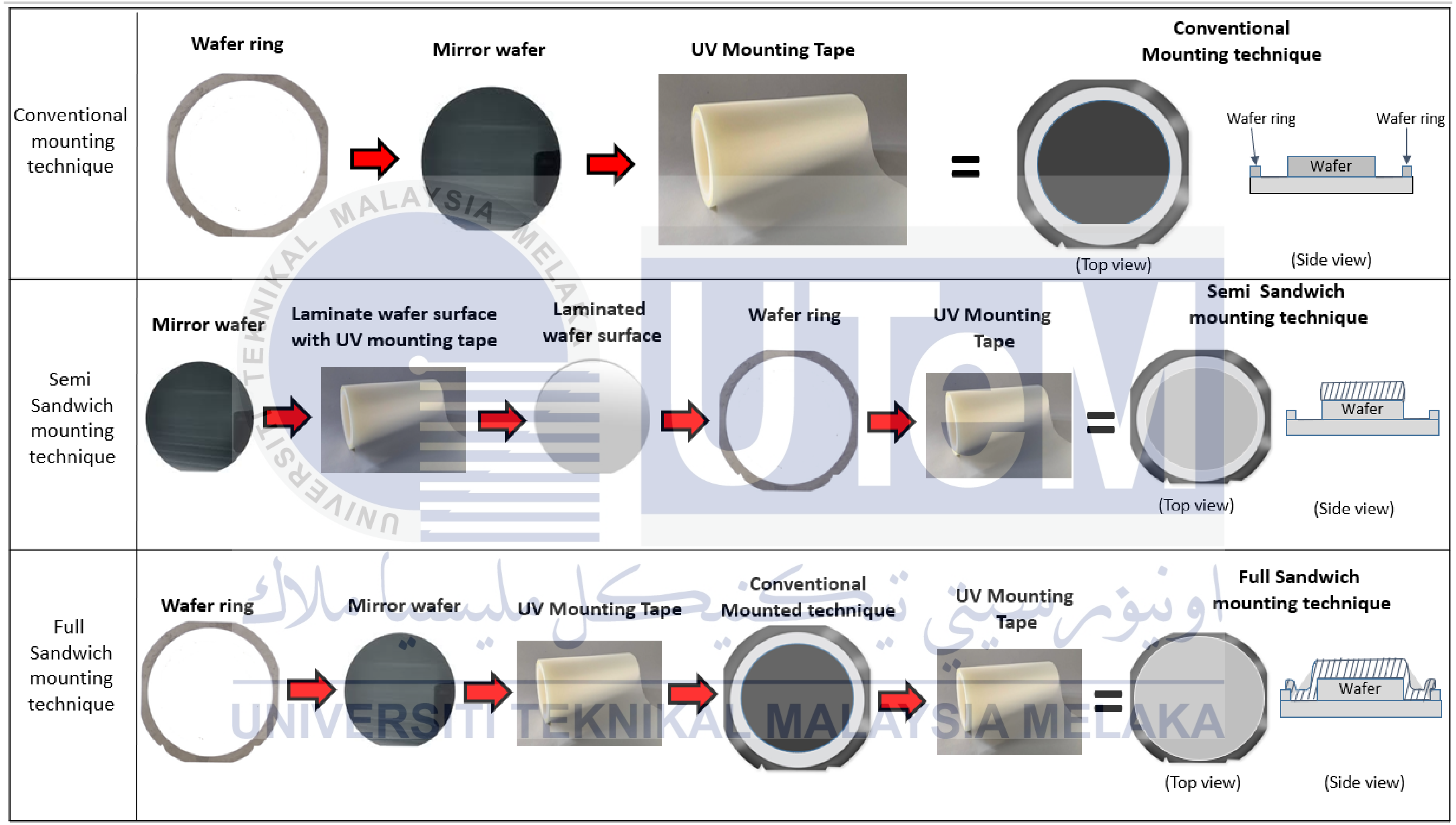


Figure 3.8: Wafer mounting techniques used in the research

According to Mohd Khairul (2022) UV tape outperformed non-UV tape regarding chipping and chip length during the wafer dicing process. This allows for a more accurate and meaningful comparison when evaluating performance, since this step is important to achieve lower chipping performance. To make the ultimate choice of mounting tape selection, it is necessary to take into consideration the following qualifications:

1) 100% yields in surface peeling test performance

2) Minimum degree of chipping on the topside and backside surfaces.

3) No crack die

To evaluate the performance based on the abovementioned criteria, the mounting tapes were assessed based on the mounting techniques outlined in Table 3.2.

Table 3.2: Mounting techniques vs mounting tape arrangement

Wafer mounting technique	Type of mounting tape on the wafer surface	Type of mounting tape at wafer back	UV curing after wafer dicing
1) Conventional mounting	No mounting tape	UV Tape	Yes
2) Semi Sandwich	Non-UV Tape UV Tape A	Non-UV Tape UV Tape A	No Yes
3) Full Sandwich	Non-UV Tape UV Tape A UV Tape B	Non-UV Tape UV Tape A UV Tape B	No Yes Yes

3.6 Wafer dicing

The wafer dicing process was performed using the Disco DFD6362 Fully Automatic Dicing Saw, as illustrated in Figure 3.9. Each silicon wafer was diced into fixed die dimensions of 6 × 6 mm, with a wafer thickness of 300 µm, employing a fixed diamond dicing blade to maintain consistency across all samples. Before the dicing operations, the equipment was calibrated by Disco Hi-Tec (Malaysia) Sdn. Bhd. to ensure optimal operating conditions. The corresponding calibration report is provided in Appendix C for reference.

Figure 3.9: Disco DFD6362 Fully Automatic Dicing Saw Machine

Throughout the research activities, the dicing parameters were maintained consistently across all wafer samples, regardless of the mounting technique employed. The process steps associated with the single-cut method, as applied in the conventional single-sided wafer mounting technique, are depicted in Figure 3.10. In this application, the dicing blade initiates cutting from the wafer surface, proceeds through the full thickness of the wafer, and extends an additional 20 µm into the mounting tape. This ensures complete separation of the dies while maintaining adherence to the underlying support tape.

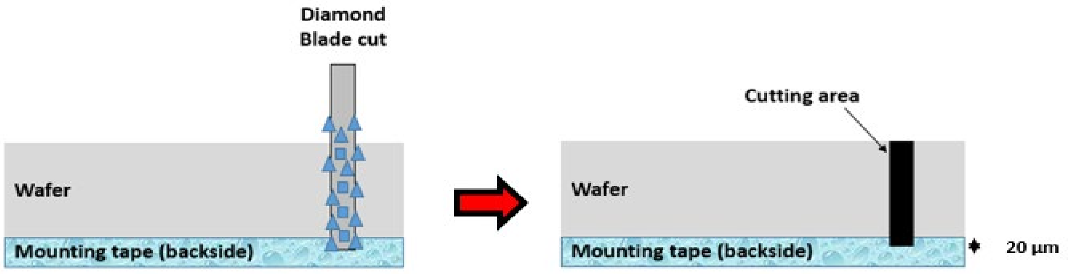


Figure 3.10: Illustration of single-cut process on single-sided conventional mounting

While for Figure 3.11 illustrates the process of the single-cut cutting method used for the double-sided semi and full sandwich wafer mounting techniques as well. The cutting initiates from the front side of the mounting tape and then penetrates down to 20 µm into the mounting tape of the backside of the wafer. The difference in wafer dicing methods between conventional, semi and full sandwich mounting is the presence of the mounting tape surface, which provides cushioning effects which require further chipping monitoring to see the impact on chipping, flexural strength and vibration performance.

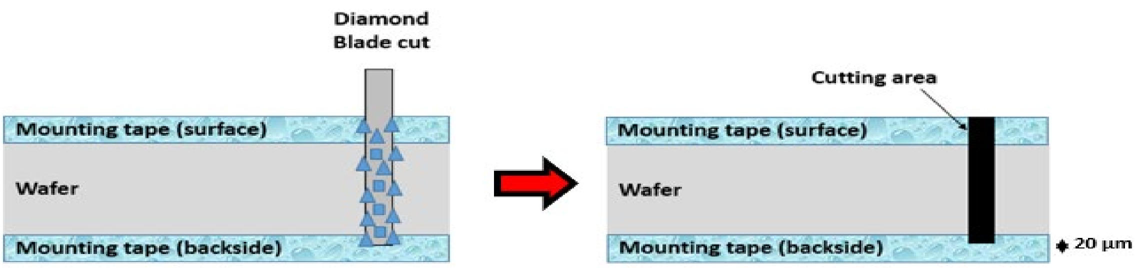


Figure 3.11: Illustration of single-cut process on double-sided semi and full sandwich mounting

The fixed dicing parameter used during the research can be referred to Table 3.3

Table 3 3: Fixed wafer dicing parameter

Parameter	Value
Wafer thickness	0.300 mm
Z height	0.065 mm
Feed speed	30 mm/s
Blade Rotation Per Minute (RPM)	40,000 RPM
Die size	6.00 x 6.00 mm

3.7 Ultraviolet (UV) curing

The primary function of the UV curing process is to reduce the adhesive strength of UV mounting tape, thereby facilitating an efficient and damage-free during the die pickup process. In the context of this study, where double-sided UV mounting tape was employed for both the semi-sandwich and full-sandwich wafer mounting techniques, the UV curing process was implemented to fulfil two specific objectives. The first objective was to enable the clean removal of the surface-mounted tape during the post-dicing cleaning stage, thereby eliminating the need for a manual surface tape peeling procedure. Once successful the automatic surface tape removal was achieved, the second objective was to ensure that individual dies could be effectively detached from the backside mounting tape. This step was essential for enabling accurate measurement and analysis of chipping on the diced samples.

If the first objective cannot be achieved during the activity, then manual surface peeling is performed. For the double-sided wafer mounting technique, the UV curing required two times additional UV curing. The first UV curing is for removing the surface mounting tape that is applied on the wafer surface. The second UV curing was conducted after the wafer dicing process/surface manual peeling process to ensure the die could be picked up for chipping measurement purposes. During the research activities, the Lintec RAD-2010 UV curing equipment was utilized as shown in Figure 3.12 and the activities were done in a cleanroom environment. However, the UV curing machine was initially calibrated to ensure optimal operating conditions, as documented in the calibration report provided in Appendix D.

Figure 3.12: Lintec RAD-2010 UV curing

Table 3.4 displays the initial parameter used on earlier research activities during the UV curing process.

Table 3.4: Initial UV curing parameter

Mounting Tape	**UV Parameter**	**Value**
Surface mounting tape	UV irradiation speed	15.0 mm/sec
	Exposure dose	552 mJ/cm^2
Backside mounting tape	UV irradiation speed	43.3 mm/s
	Exposure dose	190 mJ/cm^2

Despite initial efforts, the baseline UV curing parameter required a manual procedure to remove the surface mounting tape, rendering it unsuitable for high-throughput production environments. The primary objective was to achieve automated surface tape removal by optimizing the UV curing parameters during the wafer cleaning process. However, a UV exposure dose of 552 mJ/cm^2 proved ineffective in detaching the surface mounting tape during this stage.

As a result, two higher UV dosage levels were subsequently evaluated to enhance the tape removal efficiency. It is important to note that the applied UV dosage is directly influenced by the UV irradiation speed. Specifically, a lower irradiation speed results in a slower wafer movement beneath the UV lamp, thereby increasing the total UV exposure received by the surface mounting tape. This relationship was leveraged to optimize the curing conditions for improved surface tape removal performance.

As presented in Table 3.5, the evaluation of various UV irradiation speeds demonstrated that complete removal of the surface UV mounting tape could be achieved after the wafer cleaning process. This outcome confirms the effectiveness of the optimized UV curing conditions for surface tape removal. In contrast, the UV curing parameters for the backside mounting tape were held constant across all experimental runs, as the selected settings consistently yielded satisfactory results in terms of die pick-and-place performance.

Table 3.5: UV curing evaluation for surface mounting tape removal after washing

Mounting Tape	UV Parameter	Max Setting	Med Setting	Min Setting
Surface mounting tape	UV irradiation speed	15.0 mm/sec	10.0 mm/sec	5.0 mm/sec
	Exposure dose	552 mJ/cm^2	827 mJ/cm^2	1653 mJ/cm^2
Backside mounting tape	UV irradiation speed	43.3 mm/s		
	Exposure dose	190 mJ/cm^2		

The table demonstrates an inverse relationship between UV irradiation speed and exposure dose. As the irradiation speed decreases, the exposure dose increases and it causes a longer exposure time. When the UV irradiation speed is low (e.g., 5.0 mm/sec), the tape moves slowly under the UV source and gets the highest exposure dose (1653 mJ/cm^2). This suggests that slower speeds allow for a longer UV exposure, resulting in a higher energy dose applied to the mounting tape. In semiconductor processing, optimizing UV exposure settings is essential for controlling the adhesive properties of the mounting tape. A higher exposure dose (from lower speeds) typically enhances tape detachment performance, which is crucial for wafer separation post-dicing. Conversely, a lower exposure dose (from higher speeds) might help maintain better tape adhesion during wafer processing, minimizing the risk of wafer shifting or chipping. Proper parameter selection ensures process stability and improved yield in wafer-dicing applications

Implementing a rapid removal of the surface mounting tape during the wafer cleaning process eliminates the necessity for the manual surface peeling test, therefore the positive result will decrease the processing time of surface mounting tape removal from 5 minutes to 30 seconds and require the optimum UV irradiation speed. The manual peeling test requires careful and slow execution, resulting in inconsistencies in peeling force and prolonged processing time. In contrast, the implementation of an automated peeling process within the wafer cleaning procedure offers several advantages, including consistent water pressure, controlled table rotation, and enhanced process efficiency. This automation enables faster and more uniform tape removal. Once the process parameters are optimized to achieve automatic surface mounting tape removal within the wafer cleaning stage, subsequent chipping measurement and crack inspection can be conducted efficiently.

Mounting tape peeling test using tensile strength machine

A mounting tape peeling test was conducted to evaluate the adhesion performance of each mounting tape sample following the UV curing process. In this assessment, the selected UV mounting tape was precisely cut according to the standard jig dimensions, with a fixed width of 25 mm, and subsequently affixed to the surface of a silicon mirror wafer. The tape was adhered to the wafer surface to examine its adhesion characteristics, particularly focusing on manual surface peeling and automated removal during the wafer cleaning process, facilitated by UV optimization. The adhesion results are important for analyzing the manual peeling and the automatic mounting tape removal after the wafer cleaning process.

The Tensilon RTG-1210 per Figure 3.13 is an advanced equipment designed for the precise evaluation of materials' tensile strength and mechanical properties. As a universal testing machine (UTM), it is capable of conducting a diverse range of mechanical assessments, including tensile, compression, and flexural tests. The silicon mirror wafer with UV tapes on the wafer surface was then UV cured according to 10 mm/s and 15 mm/s UV irradiation speed, and then, the peeling test was performed towards the UV cured tape to understand the adhesion behaviour. However, before the activities started, the Tensilon RTG-1210 was checked to have completed the calibration by the machine provider, which could be referred to Appendix F.

Figure 3.13: Tensilon RTG-1210 UV mouting tape peeling tester

Once the mounting tapes on the mirror wafer were cured, the tapes were clipped by the Tensilon RTG-1210 and were pulled at 180 degrees as per Figure 3.14 based on test speed of 300 mm/min. The peeling results were then automatically recorded in the computer for compilation and analysis purposes.

Figure 3.14: 180-degree peeling test

3.8 Sample performance monitoring

This section provides an overview of the tests and measurements of the samples during the research activities to achieve the objectives set earlier. This is to ensure that the quality set for establishing the conventional and wafer mounting techniques met the quality criteria set for this activity.

3.8.1 Wafer cleaning process

The wafer cleaning process is a standard procedure that is conducted following the dicing process. This process is designed to remove any foreign particles or silicon dust from the wafer surface. In order to reduce the adhesiveness of the UV mounting tape on both the surface and backside of the wafer, it is necessary to perform a two-step UV curing procedure. To proceed with the die chipping measurement process, it is a must to eliminate the UV mounting tape from the wafer's surface during the cleaning process, as illustrated in Figure 3.15.

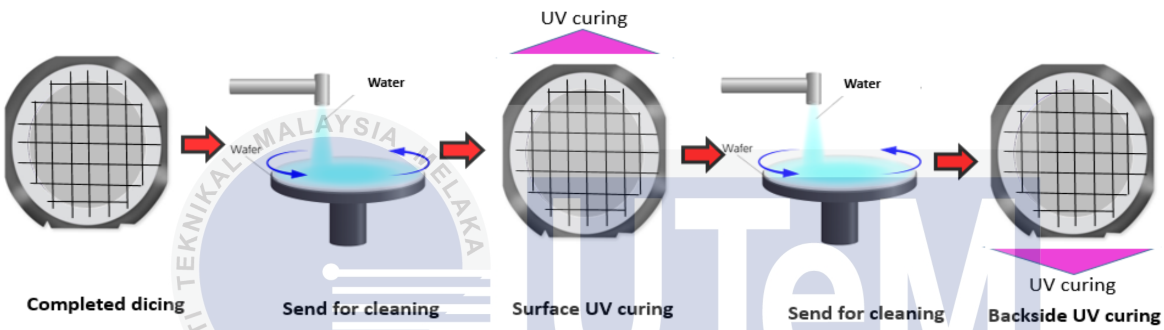


Figure 3.15: Wafer cleaning process on mounting technique with UV mounting tape

The manual surface peeling test will be omitted if the surface mounting UV tape can be removed during the cleaning procedure. Nevertheless, it is important to achieve an automatic peeling process during the wafer cleaning process to achieve higher UPH and be suitable for manufacturing practice.

3.8.2 Manual surface peeling test

A manual surface peeling test was developed to remove the surface mounting tape that applied on the wafer surface for semi and full sandwich wafer mounting process if not able to remove it during cleaning process. The wafer mounting approach has recently been revised to incorporate this new method, which is considered a crucial stage in deciding the overall success of the research. The procedure begins by manually allocating the sawn wafers to the wafer-dicing chuck table. Subsequently, the vacuum feature of the wafer-dicing chuck table is activated to ensure a firm grip on the die and to prevent any potential damage that may arise during the surface peeling procedure. Figure 3.16 demonstrates that the surface peeling test technique commences by placing a layer of cellophane tape onto the surface of the UV tape. Afterwards, the cellophane tape was pulled off to remove the surface mounting tape. If the cleaning process able to remove 100% of the mounting tape then the manual surface peeling test process will be skipped.

Figure 3.16: Surface peeling test process steps

Equation 3.1 represents the mathematical approach to determine the surface peeling test yield.

$$S = \left(\frac{T-U}{T}\right) x\ 100\% \tag{3.1}$$

In Equation 3.1, S represents the surface peeling test yield, T represents the total die amount per wafer, and U represents the total die with unpeeled surface tape.

3.8.3 Chipping measurement

As part of the research, chipping measurement was performed according to all mounting techniques. The chipping measurement process begins with the use of Zeiss Axioscope 2 MAT with 50x magnification. However, for areas that require further verification in terms of cracks a higher magnification will be used. For the wafer dicing process, the optical microscope is a common instrument that is utilized for the purpose of monitoring chipping and cracks (Feng et al., 2022).

Before commencing the research operations, the optical microscope underwent a calibration process using a microscope micrometer calibration ruler as shown in Figure 3.17. The ruler was allocated on the microscope stage and then by using the coarse and fine adjustment knobs to focus the microscope until the scale of the calibration ruler is clearly visible. Then align the divisions (e.g., 0.1 mm or 0.01 mm) parallel to the field of view through the microscope lens. Utilise the measuring software to conduct measurements based on the displayed figure from the calibration ruler, adjusting the alignment factor until the measurement reading corresponds with the known value, and thereafter save the configuration. Verify the other value by performing measurement software and once the same value is obtained, the calibration is completed.

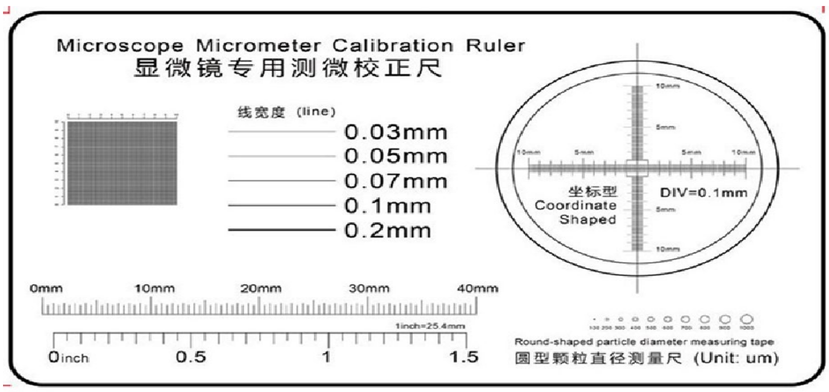


Figure 3.17: Microscope micrometer calibration ruler

For chipping measurement samples preparation, a fixed location of 30 die samples were picked up using a plastic tweezer and vacuum pen based on each mounting technique. A plastic tweezer and vacuum pen were used to avoid extra chipping occurrences during the die pick-up process. Since the die size 6 x 6 mm was diced for chipping measurement, 50x magnification was not able to capture a chipping picture based on the overall die size. For this situation, the overall chipping measurement was done by performing sectioning as illustrated in Figure 3.18. To simplify the process of measuring the chipping area, each image was taken into 12 sections along the topside and backside areas. The chipping areas then was calculated using the ImageJ software based on the specified sections after the images were uploaded. The chipping area, originally measured in μm^2, was standardized by converting it to mm^2. Distribution of the converted value among sections was thereafter carried out in order to acquire the overall sum of all the chipping measurements. Gao et al. (2013) used the same procedure to determine the chipping area, however AutoCAD software was used for the purpose.

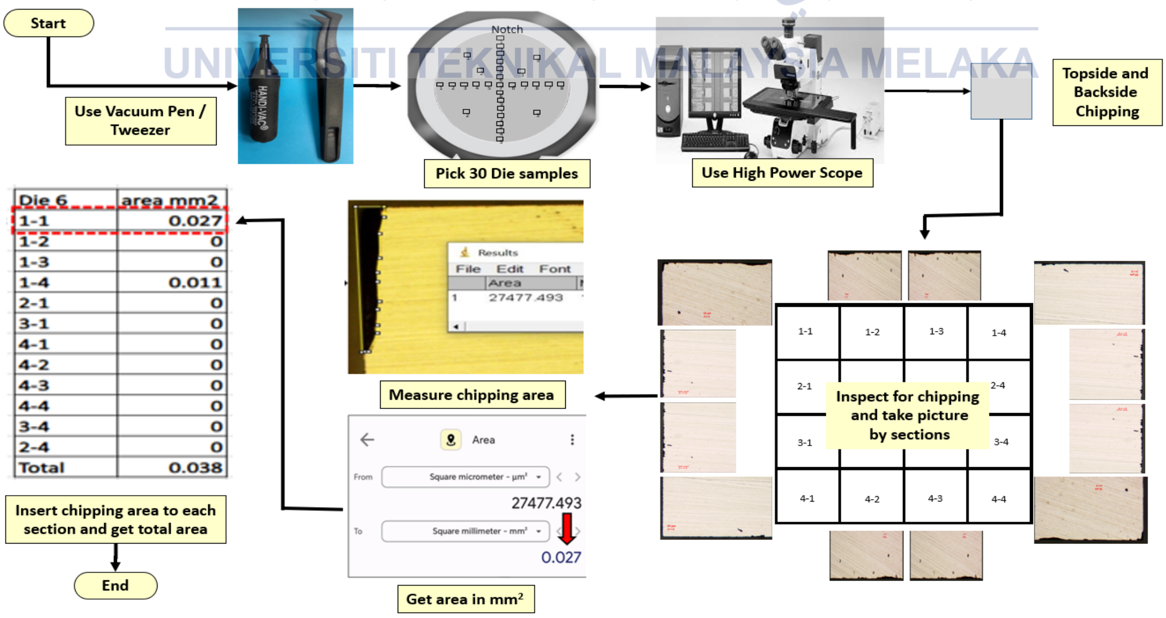
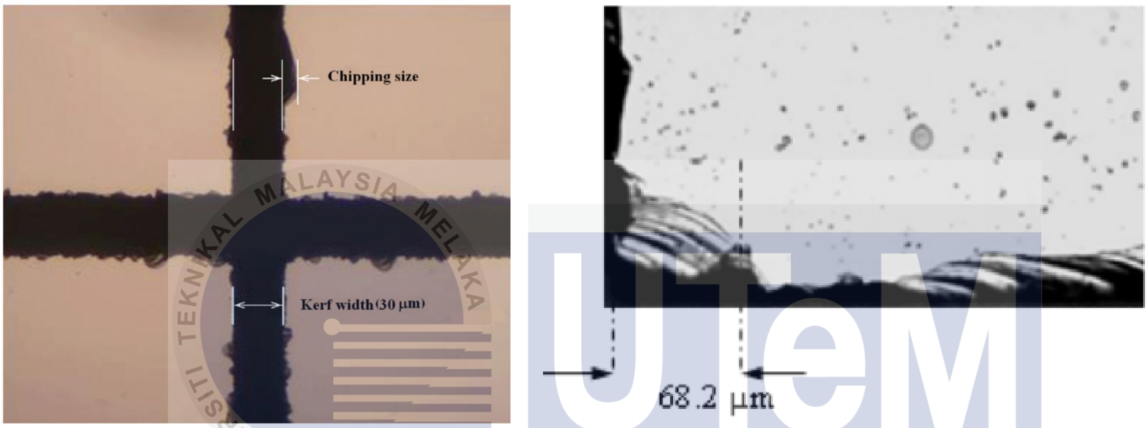


Figure 3.18: Chipping measurement process flow

In chipping measurement methodologies, the majority of previous research has employed a length-based approach, wherein the chipping is quantified by measuring the distance from the die edge to the furthest point of the chipping curve. This method, as illustrated in Figure 3.19, provides a straightforward means of assessing chipping severity along a linear path and is widely used due to its simplicity and efficiency in capturing the extent of individual chipping events.



(a) (b)

Figure 3.19: Chipping measurement (a) Topside area (b) Backside area

Lin and Cheng (2014) measured topside chipping by evaluating the distance from the kerf edge to the chipping boundary, focusing solely on the area with the maximum chipping, as illustrated in Figure 3.19(a). In comparison, Jiun et al. (2006) assessed backside chipping by measuring the chipping length from the die edge to the furthest extent of the chipped region, as shown in Figure 3.19(b). Although both methods allow for rapid evaluation of chipping performance, they are limited by their focus on a single point of maximum chipping per die, which may not accurately represent the overall chipping condition across the entire wafer. In contrast, the measurement approach adopted in this study involves quantifying the chipping area across multiple regions on each die to provide a more comprehensive understanding of chipping distribution. While this method offers a more accurate representation of the overall chipping performance, it is considerably more time-consuming, as it requires detailed inspection of each die area during the measurement process.

3.8.4 Crack inspection

Crack inspection is a crucial procedure to see if the new process meets the initial quality standards. At times, cracks may go undetected by the optical high-power scope because of its limitations, so a Scanning Electron Microscope (SEM) was utilized instead. SEM with magnifications of 100x and 1000x were utilized during the inspection to detect any potential cracks and ensure a smooth process.

3.8.5 Die backside topography measurement

As the wafer did not undergo a back wafer polishing process, it was crucial to investigate the impact of the die backside topography on chipping performance during the dicing process. Without back polishing, the rear surface of the silicon die retains grinding marks, which may contribute to surface irregularities, unlevelness and potential mechanical weaknesses. Understanding these surface characteristics is essential to determine whether they influence the wafer's tendency to chip, particularly under mechanical stress during dicing.

To assess the backside surface condition, a three-dimensional (3D) topography measurement was conducted using a non-contact Shodensha GR3400 3D profiler. This optical profiler employs light-based technology to capture detailed surface features without making physical contact with the wafer. The system measured the back surface of the silicon die, focusing specifically on the grinding marks produced during the thinning process. This analysis was performed to determine whether the surface roughness and topographical features caused by grinding contribute significantly to excessive chipping observed during the wafer dicing stage.

3.8.6 Three-point bending test

Three-point bending test is a method to test the flexural strength of the silicon die. It is important to analyse the die flexural strength performance towards the implementation of double-sided wafer mounting techniques and its effects after the dicing process. One of the most commonly used techniques for die strength characterization is the 3-point bending test (Tsai and Huang, 2022), which is widely accepted in the semiconductor industry (Talledo, 2021a). For three-point bending test on the silicon die, the flexural strength (given the symbol σ) could be used according to the following Equation 3.2 (Chang and Ler, 2022):

$$\sigma_{3\ point} = 3sF / 2wh^2 \qquad (3.2)$$

whereby F = Force of fracture in Newtons (N)

s = span in millimetres (mm)

w = width of the die in millimetres (mm)

h = thickness of the die in millimetres (mm)

Figure 3.20 illustrates the definition of the equation above.

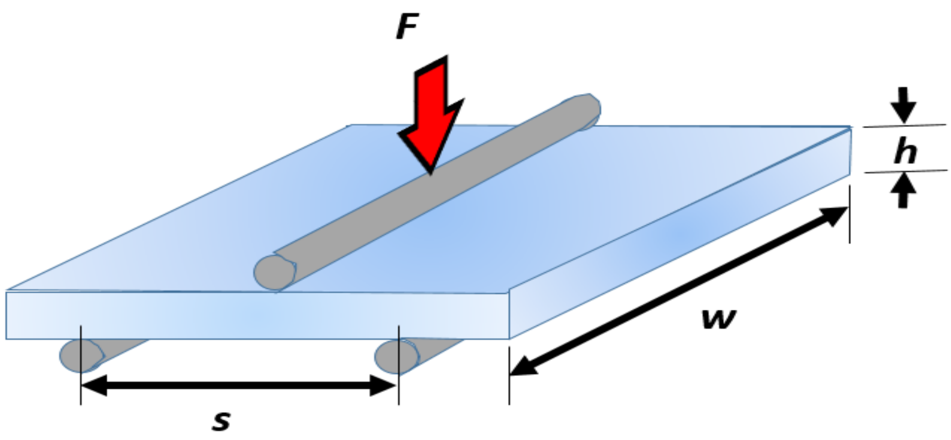


Figure 3.20: Three-point bend test equation definition

During the activities, a three-point bending test was conducted on the silicon die to measure its flexural strength using a 50N Shimadzu EZ-LX machine, as shown in Figure 3.21. However, before the activity started, the calibration was done earlier by the supplier to ensure the equipment was in optimum condition and the results can be referred to Appendix E.

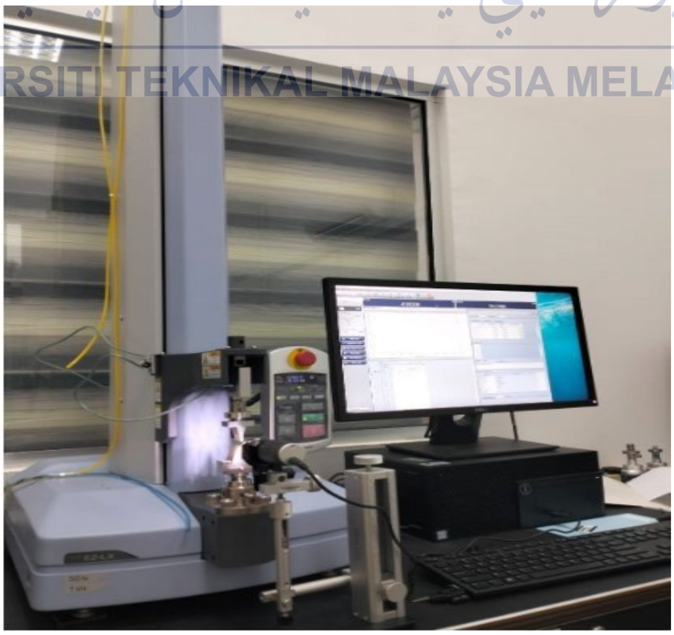


Figure 3.21: 50N Shimadzu EZ-LX machine for three-point bending test

The jig was fabricated in compliance with SEMI G86-0217 Standards (SEMI, 2022). Given the specifications of the jig, the span was set at 5mm (Talledo, 2021b), with a pin radius of 0.3 mm, and a fixed test speed of 3mm/min. During the three-point bending test operation, a camera was placed in front of the jig to ensure the die was positioned uniformly and the punch positioned in the exact middle of the die surface, as shown in Figure 3.22.

Figure 3.22: Camera for consistent die positioning on jig during three-point bending test

3.8.6.1 SEMI G86-0217 Standards

SEMI G86-0217 was a standard test method for measuring chip (die) strength using the 3-point bending method and a procedure to test the die strength. All the die strength measurements in these activities were using SEMI G86-0217 as a reference. A few criteria were highlighted in the standard to fulfil before the test could begin as below:

1) The test specimen shall be a silicon die
2) At least 25 test specimens shall be pulled from a wafer.
3) Adjust the span L, in accordance with the following conditions,

    • at $h < 0.1$ mm : $L \leqslant 2$ mm and $L \leqslant 50\,h$

• at h ⩾ 0.1 mm : 2 mm ⩽ L and L ⩽ 20 h

where h = die thickness

4) Set the test speed less than 5 mm/min in order to avoid the impact on test specimen and apply the force at midspan.

5) The radius of the supports and the loading edge shall be 0.3 mm ± 0.02 mm per Figure 3.23.

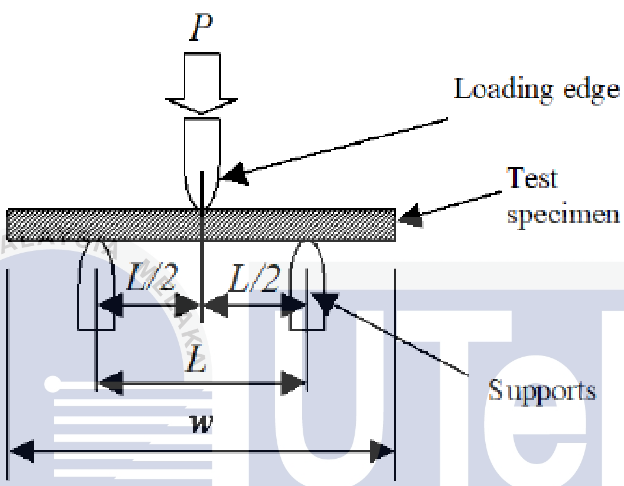


Figure 3.23: 3-point bending test jig design specification

The 3-point bending test jig was fabricated following the SEMI G86-0217 standard, and the final test jig design is illustrated in Figure 3.24. The dimensions and detailed drawings of the jig can be found in Appendix A.

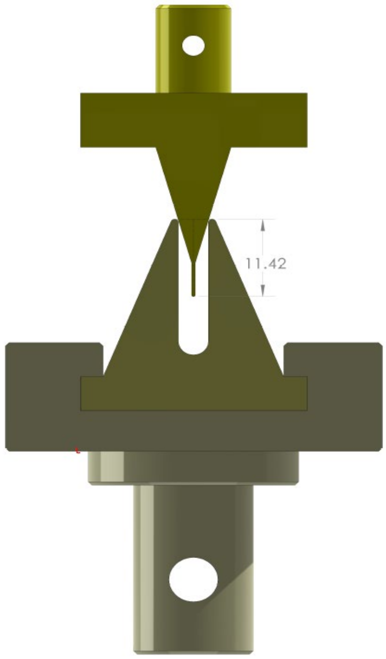


Figure 3.24: Final 3-point bending test jig design

3.8.7 Wafer dicing vibration analysis

Analysis of the vibration performance of wafer dicing equipment is crucial for evaluating each wafer mounting technique used in the wafer dicing process. The purpose of this study is to establish a correlation between the chipping performance and the machine vibration. This is to validate the previous hypothesis that higher vibration will result in higher chipping performance. However, up till now, there is no vibration analysis has been done on the wafer mounting technique during the wafer dicing machine to confirm the statement. The vibration experiment was carried out concurrently with the dicing process. As shown in Figure 3.25, a piezoelectric film sensor was connected to the National Instruments Sound and Vibration module NI-9234 in order to collect vibration data. Upon connecting the NI-9234 to a notebook, the data will be shown and stored in the NI Signal Express program.

Figure 3.25: Vibration analysis tools

The positioning of a piezoelectric film sensor in front of the cutting area of the Disco DFD6362 Fully Automatic Dicing Saw machine was carried out for this activity. This setup is depicted in Figure 3.26 and was utilized throughout the research activities. The vibration data will undergo filtering using MATLAB to include only the values related to the dicing process. The vibration data associated with the movement of the table index for each subsequent cutting line will be excluded. An analysis was conducted on 100 seconds of dicing activities using JMP software and the Analysis of Variance (ANOVA) method.

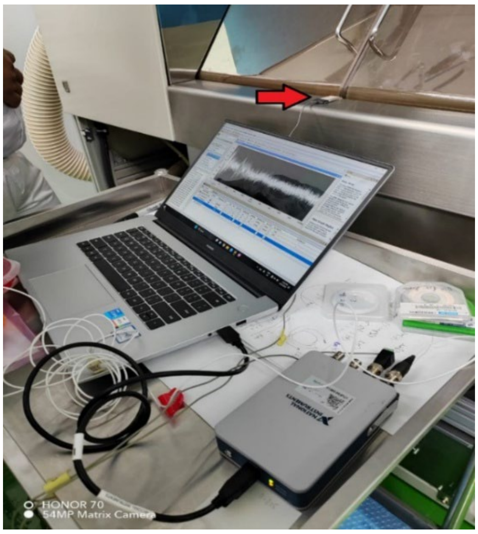


Figure 3.26: Vibration analysis setup

3.9 Summary

The following section provides an overview of the research materials and methods employed in the development of a double-sided mounting technique for enhancing chipping activities on silicon wafers. The chipping improvement was divided into three stages. During stage 1, the primary objectives were to identify the optimal mounting tape and wafer mounting techniques that result in significantly reduced chipping performance compared to conventional single-sided wafer mounting techniques based on wafer worst case or highest stress condition which is wafer with backgrinding marks which do not have polishing or stress relief. This wafers condition have wafer backside levelling condition from the backside grinding topography which is critical during wafer mounting and wafer dicing as well. The high power scope and Scanning Electron Microscope (SEM) were utilized to examine the singulation results and whether each mounting technique resulted in excessive chipping and developed cracks after the dicing process.

During stage 2, the chipping performance was assessed for all mounting techniques using a three-point bending test. The test speed was evaluated to determine the optimal level of flexural strength performance based on the wafer dicing process from each wafer mounting technique. The highest flexural strength results will represent the highest die strength performance and robust process which is good for the device reliability.

The final stage 3 involves vibration analysis during the wafer dicing process for each mounting technique. This analysis is performed to verify the vibration performance of each wafer mounting technique in relation to chipping. The vibration data was filtered using MATLAB and analyzed using JMP statistical tools to verify the results.

The development of the double-sided wafer mounting process involved several key activities, including the selection of suitable mounting tapes, tensile strength testing for tape peeling using a universal testing machine, both manual and automated surface tape peeling evaluations, optimization of UV curing parameters, and wafer dicing coupled with vibration monitoring. These process development activities were carried out at Lintec Advanced Technologies (Malaysia) Sdn Bhd. Meanwhile, the subsequent analysis, including chipping measurements and flexural strength testing, was conducted at Universiti Teknikal Malaysia Melaka (UTeM).

CHAPTER 4

RESULTS AND DISCUSSIONS

4.1 Introduction

The results of the experimental work described in the previous section are presented in this chapter. The objective of this investigation is to concentrate on three primary findings. The purpose of this chapter is to present a summary of the experiment's results on a non-polish backside silicon wafer, with a particular emphasis on chipping improvement during dicing activities. The first part represents the result of the preliminary study on developing double-sided wafer mounting techniques for chipping improvement on non-polish backside silicon wafers. The second part involves analyzing the flexural strength using a 3-point bending test toward all wafer mounting techniques. The last part concerns verifying each mounting technique's chipping and flexural strength with vibration analysis during the wafer dicing process.

4.2 Developing a double-sided wafer mounting technique

This study is driven by the objective of identifying the double-sided wafer mounting technique to achieve the lowest chipping measurements. The technique is a new approach to replace the conventional single-sided technique to increase the wafer gripping and provide cushioning effects on the wafer surface during the wafer dicing process to minimize the vibration and improve the chipping performance. The double-sided mounting technique aims to minimize chipping, particularly for silicon wafers with backgrinding marks at the backside, which has the highest stress condition for the back grinding process.

The evaluation was conducted to determine the appropriate adhesion properties of the mounting tape when developing the double-sided wafer mounting technique. The primary objective was to enhance chipping performance without cracks and ensure that the surface mounting tape could be removed manually or automatically after the wafer cleaning process without leaving any residue. To provide a comprehensive understanding to achieve the research objectives 1, 2 and 3, detailed activities are provided in Figure 4.1.

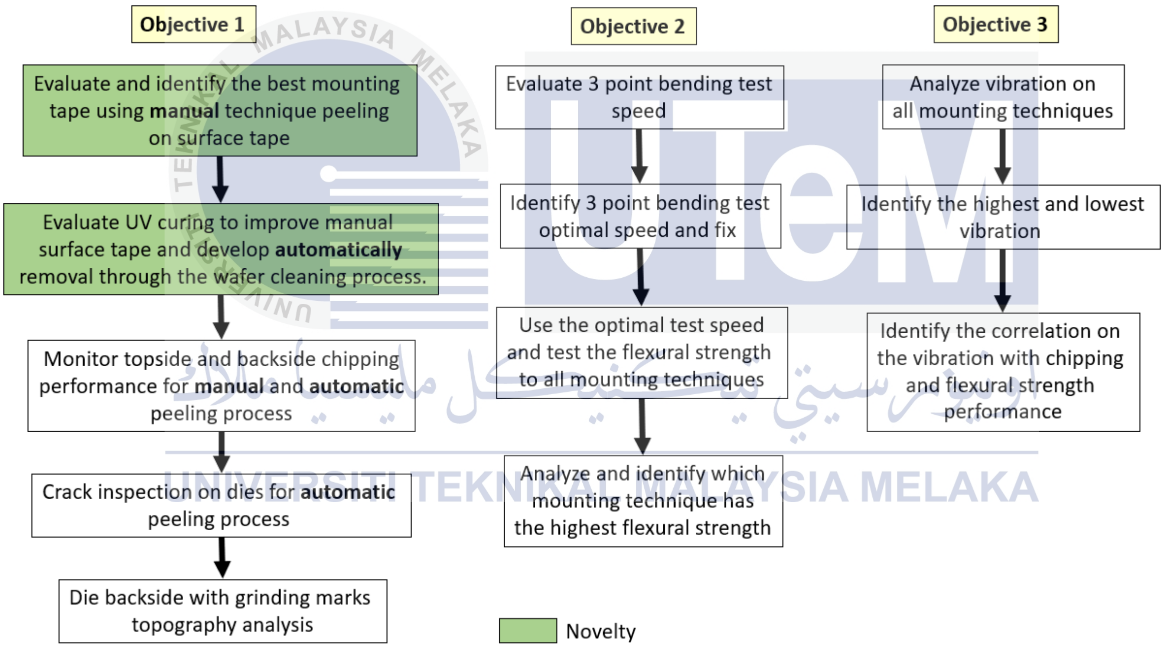


Figure 4.1: Overview of data collections involved on achieving all objectives

Figure 4.1 outlines the three main research objectives, each comprising several key tasks. The novelty of this study is highlighted in Objective 1, where a dual-approach evaluation of surface mounting tape is introduced, first through manual peeling and then improved via UV curing to enable automatic removal during the wafer cleaning process. This innovation is particularly significant as it aims to streamline surface tape removal, a known bottleneck in wafer processing. Additionally, the study integrates top and backside chipping monitoring, die crack inspection, and grinding mark analysis, which are rarely explored in combination. These novel contributions provide a more comprehensive understanding of tape behaviour and its impact on wafer chipping performance. Objectives 2 and 3 support this novelty by systematically evaluating flexural strength through optimized three-point bending tests and correlating vibration effects across different mounting techniques. Collectively, these integrated tasks form a unique and holistic methodology for advancing wafer mounting practices in semiconductor manufacturing.

4.2.1 Evaluating surface mounting tape removal through manual peeling test

In the initial implementation of the double-sided wafer mounting process, the surface mounting tape could not be completely removed using the wafer cleaning process. As a result, a manual peeling test was introduced to address this limitation. The surface manual peeling test plays a critical role in identifying the most suitable mounting tape for the development of the double-sided wafer mounting technique. The objective of this test is to ensure a 100% yield in surface peeling performance, meaning no residual mounting tape remains on the wafer surface. Any residual material can interfere with subsequent processing steps, compromise bonding efficiency, or introduce contamination. Such residuals may further lead to electrical or mechanical defects, ultimately degrading the overall performance and reliability of semiconductor devices. Thus, optimizing the wafer mounting process is essential for maintaining product integrity and quality.

Table 4.1 displays the results of a manual surface peeling test conducted on three wafer mounting techniques: conventional mounting, semi-sandwich mounting, and full sandwich mounting. Since the conventional mounting was based on single-sided wafer mounting technique, UV tape A is applied to the back of the wafer with no mounting tape is applied to the wafer surface, so surface tape removal is unnecessary. All the sawn wafers with UV mounting tape were UV cured based on the standard UV curing irradiation speed of 15 mm/s parameter, which then required a manual peeling process for removing the surface mounting tape.

Table 4.1: Initial 15 mm/s UV curing irradiation speed surface mounting tape peeling test results

Wafer mounting technique	**Type of mounting tape on wafer surface /adhesion after UV (for UV tape)**	**Types of mounting tape at wafer back**	**Surface mounting tape removal through manual peeling test yield**
Conventional mounting	No mounting tape	UV Tape A (80 mN /25mm)	Not applicable. No mounting tape was applied on the wafer surface
Semi sandwich mounting	Non-UV Tape (940 mN / 25mm)	Non-UV Tape (940 mN / 25mm)	0%
	UV Tape A (80 mN /25mm)	UV Tape A (80 mN /25mm)	70%
Full sandwich mounting	Non-UV Tape (940 mN / 25mm)	Non-UV Tape (940 mN / 25mm)	0%
	UV Tape A (80 mN /25mm)	UV Tape A (80 mN /25mm)	70%
	UV Tape B (30 mN/25mm)	UV Tape B (30 mN/25mm)	100% (Highest)

The unit mN/25 mm (milliNewtons per 25 millimetres) is used to express the peel adhesion strength of mounting tape, indicating the amount of force required to peel the tape from a substrate over a 25 mm wide strip. While this unit is based on force per unit width, it is often used as a practical surrogate for evaluating adhesive strength, which can also be conceptually linked to force per unit area (pressure). To relate it to force/area, one must consider both the tape width (25 mm) and the length of contact during peeling, allowing for an estimation of the applied adhesive force across the bonded surface area. A higher mN/25 mm value suggests stronger adhesion, resulting in more force being required to separate the tape from the wafer, while a lower value indicates weaker bonding. In semiconductor wafer processing, such as during wafer mounting, this measure helps ensure that the tape provides adequate holding force to secure the wafer, while still allowing for clean removal without inducing damage to the wafer or dies.

To enhance clarity and improve reader comprehension, the activities and results summarized in Table 4.1 have been further illustrated in the form of an infographic, as shown in Figure 4.2. This visual representation was developed to simplify complex data and highlight key comparisons and trends in a more intuitive manner. By presenting the information graphically, it allows readers to quickly grasp the overall flow, critical observations, and outcomes of the evaluated processes. The use of infographics serves as an effective communication tool, especially for conveying multi-step procedures and performance results, thereby supporting a clearer understanding of the research findings.

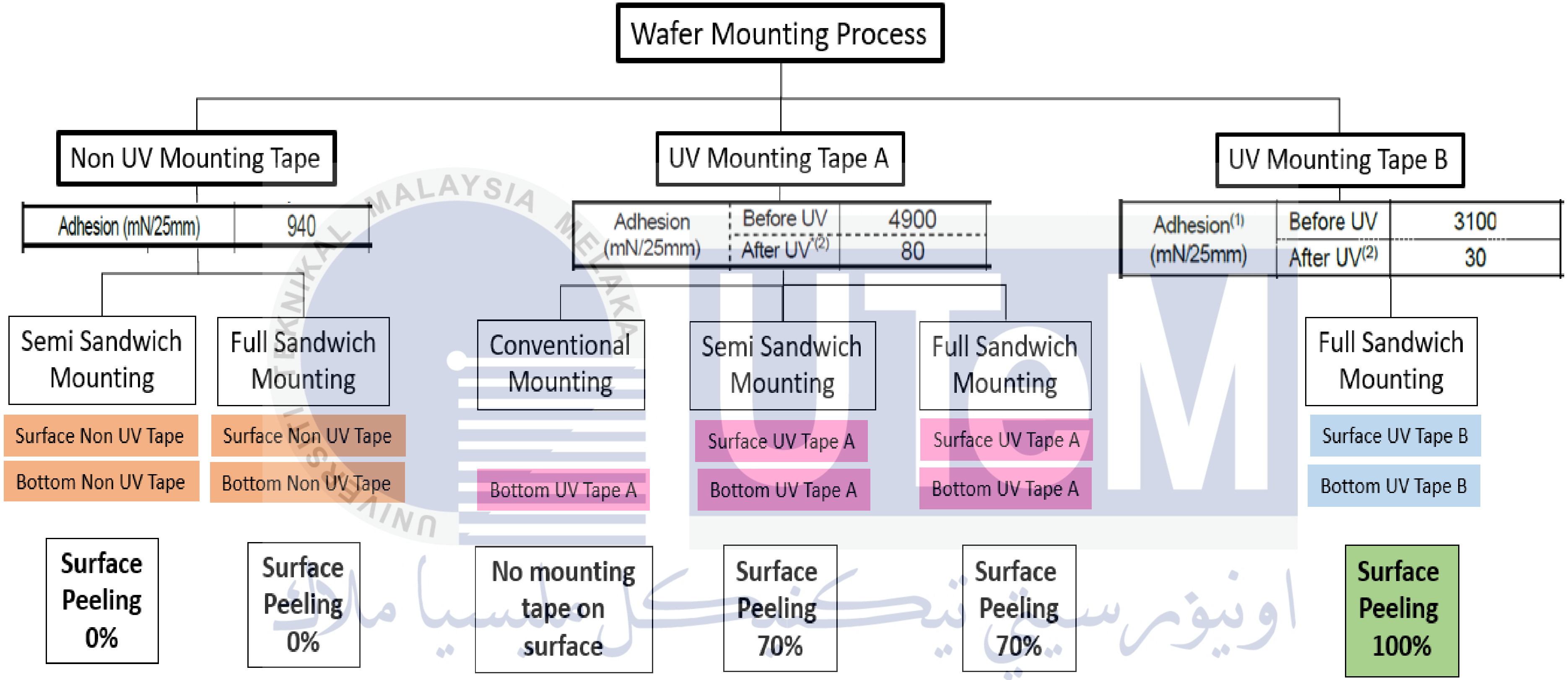
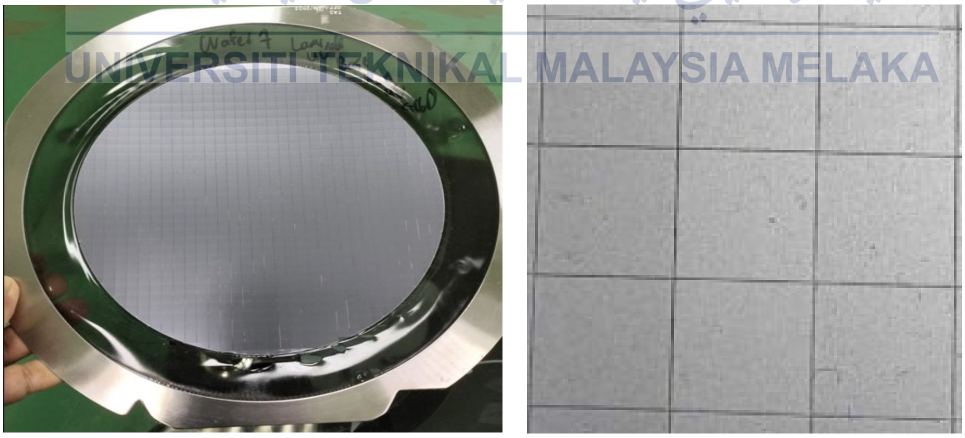


Figure 4.2: Summary of surface mounting tape manual peeling results based on 15mm/s UV curing irradiation speed

The results demonstrated the performance of the non-UV tape when used in the wafer surface mounting process. The tape, which has an adhesion value of 940 mN/25 mm, was tested for its removability and manual peeling yield. However, the outcome was unfavourable, as the tape failed to achieve 100% removal from the wafer surface. Figure 4.3(a) clearly shows that the non-UV tape remained on the diced wafer surface after the wafer cleaning process. This incomplete removal resulted in a surface tape manual peeling test yield of 0%, indicating that the non-UV tape is not suitable for applications requiring full surface tape detachment after processing, as per the zoom area on Figure 4.3(b). The inability to cleanly remove the tape may lead to process contamination or reliability issues in downstream semiconductor manufacturing steps. The surface mounting tape removal through manual peeling test yield calculation percentage was base on the Equation 3.1 given earlier. It is calculated by taking the total number of dies on the wafer, subtracting the number of dies that still have unpeeled surface tape, and then dividing the result by the total number of dies on the wafer.



(a) (b)

Figure 4.3: Non UV Tape with 0% manual peeling results (a) low magnification (b) zoom area on the wafer surface

Next the test results for UV Tape A, which has an adhesion strength of 80 mN/25 mm after UV exposure, indicate partial success in surface tape removal. As shown in Figure 4.4(a), although some die areas were successfully cleaned, the tape was not completely removed from the entire wafer surface. This partial detachment resulted in a manual peeling test yield of 70%. The remaining adhesive residue or tape sections as shown in zoom area in Figure 4.4(b), particularly visible in certain die regions, suggest that UV Tape A lacks sufficient UV-induced adhesion reduction or mechanical peelability to achieve full removal. Consequently, although it performs better than the non-UV tape, it still does not meet the desired standard for 100% surface tape detachment. This limitation could impact downstream processes, especially where full die exposure and cleanliness are required for high-reliability packaging or inspection tasks. Therefore, UV Tape A may be considered moderately effective but not ideal for processes that demand complete surface tape removal.

(a) (b)

Figure 4.4: UV Tape A with 70% manual peeling results (a) low magnification (b) zoom area on the wafer surface

The experimental results revealed that UV Tape B, characterized by the lowest after UV exposure adhesion strength of 30 mN/25 mm, exhibited the most favourable performance among all tested tape materials. This outcome highlights its optimal adhesion properties, which facilitated the complete removal of the surface tape without leaving residual contaminants, thereby ensuring a clean wafer surface post-dicing. These findings underscore the critical role of low-adhesion UV tapes in supporting the double-sided wafer mounting technique, as they enable full surface tape removal while simultaneously preserving sufficient wafer stabilization throughout the dicing process. The effectiveness of UV Tape B thus validates its suitability in enhancing the reliability and practicality of the proposed mounting configuration for advanced semiconductor dicing applications.

As shown in Figure 4.5(a), the UV tape was successfully removed from the wafer surface without leaving any visible residue, achieving full removal across all dies. This successful removal resulted in a manual peeling test yield of 100%, indicating excellent tape behaviour during the cleaning process. The effectiveness of UV Tape B is attributed to its low adhesion value after UV exposure, which facilitates easier peeling while still maintaining sufficient hold during wafer processing. The clean surface observed in the zoom area from Figure 4.5(b) confirms that UV Tape B is highly suitable for the full sandwich mounting technique, supporting both process cleanliness and die reliability. This superior performance suggests that UV Tape B is a strong candidate for high-volume manufacturing environments that demand consistent and efficient tape removal without compromising wafer or die quality.

(a) (b)

Figure 4.5: UV Tape B with 100% manual peeling results (a) low magnification (b) zoom area on the wafer surface

4.2.2 Evaluating surface mounting tape removal through UV curing dosage optimization

To establish the double-sided mounting technique in production mode, it is vital to ensure that the surface mounting tape removal can be done according to the standard manufacturing process flow. This evaluation aims to replace the manual peeling with an automatic peeling during wafer cleaning process. To proceed with the assessment of the double-sided wafer mounting process, UV Tape B with the lowest (30 mN/25mm) adhesion was selected because of the 100% peeling results of the manual surface mounting tape peeling test performed earlier. The UV curing parameters must be optimizes to ensure optimal adhesion during the wafer cleaning process and reduces the possibility of chipping during the die pick up process.

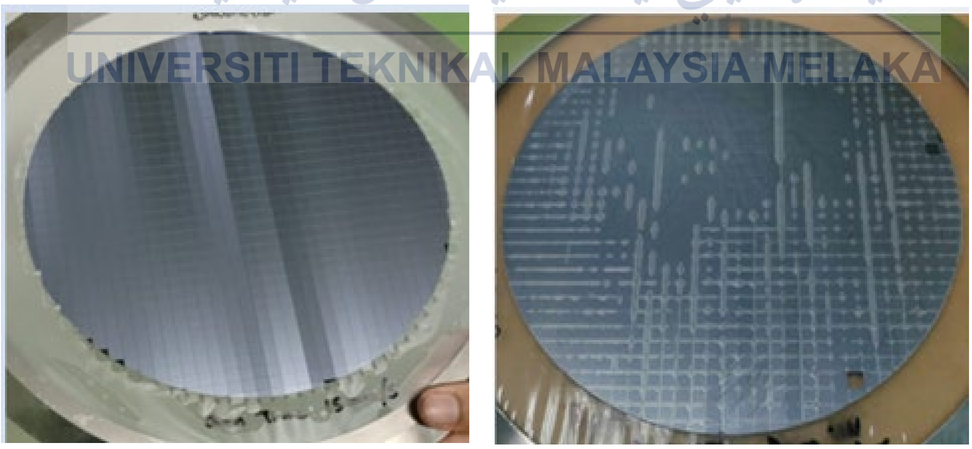
The standard UV curing process during the evaluation of manual peeling test process is based on a UV irradiation speed of 15mm/s, which produced a UV dosage of 552 mJ/cm^2, which the result previously unable to completely remove the surface mounting tape during the wafer cleaning process. Two additional UV irradiation parameters, 10 mm/s and 5 mm/s, were assessed in order to generate a higher UV curing dosage during the UV curing process. This will probably contribute to a reduction in surface tape gripping, which is expected to be eliminated during the wafer cleaning process. The 10 mm/s UV irradiation speed setting resulted in a medium UV dosage of 827 mJ/cm^2 and 5 mm/s produced 1653 mJ/cm^2 the highest UV dosage. Table 4.2 presents the outcomes of increased UV dosage on the elimination of surface mounting tape during the wafer cleaning procedure. Take note that the optimization was done based on the surface wafer area only while the backside UV curing curing parameters area remains the same.

Table 4.2: Results of UV dosage evaluation on surface mounting tape removal based on UV Tape B

Mounting Tape	**UV Parameter**	**Min / Standard Setting**	**Med Setting**	**Max Setting**
Surface mounting tape	UV irradiation speed	15 mm/sec	10 mm/sec	5 mm/sec
	Exposure dose	552 mJ/cm^2	827 mJ/cm^2	1653 mJ/cm^2
Backside mounting tape	UV irradiation speed	43.3 mm/s		
	Exposure dose	190 mJ/cm^2		
Yield of surface mounting tape removal through the wafer cleaning process		0%	100 %	100% but with flying die

The parameters for maximum, medium, and minimum UV settings are defined based on the UV irradiation speed and the corresponding exposure dose applied to the surface mounting tape during UV curing. A slower irradiation speed, results in a higher exposure dose as the tape receives more UV energy over time. Therefore, the maximum setting is defined at 5 mm/sec, producing the highest exposure dose of 1653 mJ/cm^2**.** The medium setting is set at 10 mm/sec, delivering a moderate exposure dose of 827 mJ/cm^2**.** Meanwhile, the minimum or standard setting is defined at 15 mm/sec, resulting in the lowest exposure dose of 552 mJ/cm². These settings are designed to control the tape's adhesion release characteristics for the surface mounting only, where higher doses typically weaken the adhesive strength more effectively, which is to be removed during the wafer cleaning process. The backside mounting tape uses the same parameter since it represents the function to hold the die during dicing and reducing the adhesion after UV curing for the pick and place process.

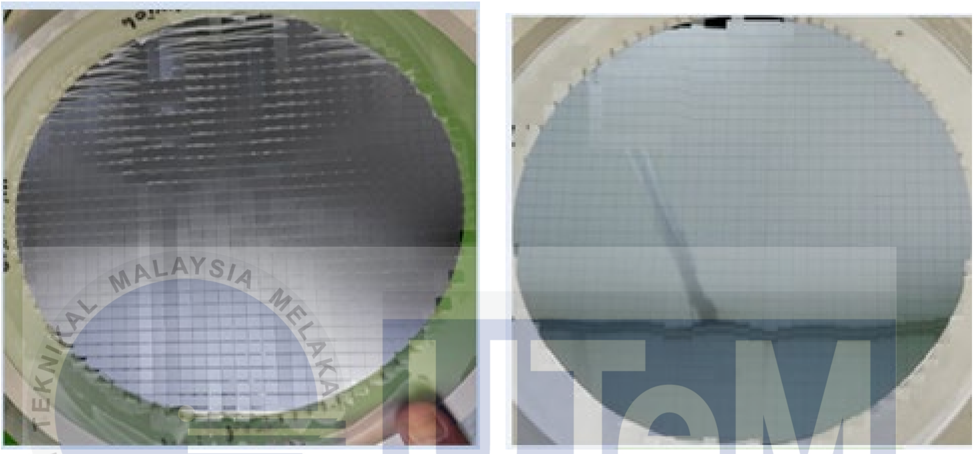
Table 4.2 indicates that the UV curing parameters, such as the UV irradiation speed and exposure dose, are crucial in the effectiveness of surface mounting tape removal during the wafer cleaning process. At the highest UV irradiation speed (15 mm/sec) and lowest UV dosage (552 mJ/cm²), it produced a negative result of 0% yield of surface tape removal, indicating insufficient curing for the surface tape detachment as shown in Figure 4.6(a). With 552 mJ/cm², it produced the lowest UV dosage, which made the surface UV mounting could not be removed even after wafer cleaning as per Figure 4.6(b).



(a) (b)

Figure 4.6: 15 mm/sec UV irradiation speed results (a) wafer after UV curing (b) wafer after UV curing and cleaning process

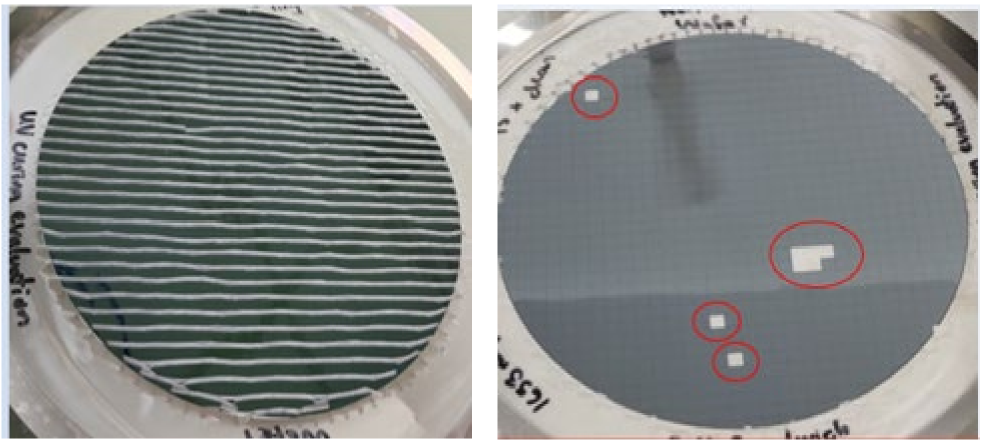
The medium setting with UV irradiation speed of 10 mm/sec, which produced a UV dosage of 827 mJ/cm², developed a slight wrinkle on UV surface mounting tape after the curing process, as shown in Figure 4.7(a). Results show complete 100% tape removal in Figure 4.7(b), which is currently the best result and ideal for the double-sided wafer mounting technique application.



(a) (b)

Figure 4.7: 10 mm/sec UV irradiation speed results (a) wafer after UV curing (b) wafer after UV curing and cleaning process

At the lowest UV irradiation speed (5 mm/sec) and maximum UV dosage (1653 mJ/cm²), it produced the highest UV tape wrinkles on the surface UV tape as shown in Figure 4.8(a). The highest wrinkles on the surface UV tape is caused by the highest UV dosage applied to the surface which achieves 100% surface tape removal too however, it induces "flying die" problems and it is likely due to excessive adhesion reduction, which is not able to hold the die firmly during the cleaning process as shown in Figure 4.8(b).



(a) (b)

Figure 4.8: 5 mm/sec UV irradiation speed results (a) wafer after UV curing (b) wafer after UV curing and cleaning process

The term "flying die" describes a condition where individual dies become detached and are unintentionally washed away during the wafer cleaning process, leading to overall quantity reduction and yield loss. A similar observation was reported by Marko Omazic (2017), who found that UV dosage is directly proportional to the reduction in mounting tape adhesion. Based on this study, a medium UV irradiation speed setting of 10 mm/sec was identified as optimal, as it provides sufficient exposure to ensure complete surface tape removal during wafer cleaning while minimizing the risk of flying dies.

4.2.2.1 Peeling test results on UV Tapes using tensile strength machine

Further verification was executed by performing a peeling test on UV curing tape (UV Tape A and UV Tape B) based on 15 mm/s and 10 mm/s UV irradiation speed using a tensile strength machine Tensilon RTG-1210. This data supports the positive results based on the UV curing parameter that managed to remove the surface mounting tape based on 10 mm/s UV irradiation speed. A peeling test was performed at a 180-degree angle, and the results are displayed in Figure 4.9.

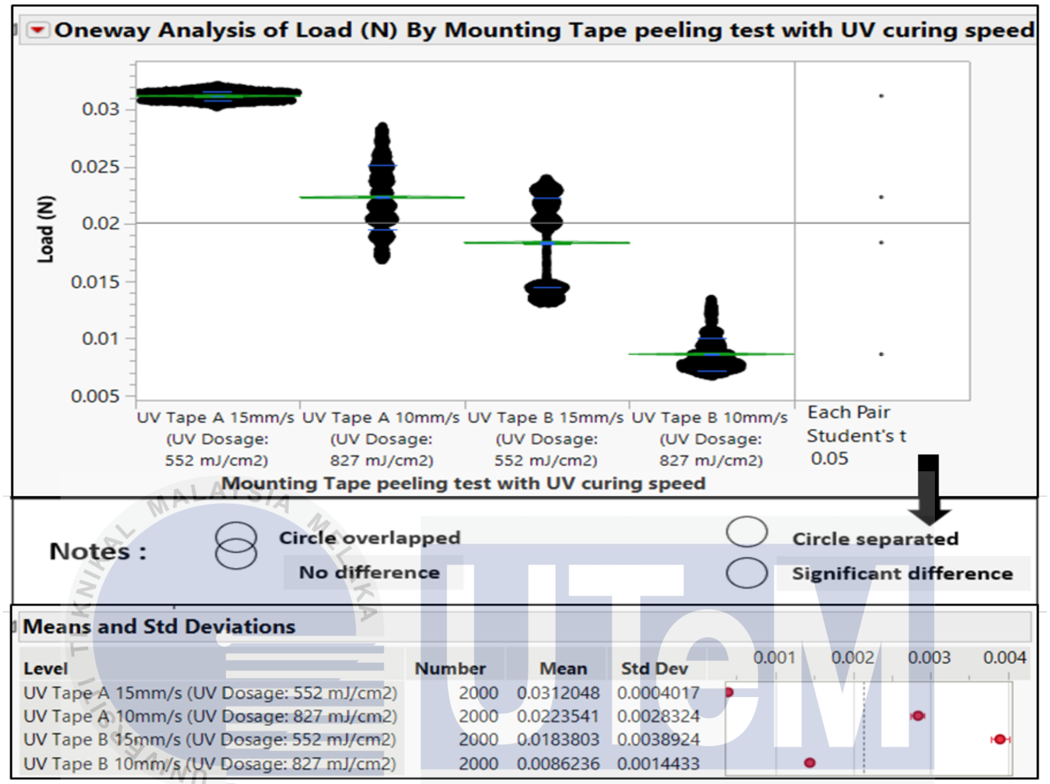


Figure 4.9: Peeling test results on UV Tape A and UV Tape B

The results demonstrated that a lower UV irradiation speed of 10 mm/s resulted in a higher UV dosage of 827 mJ/cm², which consequently led to the lowest peeling test values for both UV Tape A and UV Tape B. However, a detailed evaluation of the peeling test revealed that UV Tape B exhibited the lowest peeling test results under the same UV irradiation conditions (10 mm/s). These findings suggest that the surface mounting tape, particularly UV Tape B, may undergo automatic removal during wafer cleaning due to its minimal peeling strength. This outcome aligns with the UV curing optimization process, indicating that the optimized curing parameters significantly influence the adhesion characteristics of the mounting tape and successfully remove the surface mounting tape during the wafer cleaning process.

The use of mean and standard deviation as performance parameters in the mounting tape peeling test is crucial for evaluating both the effectiveness and consistency of the UV curing process. The mean represents the average load required to peel the tape, providing a clear indication of the adhesive strength under different UV curing speeds and dosages. This allows for direct comparison between conditions, such as different tape types and curing settings. Meanwhile, the standard deviation measures the variability of the data, indicating the stability of the peeling force is within each group. A lower standard deviation suggests more stable performance, which is desirable in semiconductor manufacturing where process stability is critical. Additionally, the application of statistical analysis, such as the Student's t-test and visual circle plots, supports the identification of significant differences between groups. Overall, the mean and standard deviation together offer a comprehensive understanding of both the central tendency and dispersion, enabling informed decisions about the optimal UV curing parameters for reliable tape performance.

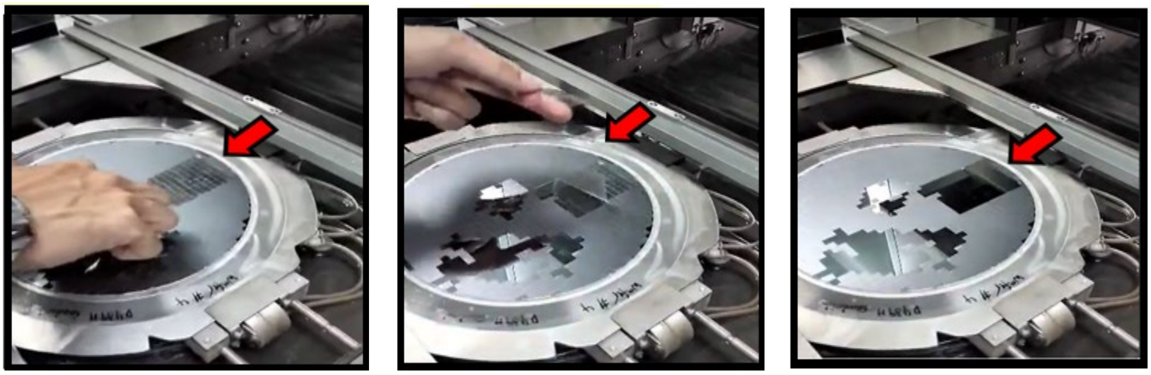
4.2.3 Mounting techniques vs chipping performance

Meeting topside and backside chipping acceptance criteria is essential in developing a double-sided wafer mounting technique to ensure high-quality die integrity and yield. Adhering to these criteria minimizes defects affecting the wafer's structural integrity and device functionality. Topside chipping can interfere with electrical performance, while backside chipping can weaken the die and produce cracks, leading to breakage during processing or assembly. By controlling chipping on both sides, the technique supports improved handling, reliable die release, and successful downstream processing. This reduces rework and increases production efficiency, making it suitable for high-volume manufacturing and enhancing product reliability.

To achieve the first objective, the chipping results must be lower than the conventional single-sided wafer mounting technique otherwise the implementation of the double-sided mounting technique is not worth it. Since the UV curing had been optimized for the surface mounting tape removal through the wafer cleaning process, there were three mounting techniques will be assessed to develop the double-sided wafer mounting technique. As mentioned in the methodology section, the double-sided semi and full sandwich wafer mounting chipping performance will be compared to the single-sided conventional mounting technique to see the effectiveness. The chipping performance then being compared according to manual peeling and automatic peeling through a wafer cleaning process to see which produced better results.

4.2.3.1 Topside chipping performance

The automatic peeling process was developed to replace the existing manual peeling process, which is unsuitable for a production environment. The existing manual peeling was based on 15 mm/s UV irradiation speed, as the surface mounting tape remains on the wafer surface which requires a manual peeling process as shown in Figure 4.10 before the chipping measurement can be done. The manual peeling process requires lots of manual handling, which is critical since it is human dependent and the process took 5 minutes per wafer for completion. The process steps were illustrated based on Figure 4.10.



(a) (b) (c)

Figure 4.10: Manual peeling process (a) Place cellophane tape on surface mounting tape (b) Pull up the cellophane tape (c) surface mounting tape peels off

The objective of developing the automatic peeling process is to remove the surface mounting tape automatically during the wafer cleaning process through UV curing optimization as shown in Figure 4.11. The automatic peeling process had been successfully developed from previous activity by identifying 10 mm/s as the best UV curing speed setting. The overall peeling process improved the removal of surface mounting tape time from 5 minutes per wafer to 30 seconds per wafer, which the process included in the wafer cleaning time and does not impact additional manufacturing time.

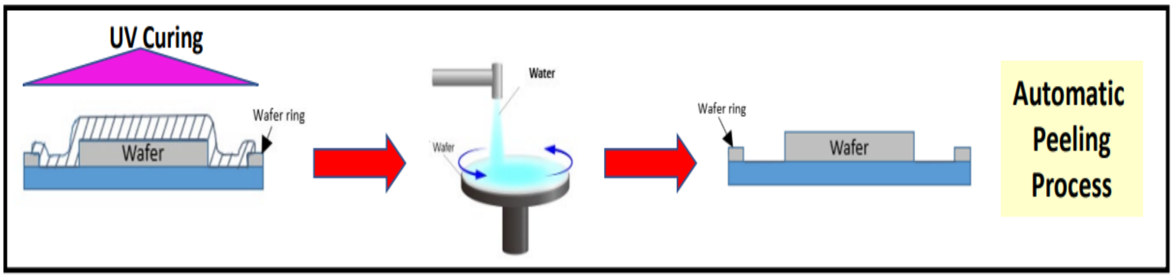
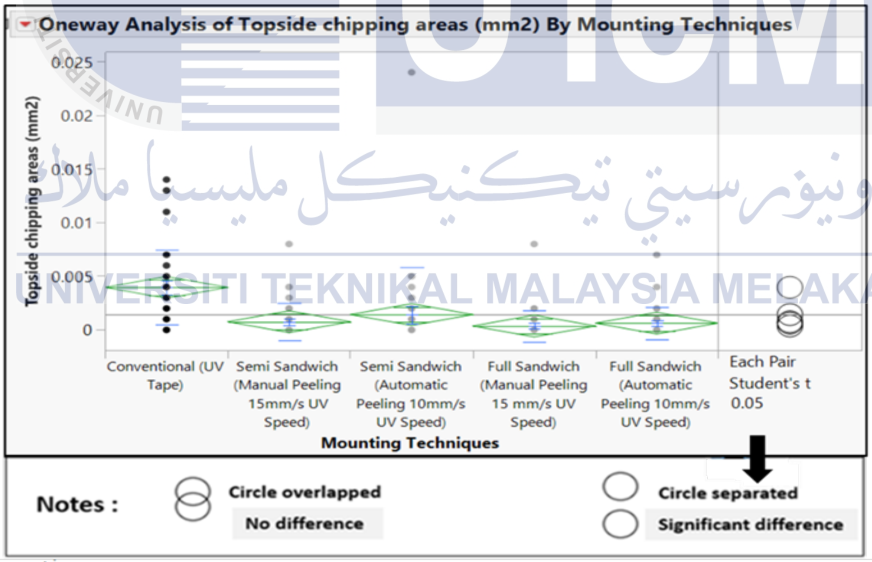


Figure 4.11: Illustration of the automatic peeling process

Upon successful development of the surface mounting tape automatic removal, chipping measurements were subsequently conducted to evaluate and monitor the overall chipping performance of the wafer during the dicing process. Figure 4.12 presents the results of the topside chipping statistical analysis based on the automatic peeling process. The surface mounting tape was then removed automatically during the wafer cleaning process before the chipping measurements were taken. The analysis highlights significant reductions in topside chipping towards the implementation of double-sided wafer mounting in comparison with the conventional single-sided wafer mounting technique based on the circle separation in the Each Pair Student's test column. The one-way analysis of variance (ANOVA) results presented in the graphical representation indicate significant variations in chipping performance across the three evaluated methods.



Means and Std Deviations

Level	Number	Mean	Std Dev
Conventional (UV Tape)	30	0.0039667	0.0034887
Semi Sandwich (Manual Peeling 15mm/s UV Speed)	30	0.0007667	0.0017555
Semi Sandwich (Automatic Peeling 10 mm/s UV Speed)	30	0.0014333	0.0044542
Full Sandwich (Manual Peeling 15 mm/s UV Speed)	30	0.0003667	0.0014967
Full Sandwich (Automatic Peeling 10 mm/s UV Speed)	30	0.0006333	0.0015196

Figure 4.12: Topside chipping performance between single-sided and double-sided wafer mounting techniques

The comparative statistical analysis presented in the one-way analysis of variance (ANOVA) investigates the effect of different wafer mounting techniques on topside chipping areas (mm^2). The results indicate a statistically significant reduction in chipping area when the double-sided semi and full sandwich wafer mounting techniques are employed in comparison to conventional single-sided UV tape wafer mounting techniques.

The statistical significance of these findings is confirmed through the Student's t-test at a 0.05 significance level, where non-overlapping circles indicate significant differences between conventional single-sided wafer mounting and the double-sided wafer mounting techniques. The substantial reduction in the topside chipping area in both semi-sandwich and full-sandwich configurations suggests that these mounting approaches provide enhanced cushioning effects by the surface mounting tape and minimize mechanical stress during the wafer dicing process which demonstrates the topside chipping mitigation.

The analysis of topside chipping areas across different wafer mounting techniques revealed that the conventional method using UV tape resulted in the highest average chipping area (0.0039667 mm^2). In contrast, the full sandwich mounting technique with automatic peeling and an optimized UV irradiation speed of 10 mm/s achieved the lowest mean chipping area (0.0006333 mm^2), representing a significant reduction of approximately 84%. The statistical comparison using Student's t-test at a 0.05 significance level showed that the chipping areas for the full sandwich configurations were significantly lower than the conventional method, as indicated by the separation of circles in the pairwise comparison plot. These findings confirm the effectiveness of the novel full sandwich technique in minimizing topside chipping during wafer dicing.

Further verification of topside chipping was conducted using Scanning Electron Microscopy (SEM) to obtain a detailed visual representation of each chipping site and to inspect the occurrence of cracks. The results, presented in Figure 4.13, provide critical insights for analysis. From the SEM images, it can be seen that the conventional single-sided wafer mounting technique has the highest chipping behaviour compared to the double-sided wafer mounting technique which has the same correlation with the ANOVA results. From all the images there is no crack observed on all runs however for the conventional single-sided wafer mounting technique it is obvious that the chipping is much higher due to there is no tape on the surface for the cushioning effect when the diamond blade starts to hit the brittle silicon wafer.

The ANOVA statistical analysis indicates that the topside chipping performance remains consistent across the double-sided wafer mounting techniques, irrespective of whether the peeling process is conducted manually at a UV curing speed of 15 mm/s or automatically at 10 mm/s. This finding suggests that the mounting tape applied to the wafer surface serves as the primary factor in absorbing vibrations generated by the dicing blade, thereby stabilizing the singulation process and mitigating topside chipping performance.

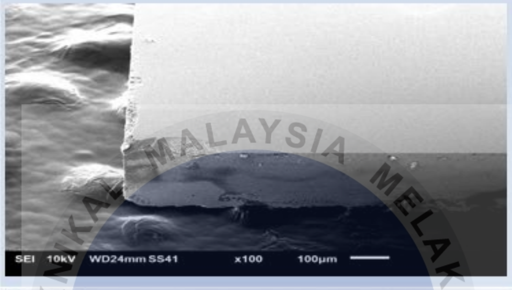
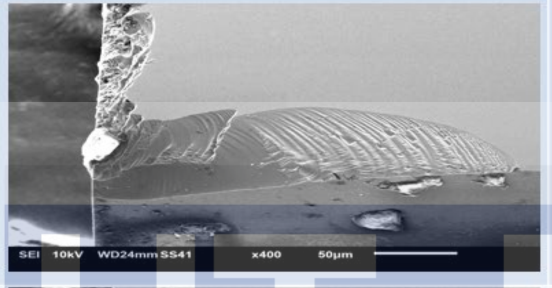
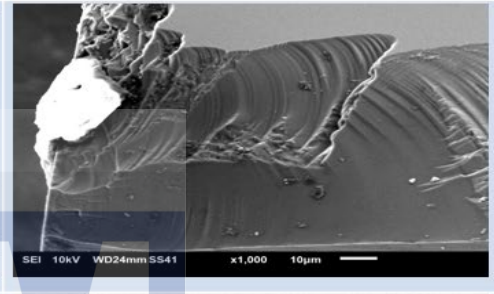
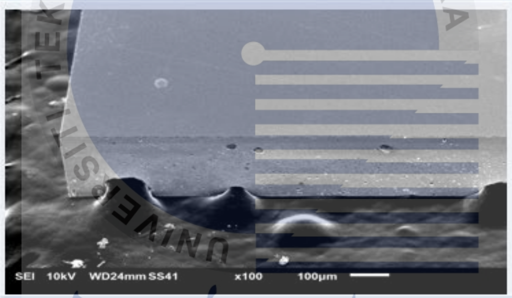
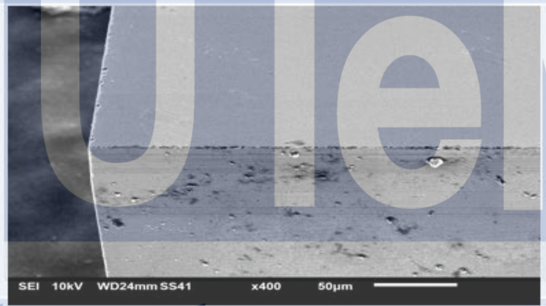
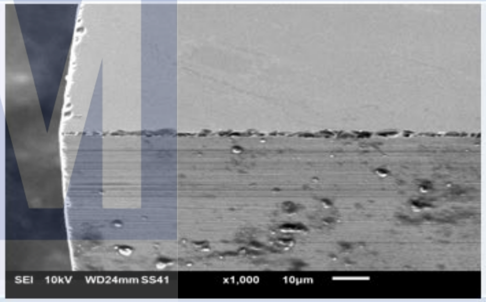
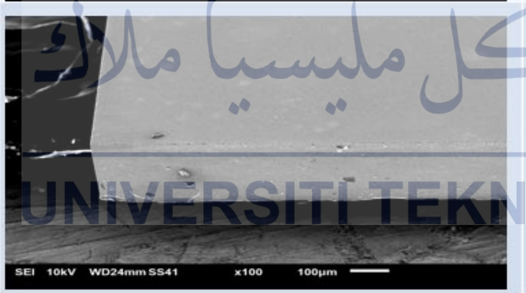
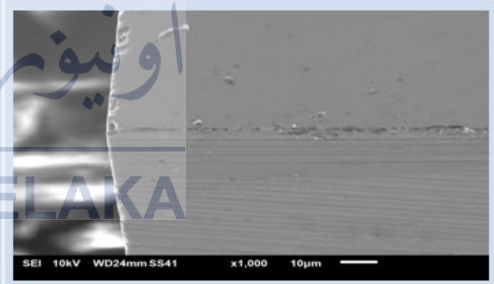
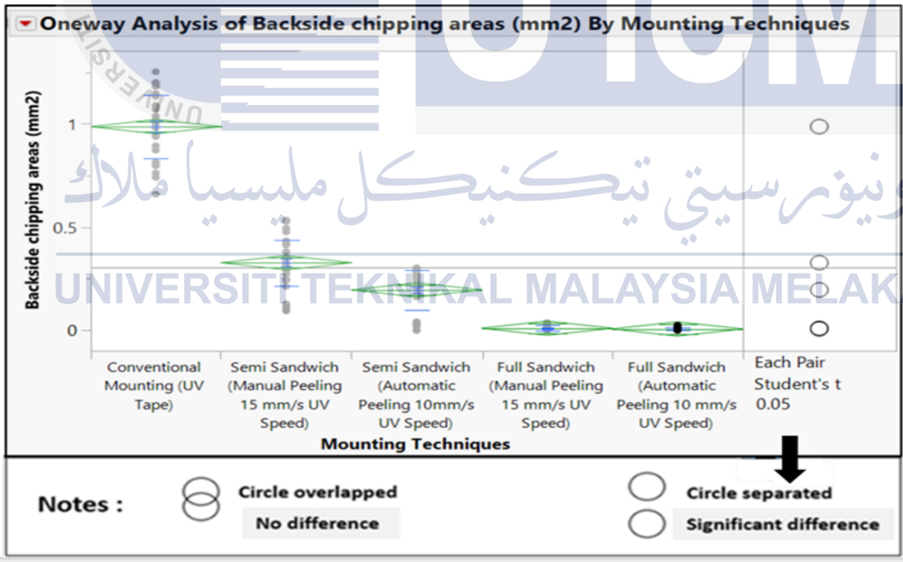
Wafer Mounting Techniques	100 X	400 X	1000 X
Conventional (Topside chipping)			
Semi Sandwich (Topside chipping)			
Full Sandwich (Topside chipping)			

Figure 4.13: SEM image on the topside areas

4.2.3.1 Backside chipping performance

The backside chipping performance was evaluated to determine its impact on overall chipping performance. The overall backside chipping performance was combined based on an initial 15 mm/s and optimized 10 mm/s UV curing speed which is shown in Figure 4.14. Results showed the conventional single-sided mounting technique produced the highest backside chipping performance, followed by semi sandwich double-sided wafer mounting and the full sandwich wafer mounting technique developed the lowest backside chipping performance. The same observation reported by Aiza Marie and Bryan Christian (2021), which the application of mechanical dicing based on the conventional single-sided wafer mounting process developed mechanical stress causing high backside chipping which may induce higher crack issues.



Means and Std Deviations

Level	Number	Mean	Std Dev
Conventional Mounting (UV Tape)	30	0.9867667	0.1550163
Semi Sandwich (Manual Peeling 15 mm/s UV Speed)	30	0.328	0.1102852
Semi Sandwich (Automatic Peeling 10mm/s UV Speed)	30	0.1967	0.0960309
Full Sandwich (Manual Peeling 15 mm/s UV Speed)	30	0.0112667	0.0140882
Full Sandwich (Automatic Peeling 10 mm/s UV Speed)	30	0.0075333	0.0064793

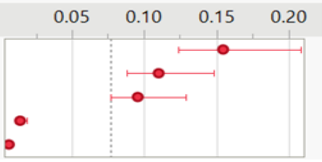


Figure 4.14: Backside chipping performance between single-sided and double-sided wafer mounting techniques

The analysis of backside chipping areas across various wafer mounting techniques revealed that the conventional method using UV tape exhibited the highest average chipping area at 0.9868 mm². In contrast, the full sandwich mounting technique with automatic peeling and 10 mm/s UV irradiation speed achieved the lowest average backside chipping at 0.0075 mm², representing a chipping reduction of more than 84%. The results from the Student's t-test at a 0.05 significance level indicate statistically significant differences between the conventional and full sandwich double-sided wafer mounting techniques. Overall, the full sandwich method demonstrated superior performance in minimizing backside chipping, establishing its effectiveness as a novel improvement over traditional mounting approaches.

The double-sided full-sandwich wafer mounting technique consistently demonstrated the lowest backside chipping across both UV curing speeds of 15 mm/s (manual) and 10 mm/s (automatic). This superior performance can be attributed to the extended surface coverage of the mounting tape, which extends to the wafer ring area, thereby providing enhanced structural support and additional gripping performance as per the illustration in Figure 4.15.

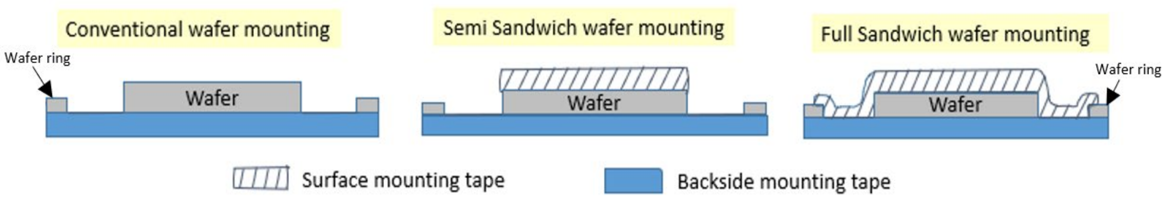


Figure 4.15: Illustration of mounting techniques toward wafer cushioning and gripping performance

It is observed that the conventional mounting does not have mounting tape on the wafer surface. This expected leads to significantly higher vibration during the dicing process and results in the highest chipping due to no support given to the wafer from the surface but only from the backside of the wafer. According to Au-Zou Tai, the vibration is the critical aspect of the wafer dicing equipment from the high-speed spindle rotation including the motion of the x,y and z-axis operation which may affect the chipping performance (Tai and Fang, 2023). Nevertheless, in Tai's research did not specify a vibration level to comprehend the behaviour concerning the generation of the elevated backside chipping starting points. Therefore it is important to have vibration data to support the statements which will be conducted at the end of the research.

To further validate the topside chipping characteristics, Scanning Electron Microscopy (SEM) analysis was performed to obtain a detailed visual representation of each chipping site and to examine the presence of cracks. The results, as illustrated in Figure 4.6, offer essential insights for comprehensive analysis. The SEM image of the backside chipping represents the ANOVA statistical data from Figure 4.16 which shows the conventional single-sided wafer mounting has the highest backside chipping, followed by double-sided semi sandwich wafer mounting and double-sided full sandwich wafer mounting technique has the lowest backside chipping performance.

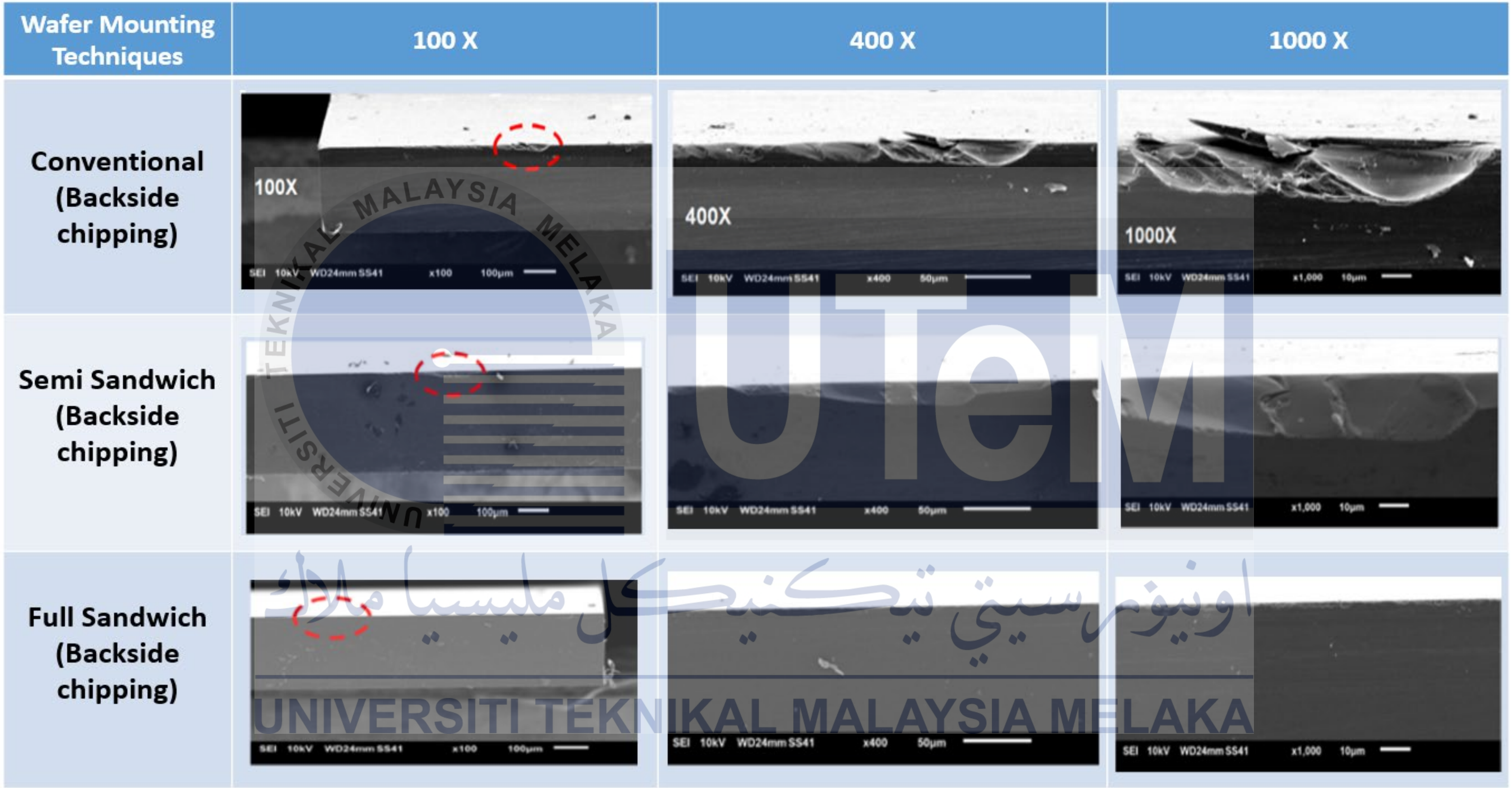
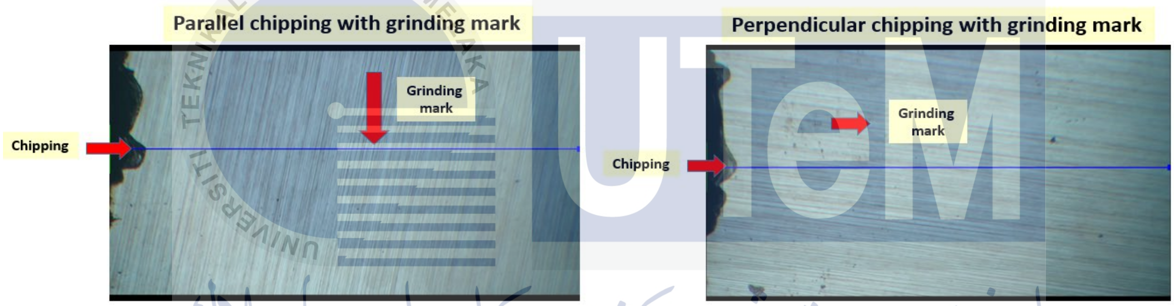


Figure 4.16: SEM image on backside areas

4.2.4 Die backside topography measurement

Since the first objective is to evaluate the double-sided wafer mounting performance towards non-polish backside silicon wafers, it is very important to understand the die backside behaviour. Given the presence of grinding marks on the back of the silicon wafers, it is crucial to understand whether these marks orientation impact the chipping performance. Two types of chipping in relation to the grinding marks were observed and were analzsed. The dies after dicing process were pick-up using plastic tweezer and observed it has backgrinding marks consist of parallel and perpendicular chipping, as illustrated in Figure 4.17.



(a) (b)

Figure 4.17: Grinding marks patterns (a) Parallel with chipping (b) Perpendicular with chipping

An analysis was conducted to examine the impact of parallel and perpendicular grinding marks on surface roughness and their respective contributions to chipping behaviour. To evaluate the performance of two types of chipping concerning grinding marks, the arithmetical mean roughness value (Ra) was analyzed. The arithmetical mean roughness value (Ra) represents the average of absolute deviations from the mean line of a surface's profile as illustrated in Figure 4.18.

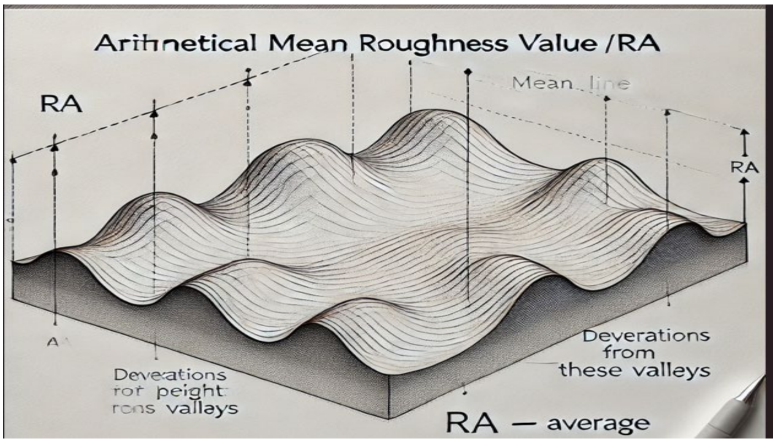
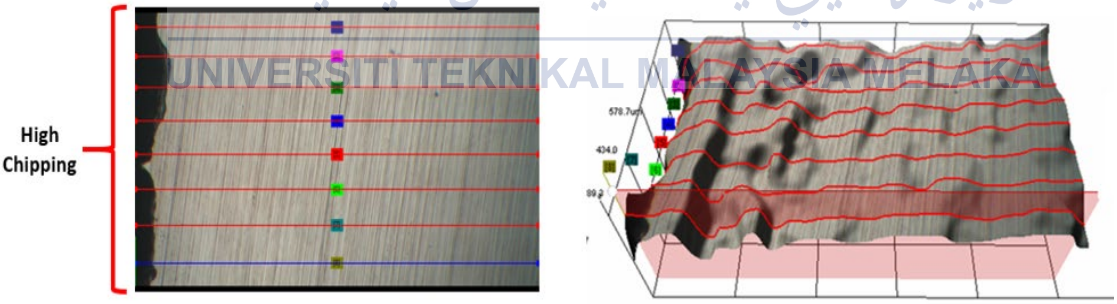


Figure 4.18: Arithmetical mean roughness value (Ra) illustration

It quantifies surface roughness by calculating the average height of peaks and valleys across a measured area, making it a standard parameter for assessing surface texture in engineering and manufacturing. The metric Ra represents the average value of surface roughness. Subsequently, the chipping data associated with parallel grinding marks on the silicon die, as shown in Figure 4.19, were examined.

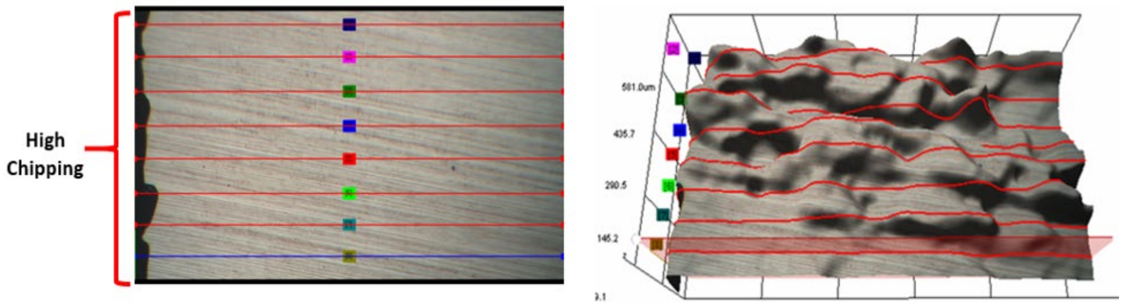


(a) (b)

Figure 4.19: High chipping area surface roughness with parallel grinding marks

(a) Bottom view (b) Bottom topography view

Next, the chipping data corresponding to perpendicular grinding marks were analyzed, as illustrated in Figure 4.20.

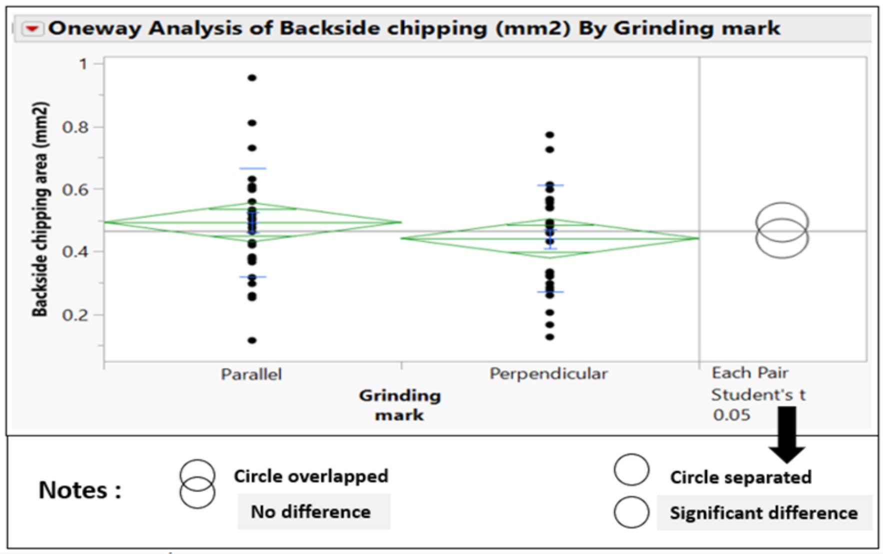


(a) (b)

Figure 4.20: High chipping area surface roughness with perpendicular grinding marks

(a) Bottom view (b) Bottom topography view

A statistical T-Test was conducted on 30 samples to investigate the potential impact of grinding marks towards the backside chipping area correlation. A T-test is a statistical method used to compare the means of two groups to determine if there is a significant difference between them. It helps assess whether observed differences are due to actual effects or random variation. The statistical significance was determined using a T-test with $\alpha = 0.05$.



Means and Std Deviations

Level	Number	Mean	Std Dev
Parallel	30	0.4931	0.1716949
Perpendicular	30	0.4415	0.1695541

Figure 4.21: T-Test results on parallel and perpendicular chipping towards grinding marks

The analysis presented in Figure 4.21 examines the correlation between the backside chipping area and grinding mark orientation, specifically comparing parallel and perpendicular grinding marks. The results indicate no statistically significant difference in chipping performance between the two orientations, suggesting that the direction of grinding marks does not influence backside chipping. These findings imply that other factors, such as wafer mounting techniques and dicing parameters, may have a more substantial impact. However, the dicing parameters were fixed in this activity and the only contribution to backside chipping performance is the wafer mounting techniques.

Similar findings regarding the chipping edge size which does not depend on the crystal orientation and the grinding mark in the study by Shang Gao (2013). The results from this study are consistent with those findings, indicating no significant discrepancies between the data sets. Since the grinding mark pattern does not have a significant impact towards the chipping behaviour, a total of 30 samples were then collected for the conventional, semi, and full sandwich wafer mounting techniques with random grinding mark patterns. These samples underwent a 3-point bending test to examine any potential correlation between chipping behavior and die flexural strength performance.

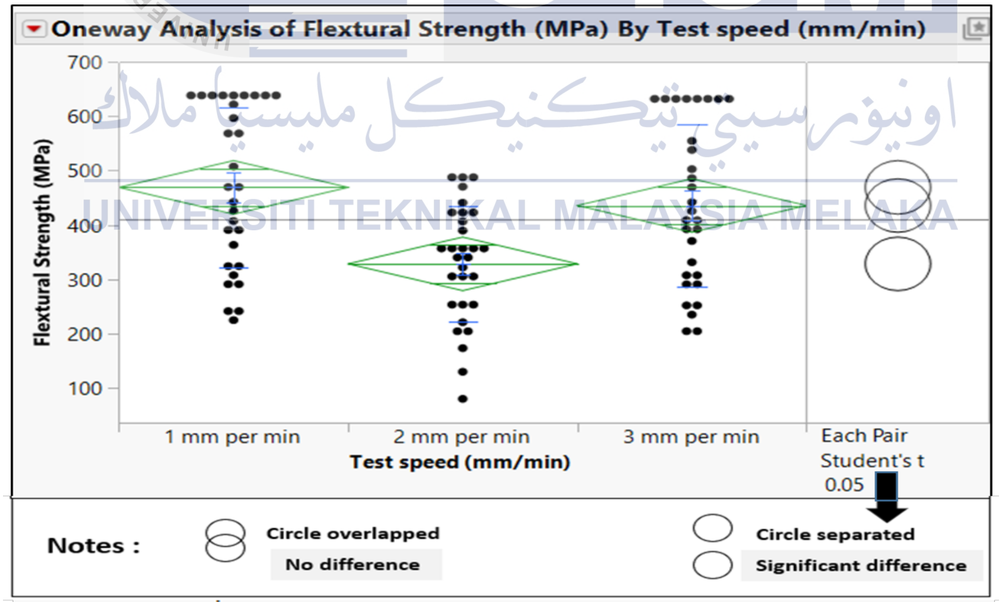
4.3 Three-point bending test

Since the double-sided wafer mounting had been successfully developed, then the second objective is to evaluate the three-point bending test on each mounting technique. The 3-point bending test is essential for evaluating the mechanical strength and fracture resistance of silicon dies, which are widely used in semiconductor manufacturing. It measures flexural strength by generating force at the middle point, supported at both ends, to simulate the applied stress. Silicon dies, due to their brittleness, are susceptible to cracking and fracturing under mechanical stress. This test assesses their resistance to bending and yields essential data for relating with the wafer mounting techniques and chipping performance, which is vital for semiconductor manufacturing applications. Furthermore, it facilitates the comparison of various processing processes and materials to enhance reliability and performance in electronic devices.

To test the three-point bending test, the setup preparation was according to the SEMI G86-0217 standard whereby it mentioned the test speed setting should be less than 5 mm/min. Test speed is crucial in the three-point bending test for silicon dies because it affects stress distribution, crack propagation, and material behaviour. Too fast or too slow on the test speeds can introduce errors during testing. Controlled speeds ensure accurate flexural strength measurements and comply with standards, providing reliable insights into the brittle failure mechanisms of silicon under realistic conditions. Before the three-point bending test was executed, an assessment was conducted to determine the optimal test speed. Due to the limited availability of samples for the destructive test, only three speed evaluations could be conducted, with 30 samples per run.

4.3.1 Test speed assessment

The test speeds evaluated were 1 mm/min, 2 mm/min, and the final test speed of 3 mm/min, as discussed earlier before the speed was finalized. The test speed was fixed based on the results that demonstrated the highest flexural strength performance while maintaining the fastest process efficiency. This approach ensures the optimal setting for overall evaluation, enhancing consistency, reliability, and repeatability in testing. It also helps in determining the best process conditions for improved silicon die durability. The results of the test speed assessment, based on analysis of variance (ANOVA), was displayed in Figure 4.22.



Means and Std Deviations

Level	Number	Mean	Std Dev
1 mm per min	30	469.84003	145.94406
2 mm per min	30	329.58423	106.56101
3 mm per min	30	436.61863	149.46698

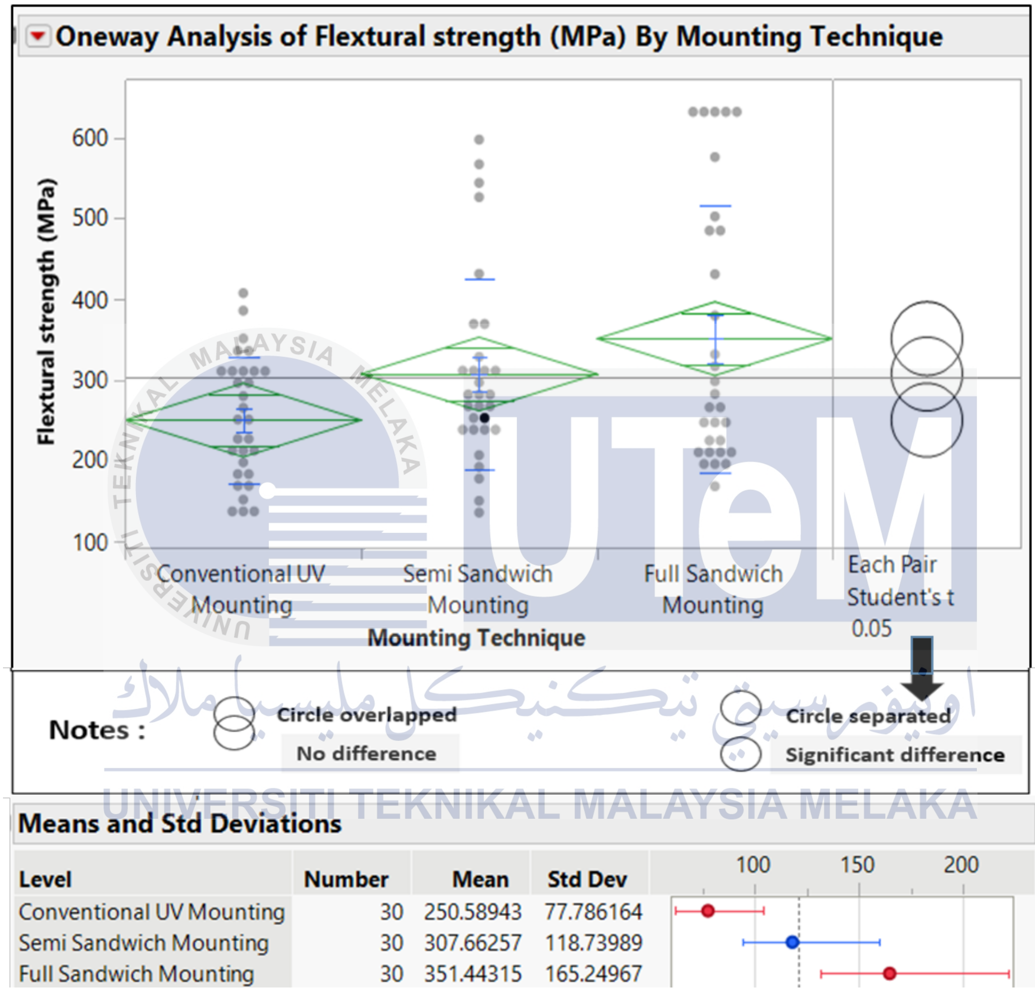
Figure 4.22: Test speed assessment results

The analysis of flexural strength (MPa) by test speed (mm/min) examines the effect of different testing speeds on the mechanical performance of silicon dies. Results showed that 1mm/min and 3 mm/min test speeds had significantly higher flexural strength results compared to 2 mm/min test speed. This is because the circle for 1mm/min and 3 mm/min were overlapped means they are no difference between them and both of the circles being separated with 2mm/min circle means the 1mm/min and 3mm/min are significantly higher than 2mm/min. The decision was to fix the test speed at 3 mm/min, as it given the optimum flexural strength reading with a higher speed performance. The higher speed will produce faster time for overall test completion since it involves high test samples for the overall evaluation. These findings highlight the importance of selecting an appropriate test speed for evaluating the silicon die strength. Optimizing test parameters ensures reliable strength characterization, improving semiconductor manufacturing processes and enhancing overall die reliability.

4.3.2 Three-point bending test on mounting techniques

After the test speed for the three-point bending test was fixed to 3 mm/min, the test was conducted on silicon dies using the conventional, semi, and full sandwich wafer mounting techniques to see the flexural strength performance. Flexural strength in a three-point bending test refers to the maximum stress a material can withstand on its surface at the point of failure during bending. It is a measurement of the material's ability to resist deformation under load and is crucial for brittle materials like silicon.

The test provides valuable insights into the material’s resistance to deformation and helps determine the most effective wafer mounting technique to improve overall die strength. By comparing different mounting techniques, this study aims to identify the most effective wafer mounting technique for minimizing mechanical failures during semiconductor manufacturing. The three-point bending test results will help to identify the effects of chipping towards the die strength as well by referring to each single wafer mounting technique. A total of 30 samples for each mounting technique were tested, and the results are shared in this section.



Level	Number	Mean	Std Dev
Conventional UV Mounting	30	250.58943	77.786164
Semi Sandwich Mounting	30	307.66257	118.73989
Full Sandwich Mounting	30	351.44315	165.24967

Figure 4.23: Flexural strength performance based on mounting technique with fixed 3mm/min test speed

Figure 4.23 displays the outcomes of flexural strength analysis for three wafer mounting methods: conventional UV mounting, semi sandwich mounting, and full sandwich mounting. Flexural strength is measured in Megapascal (MPa), and the data evaluates these approaches through a one-way analysis of variance (ANOVA) and paired Student's t-tests at a significant level p-value of 0.05. The overlapping circles indicate no statistically significant difference in flexural strength between conventional UV and semi-sandwich mounting procedures with both techniques exhibiting comparable mean values.

The flexural strength analysis revealed that the conventional UV mounting technique recorded the lowest average strength at 250.59 MPa, while the full sandwich wafer mounting technique exhibited the highest average strength at 351.44 MPa. This represents an approximate 40% increase in flexural strength, demonstrating the benefit of the double-sided mounting approach with lower chipping performance. These findings highlight that the full sandwich mounting technique not only improves chipping performance but also enhances the die strength of the silicon dies.

The double-sided full sandwich mounting technique demonstrates a significant difference in flexural strength relative to conventional wafer mounting, as indicated by the divergence of circles in the t-test results. Surprisingly, there were unexpected results for semi sandwich wafer mounting which showed it does not produce a significant difference between conventional and full sandwich wafer mounting techniques. However, the double-sided full sandwich wafer mounting technique demonstrated significantly higher flexural strength compared to the single-sided wafer mounting which was expected according to its lowest chipping performance.

The analysis showed the full sandwich double-sided wafer mounting technique has developed significantly the highest flexural strength performance in comparison with the single-sided conventional mounting technique. From the result, the full sandwich double-sided wafer mounting technique has produced positive outcomes which enhance durability, ensure reliability in applications involving mechanical loads, reduce the likelihood of IC failure and improve performance in demanding environments, particularly for brittle materials like silicon. This outcome is attributed to the complete coverage of the wafer surface by the mounting tape, which is assumed to reduce vibration during the dicing process. To validate this hypothesis, the third research objective focuses on confirming this observation through vibration analysis. Therefore, a comprehensive vibration study is conducted across all evaluated mounting techniques to verify the theoretical assumption and assess its impact on wafer stability and dicing performance.

4.4 Vibration analysis on mounting techniques

To address the third research objective, which aims to verify the chipping and flexural strength of each wafer mounting technique through vibration analysis, it is essential to conduct a comprehensive assessment of the vibrational characteristics associated with each technique. This requires an in-depth evaluation of the time and amplitude of vibrations generated during the wafer dicing process, as well as their correlation with the occurrence of chipping and variations in flexural strength. Figure 4.24 displays the vibration analysis results for the conventional single-sided wafer mounting technique, along with the double-sided semi and full sandwich wafer mounting techniques obtained from the piezoelectric film sensor.

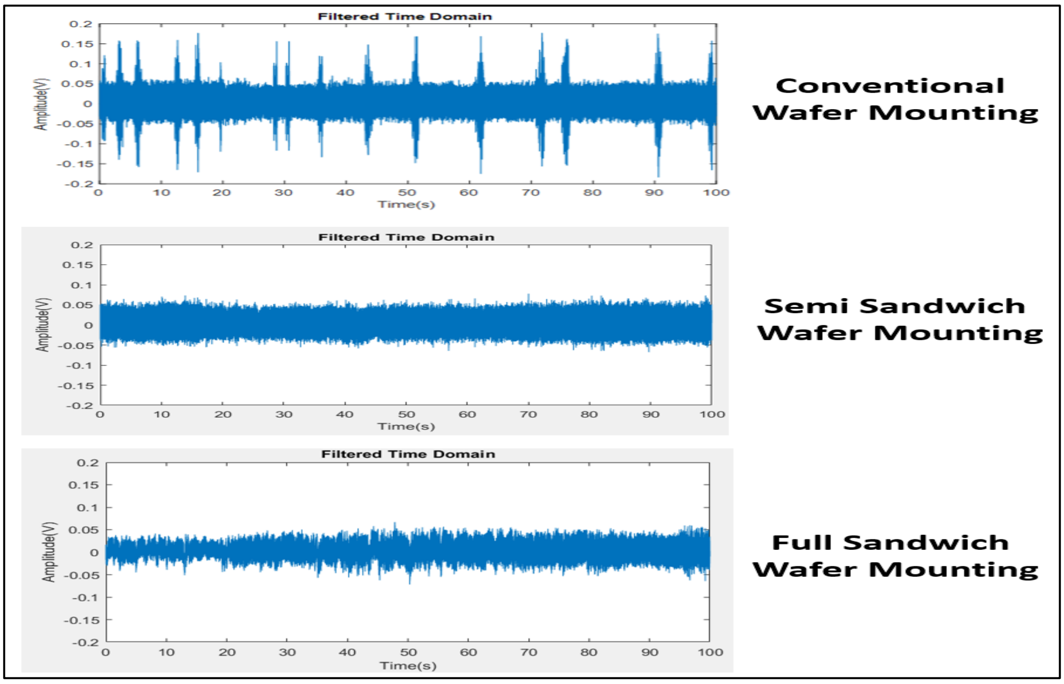


Figure 4.24: Compilation of wafer dicing vibration data on mounting techniques

The vibration data illustrates the impact of three wafer mounting techniques on amplitude consistency during the dicing process. Conventional wafer mounting exhibits the highest amplitude variations, indicating significant instability and vibration during wafer dicing. The semi-sandwich wafer mounting technique reduces amplitude fluctuations, offering improved stability compared to the conventional method. Notably, the full-sandwich wafer mounting demonstrates the lowest amplitude levels, signifying minimal vibration and enhanced stability. The reduction in vibration for the full-sandwich method represents higher die stability and lower cutting vibration, resulting in improved reliability and reduced chipping. Overall, the full-sandwich mounting technique provides superior vibration control during the dicing process.

To conduct a statistical analysis of the vibration signals, the recorded signals were transformed into 100 discrete values based on a 100-second duration wafer dicing process for each wafer mounting technique. The transformed dataset was subsequently subjected to statistical evaluation, with the analysis of variance (ANOVA) employed to compare the vibration performance across all wafer mounting techniques. The results of this analysis are presented in Figure 4.25, providing a quantitative assessment of the variations in vibrational characteristics among the different mounting approaches.

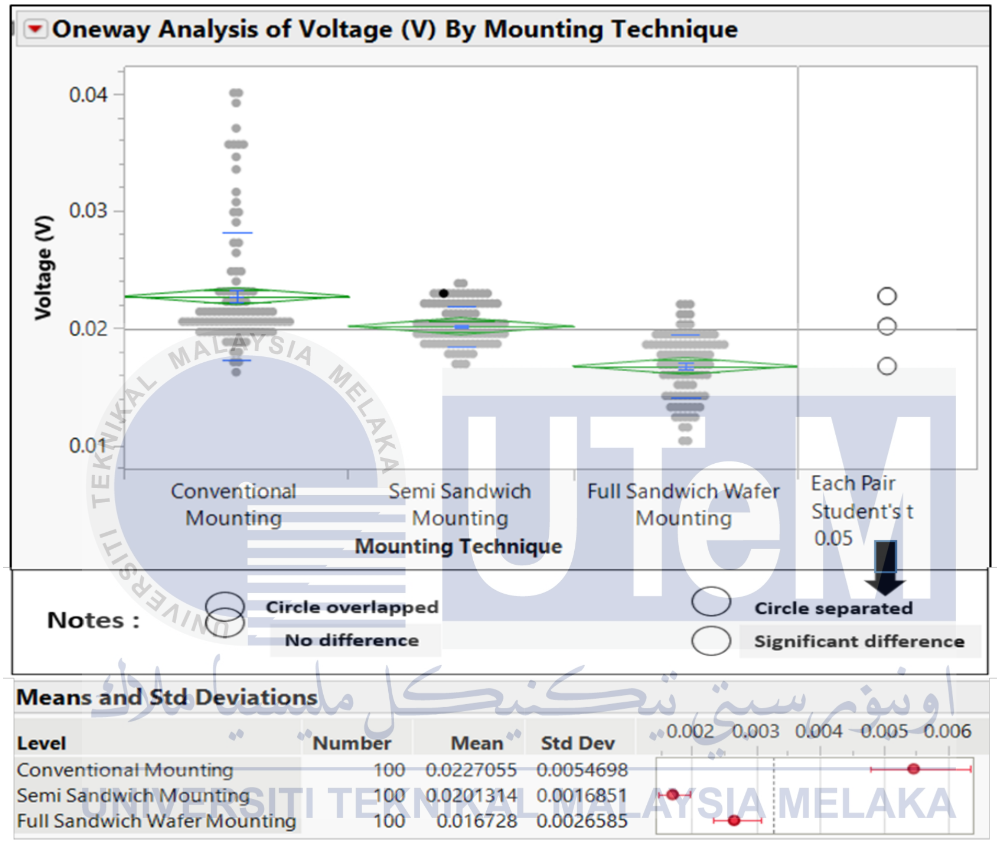


Figure 4.25: Wafer dicing vibration analysis on wafer mounting techniques

The ANOVA results indicate that the double-sided mounting techniques, such as the semi and full sandwich wafer mounting techniques, exhibited significantly lower vibration performance in comparison to the conventional single-sided mounting technique by referring to the circle separation in Each Pair Student's Test column. Notably, the double-sided full sandwich wafer mounting technique produced the lowest vibration performance among all mounting techniques and semi sandwich is the second lowest compared to the single-sided wafer mounting.

The vibration performance analysis in voltage demonstrated that the conventional UV mounting technique recorded the highest average vibration at 0.023 V, indicating significant mechanical instability during wafer dicing. In contrast, the full sandwich wafer mounting technique achieved a substantially lower average vibration of 0.017 V. This corresponds to a vibration reduction of approximately 26%.

In contrast, the conventional single-sided wafer mounting technique, which does not have mounting tape on the wafer surface, is shown to generate the highest vibration during wafer dicing. This leads to lower wafer holding instability, which is likely associated with the highest chipping performance and the lowest die flexural strength. The double-sided semi sandwich wafer mounting technique do not have full coverage mounting tape on the wafer surface which absorbs vibration in some areas and generates second lower vibration performance while full sandwich surface mounting tape covers all areas which absorbs more vibration area resulting in the lowest vibration performance among all wafer mounting techniques.

4.5 Summary

To enhance the wafer mounting technique, a full sandwich double-sided wafer mounting approach has been successfully developed. The application of surface mounting tape on the wafer surface has effectively mitigated both topside and backside chipping by offering cushioning effects and enhanced gripping stability. Furthermore, the surface mounting tape was successfully removed during the wafer cleaning stage, demonstrating its feasibility for immediate integration into production processes.

The reduction in chipping observed with the implementation of the full sandwich double-sided wafer mounting technique has also led to a significant enhancement in the flexural strength of the wafer. This is because lower chipping levels reduce the initiation sites for cracks, thereby improving mechanical durability. As flexural strength is directly related to the structural integrity of the die, this advancement is anticipated to improve overall device reliability, meeting industry performance and quality standards.

Additionally, vibration analysis was conducted to compare the single-sided and double-sided wafer mounting techniques during the wafer dicing process. This analysis is critical in understanding the root causes of excessive chipping and the occurrence of die cracks, which have been persistent issues in conventional single-sided mounting methods for over a decade. The findings revealed that single-sided mounting generates higher vibration levels during dicing, which strongly correlates with increased chipping. In contrast, the double-sided technique significantly reduced vibration, thereby improving both chipping resistance and flexural strength performance.

The chipping performance of the double-sided wafer mounting technique developed in this study cannot be directly compared with findings from other researchers due to differences in chipping measurement methodologies. While the current study quantifies chipping based on the total affected area in square millimetres (mm^2), other studies typically use linear measurements in micrometres (µm) to represent chipping length. Despite this discrepancy in measurement approaches, the primary objective of achieving reduced chipping performance was successfully met, as the results demonstrate a clear improvement in minimizing chipping, thereby supporting the effectiveness of the proposed technique.

CHAPTER 5

CONCLUSION AND FUTURE WORK

This chapter compiles and presents the key findings from the study, along with suggested directions for future research. Section 5.1 summarizes the achievements of the proposed research, as demonstrated by the experimental results. This section also discusses the connections between these achievements and the study's objectives. Section 5.2, the final section of the thesis, outlines several areas that could be further explored in subsequent research projects.

5.1 Conclusion

State-of-the-art wafer mounting necessitates the development of advanced processing methods to replace the conventional single-sided wafer mounting approach. The objective is to achieve minimal topside and backside chipping on the non-polished backside of silicon wafers. The key finding from this study indicates that the double-sided full-sandwich wafer mounting technique significantly reduces both topside and backside chipping, demonstrating superior performance compared to the conventional single-sided mounting method. This improvement is attributed to the additional UV mounting tape applied to the wafer surface, which provides a cushioning effect when the dicing blade contacts the wafer. Furthermore, the additional support at the wafer’s backside enhances stability during the dicing process, resulting in greater overall wafer stability and a significant improvement in chipping performance.

The double-sided full-sandwich wafer mounting technique then demonstrated the highest flexural strength performance compared to the conventional single-sided wafer mounting approach. This superior mechanical performance is attributed to the uniform support provided by the double-sided mounting configuration, which minimizes stress concentration and enhances the structural integrity of the silicon wafer. In contrast, the semi-sandwich wafer mounting technique exhibited inconsistent flexural strength measurements, indicating variability in its effectiveness. Such inconsistencies suggest that the semi-sandwich approach may not provide the necessary stability to achieve reliable mechanical reinforcement. Given these findings, the full-sandwich wafer mounting technique emerges as the preferred method for improving wafer robustness, ensuring minimal chipping and enhanced mechanical resilience. This advancement is particularly critical in semiconductor manufacturing, where wafer strength directly impacts the reliability of integrated circuits. The results highlight the necessity of adopting the full-sandwich technique for applications requiring high flexural strength and consistent mechanical performance.

The vibration analysis is very important in justifying early hypotheses by other researchers that higher vibration caused higher chipping and the engineering data had proven it. The double-sided full sandwich wafer mounting technique developed the lowest vibration performance during the wafer dicing process. It correlates with the lower chipping results and highest flexural strength performance. The lower vibration will cause higher stability during wafer dicing performance which helps semiconductor manufacturers improve their device robustness through the implementation of the double-sided full-sandwich wafer mounting technique.

In summary, the comparative analysis of wafer mounting techniques presented in Figure 5.1 underscores the critical impact of mounting configuration on wafer integrity during the dicing process. The conventional single-sided wafer mounting technique exhibits lower wafer holding power, resulting in increased vibration levels, which in turn lead to higher chipping rates and reduced flexural strength. In contrast, the full-sandwich double-sided wafer mounting technique significantly enhances wafer stability by providing superior holding power. This improvement translates into reduced vibration during dicing, leading to lower chipping defects and a substantial increase in wafer flexural strength. These findings highlight the necessity of adopting advanced wafer mounting strategies to mitigate mechanical stress and improve die robustness in semiconductor manufacturing. The enhanced structural integrity achieved through the full-sandwich double-sided wafer mounting technique contributes to greater reliability and performance of integrated circuits (ICs), reinforcing its potential as a preferred approach for minimizing defects and optimizing wafer processing efficiency.

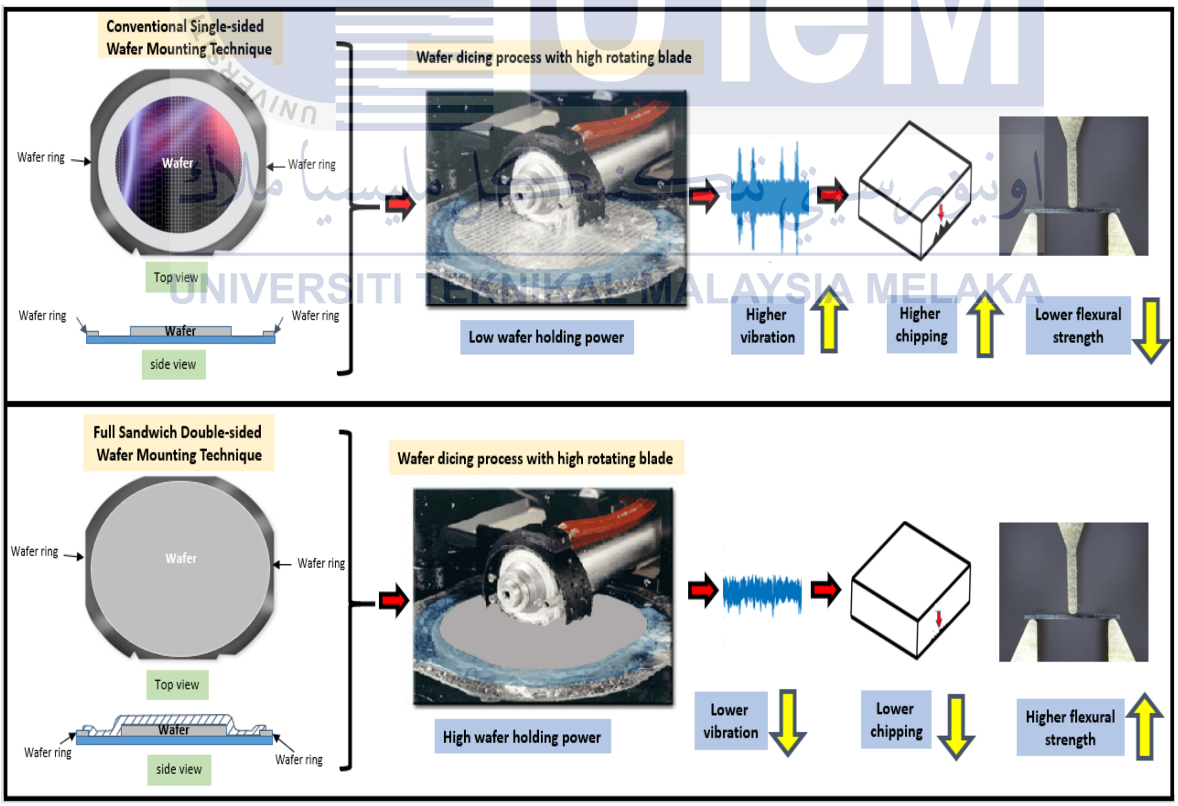


Figure 5.1: Single and double-sided wafer mounting techniques performance

5.2 Contribution to Research Work

The implementation of the double-sided full sandwich wafer mounting technique contributes significantly to advancing research in semiconductor manufacturing. Key contributions include:

i. **Silicon die chipping reduction:** The double-sided full sandwich wafer mounting method significantly minimizes topside and backside chipping by providing secure and stable wafer handling throughout the dicing procedure. The improved stability reduces mechanical stress on the wafer, resulting in a significant enhancement in device yield and overall product quality. This method effectively mitigates chipping issues, thereby improving the structural integrity of silicon wafers and leading to the manufacture of more reliable and defect-free semiconductor devices. As a result, embracing this approach provides substantial benefits for semiconductor manufacturing firms, facilitating economical production while ensuring they remain competitive in a challenging market.

ii. **Improved flexural strength:** The mounting method improves the flexural strength of silicon dies by effectively reducing mechanical stresses encountered during the handling and manufacturing process. The method enhances the die structure by reducing stress concentrations, thereby increasing its durability against mechanical loads and reducing the likelihood of cracking or damage in later manufacturing processes. This enhancement significantly bolsters the overall strength and dependability of the final semiconductor products. Furthermore, by maintaining the structural integrity of the dies, this approach facilitates the manufacturing of superior devices, adhering to demanding industry standards and responding to the growing need for robust, dependable, and efficient semiconductor components.

iii. **Enhanced yield and cost efficiency:** The defect reduction through a double-sided wafer mounting technique during manufacturing, resulting in improved product quality and higher yields. Although the initial implementation costs for this complex technique may be higher, the long-term benefits significantly outweigh these expenses. This method generates substantial financial savings over time by reducing operator costs for visual inspection, improving production efficiency, and reducing defect rates. These advantages collectively optimise the total cost of ownership, rendering the technique a cost-effective solution for semiconductor manufacturers. Additionally, its capacity to improve product reliability is consistent with the industry's requirement for high-quality components, therefore strengthening the competitive advantage of organisations that implement it.

iv. **Optimization of vibration control:** The technique effectively mitigates and absorbs vibrations during the wafer dicing process, thereby resolving a critical challenge that has long affected semiconductor manufacturing. Defects, including chipping and splitting, are primarily caused by vibrations, which compromise the quality of the end product and the integrity of the die. This method not only mitigates these risks but also introduces a breakthrough approach to vibration management, which improves the precision and consistency of dicing operations. The technique establishes the foundation for future innovations by offering a durable solution to this persistent problem, thereby promoting further exploration and development in vibration control strategies to advance semiconductor manufacturing technologies.

v. **Improved manufacturing reliability:** By ensuring uniform support during critical manufacturing processes, the double-sided mounting approach significantly reduces the occurrence of defects such as chipping and fractures, thereby ensuring greater consistency in wafer performance. This improvement significantly enhances the reliability of semiconductor products, which is essential for the long-term functionality of consumer applications. Cracks in the die, if not adequately addressed, can propagate and lead to failure during operation, compromising product performance and customer trust. The double-sided mounting technique not only enhances product reliability but also enhances the competitiveness of semiconductor manufacturers in a market that demands high-quality, dependable components by mitigating these risks.

vi. **Theoretical and practical insights:** This research provides a comprehensive framework for investigating the complicated connection between the mechanical properties of silicon wafers, vibration control, and wafer mounting techniques. The study contributes to the academic literature on semiconductor technology by offering precise insights into the ways in which various mounting methods affect vibration absorption and stress distribution during critical manufacturing processes. Additionally, the results are a valuable resource for directing future industry practices, allowing manufacturers to enhance wafer handling and processing techniques. This framework facilitates the development of innovative solutions to enhance wafer reliability and overall product quality, in addition to advancing theoretical understanding.

5.3 Suggestions for Future Work

Here are several suggestions for future work on the implementation of a double-sided full sandwich wafer mounting technique to further enhance its effectiveness and applicability in semiconductor manufacturing. Firstly, the wafers provided by the industry for research activities were based on mirror silicon (Si) wafers and there was no circuitry available on the wafer. Therefore, it is best to monitor the chipping performance on complete circuitry production silicon wafers since basic chipping behaviours and mechanical responses, do not entirely replicate the circumstances present in production wafers with circuitry. The absence of circuitry significantly decreases the complexity of the wafer structure and disregards other elements that may affect chipping performance, like metallisation layers, interconnects, or other structural components essential to working devices.

The presence of polyimide on the sawing street greatly increases blade loading during the dicing operation, complicating efforts to attain precise and lower chipping performance. Polyimide and metals on the sawing street, frequently employed as protective layers and testing the wafer functionality during wafer processing, elevate the resistance faced by the dicing blade, resulting in increased friction and wear. The additional blade loading may lead to irregular cuts, heightened chipping, and diminished blade longevity, eventually affecting wafer quality and manufacturing efficiency. Resolving this issue necessitates the optimisation of dicing settings and methodologies to mitigate the impact of polyimide, hence enhancing performance, increasing yield, and improving the dependability of semiconductor components. If the double-sided full sandwich wafer mounting technology enhances material peeling and chipping performance, it will provide additional advantages to wafer dicing quality.

Then, Silicon carbide (SiC) wafers have attracted considerable interest in the semiconductor sector due to their enhanced material qualities, such as increased hardness, which makes them more brittle (R. Xue et al., 2021), thermal conductivity, and chemical stability relative to conventional silicon wafers. Nonetheless, their distinctive crystal structure and enhanced hardness make them considerably more brittle, presenting considerable hurdles throughout the wafer dicing procedure. The intrinsic brittleness of SiC wafers heightens the probability of chipping, cracking, and other mechanical imperfections, especially under the mechanical forces exerted by traditional dicing techniques. These difficulties make it necessary to evaluate the performance of the new full sandwich double-sided wafer mounting technique on SiC wafers. This technique offers improved wafer support and reduces vibrations, therefore addressing the particular challenges related to dicing fragile materials like as SiC. The full sandwich wafer mounting technique may reduce defect rates by providing better mechanical stability and stress distribution during the dicing process, therefore enhancing the yield and quality of SiC wafers.

The evaluation of the full-sandwich double-sided wafer mounting technique was conducted on a limited wafer sample, which may not fully represent high-volume production complexities. Future research should extend this analysis to industrial-scale production to better assess chipping performance and identify optimization opportunities. Increased blade loading can induce cracks (Ma et all. 2021), compromising device reliability. Additionally, longer cutting distances may cause adhesive buildup on the blade, leading to clogging and increased mechanical strain on the wafer. Understanding the relationship between cutting distance, adhesive properties, and blade performance is crucial for optimizing the full-sandwich mounting technique.

This study implemented UV mounting on 6 mm × 6 mm dies, demonstrating that optimized UV curing effectively aids surface tape removal during washing. The optimized parameters enabled efficient tape removal without damaging the dies or leaving adhesive residues, highlighting the viability of UV mounting for silicon wafer manufacturability. Future research should evaluate these UV curing settings across a broader range of die sizes to ensure optimal performance in semiconductor manufacturing processes.

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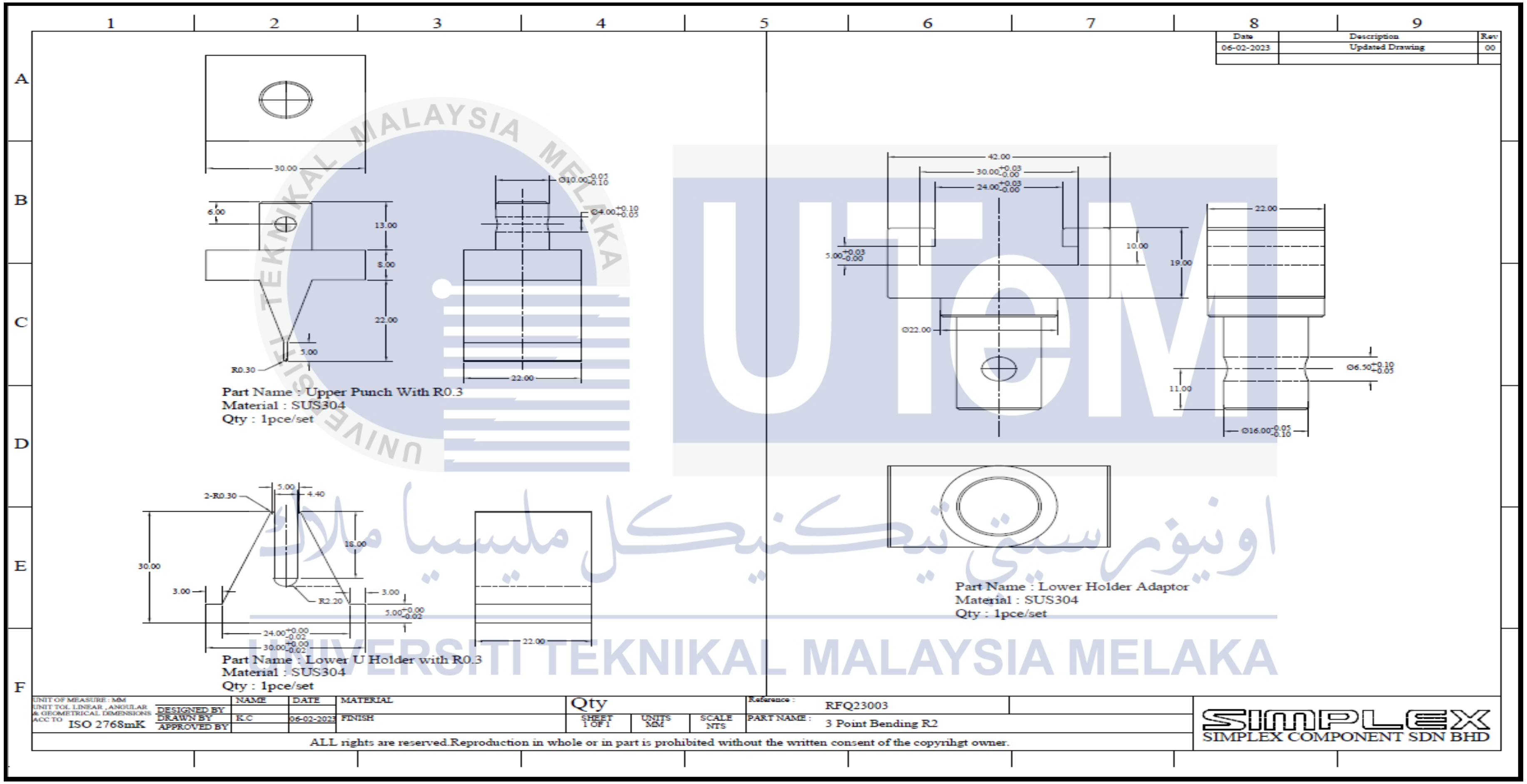
APPENDIX A

3-Point Bending Test Jig Drawing



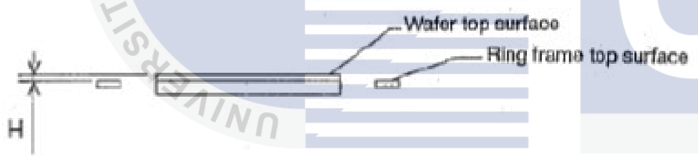
APPENDIX B

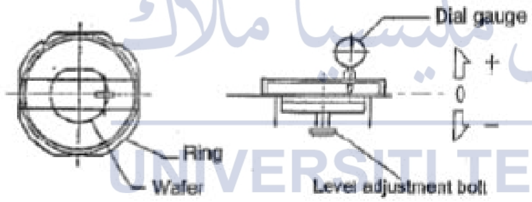
Wafer mounting calibration report

Mounter : calibration of mounting table height

3. Wafer Table Level Adjustment

1) Place a wafer and a ring frame on the wafer table and the ring frame table respectively, and allow the suction pad to suck them.
2) Place a table level adjustment jig on the ring frame. (Change the dial gauge position depending on the size of the wafer to be measured.)
3) Open the cover under the wafer table. Turn the level adjustment bolt to adjust the height.
Setting value H : 0.2 to 0.3 mm





Level jig for table height

Setup checklist :

Customer	LATM
Machine model	RAD2500M/12
Mfg. No.	D14S000171

Result : Pass

Date	Checked item						Inspected by
	Table flatness	Table height	Vacumm gauge	Air pressure	Attachment accuracy	Wafer pressure	
4-Jan -24	Ok	Ok	Ok	0.5MPa	Ok	0.05MPa	PF Chow
2-Feb-24	Ok	Ok	Ok	0.5MPa	Ok	0.05MPa	PF Chow
5-Mar-24	Ok	Ok	Ok	0.5MPa	Ok	0.05MPa	PF Chow
5-Apr -24	Ok	Ok	Ok	0.5MPa	Ok	0.05MPa	PF Chow
3-May-24	Ok	Ok	Ok	0.5MPa	Ok	0.05MPa	PF Chow
6-Jun-24	Ok	Ok	Ok	0.5MPa	Ok	0.05MPa	PF Chow
5-Jul-24	Ok	Ok	Ok	0.5MPa	Ok	0.05MPa	PF Chow
6-Aug-24	Ok	Ok	Ok	0.5MPa	Ok	0.05MPa	PF Chow
6-Sep-24	Ok	Ok	Ok	0.5MPa	Ok	0.05MPa	PF Chow
4-Oct-24	Ok	Ok	Ok	0.5MPa	Ok	0.05MPa	PF Chow

APPENDIX C

Wafer Dicing Calibration Report

DISCO HI-TEC (MALAYSIA) SDN. BHD.

Kuala Lumpur Office
L10-1&2, Volt Business Suites, Tower 5, Icon City
No. 1B, Jalan SS8/39 47300 Petaling Jaya, Selangor Malaysia.
TEL 60-3-7865-8062 FAX : 60-3-7865-8859

DISCO
www.disco.com.sg

Service Report #: DHS70568-0278

COST TYPE	CATEGORY
Chargeable Service	Relocation Setup

COMPANY INFORMATION

Customer Name:	Lintec Advanced Technologies (Malaysia) Sdn. Bhd.	Contact Name:	Chow Peng Fei
Address:	No. 35, Jalan Serendah 26/40, Kawasan Perindustrian Hicom Seksyen 26, I-Parc 2, 40400 Shah Alam,	Phone Number:	
City , State , ZIP:	40400	Email:	chowpf@lintec.com.sg
P.O.Number:	M24VPO-00079	Balance BPO:	

MACHINE INFORMATION

MODEL	SERIAL NUMBER	SHIPPED DATE	CURRENT SOFTWARE	DPR #
DFD6362	NL1681	24/07/2018		

DETAILS

PURPOSE OF VISIT

Machine Re-Location and Setup.

ACTIONS AND RESULTS

- Hook up all the utilities such as Power, Chiller Water, DI water, Air, Exhaust.
- Above Dicer saw (Dfd6362) connected with DWR-1721 (NR2044) .
- Replaced New Touch Panel (Topre brand) on DFD6362.
- Drain off all the water tank on DWR-1721 and Re-setup again.
- Prrformed m/c Health check as following .

1. X & Y axis Perpendicurity: 0.002/150mm.
2. X & Spd 1 Perpendicurity: 0.005/150mm.
3. X & Spd 2 Perpendicurity: 0.002/150mm
4. Spd 1 & Spd 2 thrust and radius : < 0.002mm
5. Spd Revolution check :
- Z1 : 29,920 rpm
- Z2 : 29,990 rpm
6. Wheel mount conditioning on Z1 & Z2 done.
7. Chuck Table Flatness :
- CH1 : 0.005/200mm.
- CH2 : 0.002/200mm.

Test cut mylar tape, Result : Ok

RECOMMENDATIONS

REMARKS

APPENDIX D

UV Curing Calibration Report

CALIBRATION REPORT

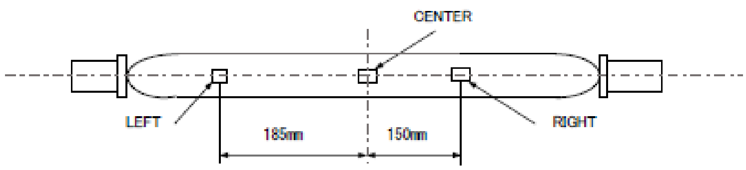
RAD-2010M/12 UV LIGHT INTENSITY & EXPOSURE DOSE

Customer	LATM
Mfg. No.	D145000971
UV Power Unit Mfg. No.	UA11307
Lamp Unit Mfg. No.	# 48243
Mirror Type	AL Mirror
Lamp	HHL2800/B-FL-N

Date : 4/1/2024

Inspected by : Fu Hee Tom

Approved by : Chow Peng Fei



Measurement Condition

	Measured Value
Lamp Voltage [V]	430
Lamp Power [W]	2125
Set Irridiation	3.8
Lamp Unit Temperature [°C]	40
Lamp Life [H]	495

	Coefficient	Display
Voltage Multiplying Factor	1	430
Voltage Offset Value	0	
Power Multiplying Factor	1	2125
Power Offset Value	0	
Intensity Multiplying Factor	0.125	
Intensity Offset Value	0	
Exposure Dose Multiplying Factor	0.074	
Exposure Dose Offset Value	0	

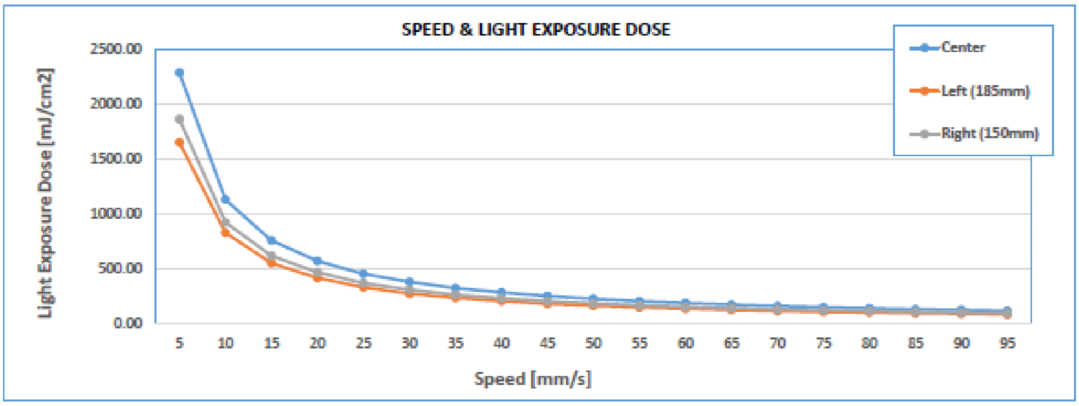
Measurement Tool	UV-M10-S/ORC
Calibration Tool No.	100
Filter	49

Light Intensity Measurement [mW/cm2]

	Left (185mm)	Center	Right (150mm)
Light Intensity	238.14	337.12	269.99

Exposure Dose Measurement [mJ/cm2]

Speed	Left (185mm)	Center	Right (150mm)	Display
5 mm/s	1656.2	2292.71	1867.39	1646
10 mm/s	832.51	1133.86	928.06	821
15 mm/s	556.15	760.97	621.32	540
20 mm/s	419.93	574.77	470.89	401
25 mm/s	334.18	457.66	372.89	326
30 mm/s	276.85	383.18	313.60	267
35 mm/s	238.63	326.34	266.56	225
40 mm/s	209.23	287.63	234.71	203
45 mm/s	184.24	254.31	207.27	177
50 mm/s	167.58	229.81	188.16	157
55 mm/s	150.92	208.25	170.03	144
60 mm/s	141.12	192.08	156.80	135
65 mm/s	127.89	175.91	144.06	121
70 mm/s	120.05	164.64	134.75	114
75 mm/s	110.74	152.88	125.44	103
80 mm/s	105.35	144.06	118.09	97
85 mm/s	98.00	134.75	110.74	89
90 mm/s	93.59	128.87	104.86	87
95 mm/s	87.71	120.54	98.49	79



Result : OK

APPENDIX E

Universal Testing Machine Calibration Report

KL Analytical Sdn Bhd (677718 K) (200501000673)

UNCONTROLLED COPY
FOR REFERENCE ONLY
APPROVED BY ....

K-3-7, No. 2, Jalan Solaris
Solaris Mont' Kiara
50480 Kuala Lumpur, Malaysia
Tel : +603-6203 6083
Fax : +603-6203 6483
Email : info@klanalytical.com
Website :www.klanalytical.com

Certificate of Calibration

Number of page(s) 1/2

Certificate No.	KLA/220826/AD01			
Equipment	Universal Testing Machine			
Manufacturer	Shimadzu			
Model	EZ-LSONX	Serial No.	:	I 30835535058CS
Capacity	5kgf	Control No.	:	0
Requested By	UNIVERSITI TEKNIKAL MALAYSIA MELAKA FAKULTI KEJURUTERAAN PEMBUATAN, HANG TUAH JAYA, 76100 DURIAN TUNGGAL, MELAKA.			
Calibration range	0.05 - 5.00kgf			
Resolution	0.0005	Indicator	:	Digital
Calibration mode	True Force			
Date of Calibration	26 August, 2022	Issue date	:	8 September, 2022
Calibration Due Date	25 August, 2023	(As request by customer)		
Calibration location	On Site			
Condition of the item	In Good Condition			
Environments	Temperature	25.0 ± 1.0 °C		
	Relative Humidity	52.5 ± 1.5 %		
Calibration Method Reference	ISO 7500-1 2018(E)			

Reference Instrument	Serial No.	Certificate No.	Due Date
Dead Weight (2kg - 10kg)	N/A	PSYP-21080028	4 December, 2022
Standard Weight (1g -2kg)	N/A	PSYP-22028615	25 April, 2023

Traceability: This certificate is traceable to the International System of Unit which is maintained by the National Institute of Metrology

Calibrated by
....
Mohd Fazliady Mat Nor
Calibration Officer

KL ANALYTICAL SDN BHD CO. NO. 200501000673 (677718 K)

Approved by
....
Lee Keng Yih

KL Analytical Sdn Bhd (677718 K) (200501000673)

K-3-7, No. 2, Jalan Solaris
Solaris Mont' Kiara
50480 Kuala Lumpur, Malaysia
Tel : +603-6203 6083
Fax : +603-6203 6483
Email : info@klanalytical.com
Website :www.klanalytical.com

Certificate of Calibration

Certificate No. KLA/220826/AD01

Table 1 : Calibration results Tensile

Reference Force (kgf)	UUT Value (kgf)	Error (%)	Relative Expanded Uncertainty (%)	k	Class of Machine
0	0	0	0.00	0	0
0.0500	0.05002	0.05	0.25	2	0.5
0.1500	0.14989	-0.08	0.25	2	0.5
0.2500	0.2499	-0.05	0.28	2	0.5
0.400	0.3996	-0.09	0.30	2	0.5
0.500	0.4995	-0.11	0.29	2	0.5
1.00	0.9992	-0.08	0.30	2	0.5
2.00	1.9970	-0.15	0.34	2	0.5
3.00	2.9953	-0.16	0.30	2	0.5
4.00	3.9915	-0.21	0.34	2	0.5
5.00	4.9910	-0.18	0.31	2	0.5

Table 2 : The Characteristic values of the force measuring system

Reference force	(%) Relative error of				Relative Resolution
	Accuracy (q)	Repeatability (b)	Reversibility (v)	Zero (f_0)	
-	-	-	-	-	-
0.05	0.0467	0.1000	0.0067		0.0400
0.15	-0.0756	0.1467	-0.0890		0.0133
0.25	-0.0533	0.2400	-0.0934		0.0400
0.40	-0.0917	0.3000	-0.1168		0.0250
0.50	-0.1067	0.2600	-0.1668	0.0000	0.0200
1.00	-0.0833	0.3000	-0.1334		0.0500
2.00	-0.1500	0.4250	-0.1753		0.0250
3.00	-0.1556	0.2833	-0.2059		0.0167
4.00	-0.2125	0.3750	-0.2756		0.0125
5.00	-0.1800	0.3000	-0.1903		0.0100

* UUT - Unit Under Test

* The uncertainties are for a confidence probability of approximetely 95% and have a coverage factor k =2 unless stated otherwise

APPENDIX F

Tensilon RTG 1210 Calibration by equipment supplier