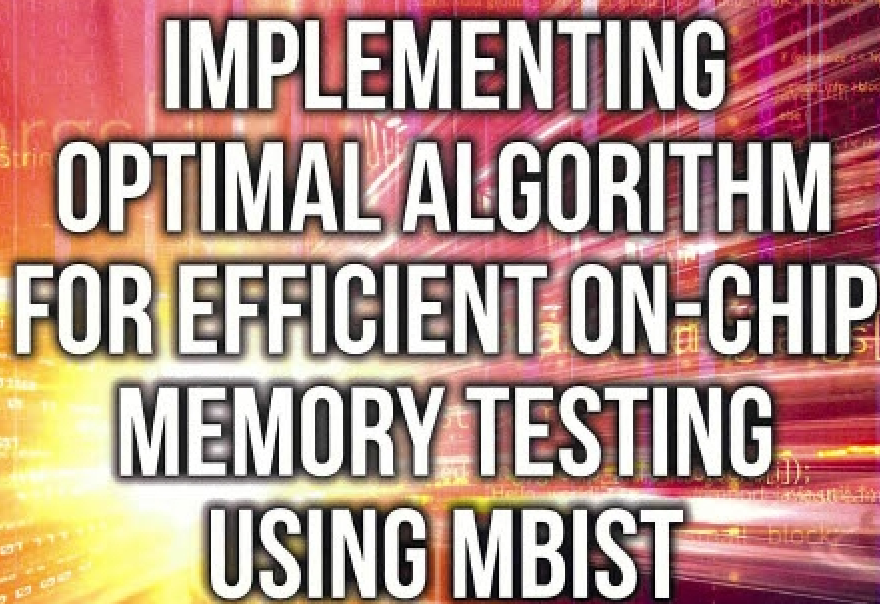
IMPLEMENTING OPTIMAL ALGORITHM FOR EFFICIENT ON-CHIP MEMORY TESTING USING MBIST



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IMPLEMENTING OPTIMAL ALGORITHM FOR EFFICIENT ON-CHIP MEMORY TESTING USING MBIST

This book discusses the implementation of Memory Built-In Self-Test (BIST) for memory testing, including the memory fault models's descriptions, the method to implement a Memory BIST circuitry, and the elaboration on its test algorithm. Memory testing efficiency depends on the test coverage and duration. Hence, selecting an appropriate test algorithm is crucial to achieving an optimal balance between the test quality and cost. This book comprehensively explains the problems and challenges in memory testing and offers several solutions. It helps readers understand the Memory BIST functionality and choose the right test algorithm and implementation technique to optimize fault detections.

AIMAN ZAKWAN JIDIN completed his PhD in Electronic Engineering at Universiti Malaysia Perlis, Malaysia in 2024. His research focuses on creating a new low-complexity memory testing algorithm for optimum static fault coverage in SRAM. Previously, he gained expertise as an FPGA IP Core Design Engineer at Altera Corporation Malaysia. He is currently a senior lecturer and researcher at Universiti Teknikal Malaysia Melaka (UTeM). His research interests include DFT, VLSI and FPGA system design.

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