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Optimization of Process Parameter Variability in 45 nm PMOS Device using Taguchi Method

[1]F. Salehuddin, [1]I. Ahmad, [1]F.A. Hamid and [2]A. Zaharim
[1]College of Engineering, Universiti Tenaga Nasional, Km 7, Jalan Kajang-Puchong,
43009 Kajang, Selangor, Malaysia
[2]Faculty of Engineering and Built Environment, Universiti Kebangsaan Malaysia,
43600 Bangi, Selangor, Malaysia

Abstract: This study reports on an investigation of the effect and optimization of process parameter variability on poly sheet resistance (R_S) and leakage current (I_{Leak}) in 45 nm PMOS device. The experimental studies were conducted under varying four process parameters, namely Halo implantation, Source/Drain Implantation, Oxide Growth Temperature and Silicide Anneal Temperature. Taguchi Method was used to determine the settings of process parameters. The level of importance of the process parameters on the poly sheet resistance and leakage current were determined by using Analysis of Variance (ANOVA). Virtual fabrication of the devices was performed by using ATHENA module. While the electrical characterization of the devices was implemented by using ATLAS module. The optimum process parameter combination was obtained by using the analysis of Signal-to-Noise (S/N) ratio. The confirmation tests indicated that it is possible to decrease the poly sheet resistance and leakage current significantly by using the Taguchi method. The results show that the R_S and I_{Leak} after optimizations approaches are 67.53 Ω sq^{-1} and 0.1850 mA μm^{-1}, respectively. In this study, S/D implantation was identified as one of the process parameters that has the strongest effect on the response characteristics.

Key words: Optimization, variability, 45 nm pmos device, taguchi method, silvaco

INTRODUCTION

Parameter variability in an integrated circuit manufacturing process is becoming increasingly important when it comes to being deep submicron devices due to feature scaling. Besides, the impact on device performance due to these variations is also increasing and affecting the yield. The process parameter fluctuations in general can be organized as global variations and local variations. Local variations between identically laid-out devices arise from random microscopic process variations. The random distributions arise from the variation of process parameters, for example, impurity concentration densities, oxide thickness and diffusion depths, which result from varying operating or environmental conditions during the deposition or diffusion of the impurity dopant. The fluctuations in the process parameters may result in the variation of sheet resistance and threshold voltage. The variations will impact the performance of a device, which may exhibit wider variability leading to the degradation of yield in modern technologies and applications. Furthermore, for several decades the output from semiconductor manufacturers has been high volume products with process optimization being continued throughout the lifetime of the product to ensure a satisfactory yield (Ramakrishnan, 2009). The technique described in this report to identify semiconductor process parameters whose variability would impact most on the device characteristics is realized through a process using Taguchi Method. This is because the Taguchi method is a systematic application of design and analysis of experiments for designing and improving product quality at the design stage (Montgomery, 2005).

In recent years, the Taguchi method has become a powerful tool for improve product during research and development. So, the high quality of products can be produced quickly and at low cost (Arghavani *et al*., 2007). Optimization of process parameters is the key step in the Taguchi method to achieving high quality without increasing cost. This is because optimization of process parameters can improve the quality of product. The optimum values of process parameters that obtained from the Taguchi method are insensitive to the variation of environmental conditions and other noise factors.

Basically, classical process parameter design is complex and not easy to use (Esme, 2009). A large number of experiments have to be carried out when the number of the process parameters' increases. To solve this task, the

Corresponding Author: F. Salehuddin, College of Engineering, Universiti Tenaga Nasional, Km 7, Jalan Kajang-Puchong, 43009 Kajang, Selangor, Malaysia

Taguchi method uses a special design of orthogonal arrays to study the entire process parameter space with only a small number of experiments. Using an orthogonal array to design the experiment could help the designers to study the influence of multiple controllable factors on the average of quality characteristics and the variations in a fast and economic way, while using a signal-to-noise ratio to analyze the experimental data could help the designers of the product or the manufacturer to find out the optimal parametric combinations.

MATERIALS AND METHODS

Sample used in these experiments were <100> oriented and p-type (boron doped) silicon wafers. N-wells are created starting with developing a 200 Å oxide screen on the wafers followed by phosphorus doping. The oxide layer was etched after the doping process was completed. It was followed by annealing process to strengthen the structure. Next, STI was developed to isolate neighboring transistor. A 130 Å stress buffer was developed on the wafer with 25 min diffusion processes. Then, a 1500 Å nitride layer was deposited using the Low Pressure Chemical Vapor Deposition (LPCVD) process. This thin nitride layer was acted as the mask when silicon was etched to expose the STI area. Photo resistor layer was then deposited on the wafers and unnecessary part will be removed using the Reactive Ion Etching (RIE) process. An oxide layer was developed on the trench sides to eliminate any items from entering the silicon substrate. Chemical Mechanical Polishing (CMP) was then applied to eliminate extra oxide on the wafers.

Lastly, STI was annealed for 15 min at 900°C temperature. A sacrificial oxide layer was then developed and etched to eliminate defects on the surface (Elgomati, 2007). The gate oxide was grown and a Boron Difluoride (BF_2) threshold-adjustment implants were done in the channel region through this oxide. The polysilicon gate was then deposited and defined followed by the halo implantation. In order to get an optimum performance for PMOS device, arsenic was doped at a 3.37×10^{13} atom cm^{-3}. Sidewall spacers were developed after that process. Sidewall spacers were then used as a mask for source/drain implantation. Boron atoms were implanted at a desired concentration to ensure the smooth current flow in PMOS device (Hamida, 2007). Silicide layer was then annealed on the top of polysilicon.

The next step in this process was the development of Boron Phosphor Silicate Glass (BPSG) layer. This layer will be acted as Premetal Dielectric (PMD), which is the first layer deposited on the wafer surface when a transistor was produced. This transistor was then connected with aluminum metal. After this process, the second aluminum layer was deposited on the top of the Intel Metal Dielectric (IMD) and unwanted aluminum was etched to develop the contacts (Hamida, 2007). The final step in the development of the PMOS transistor device is to define the electrodes. After the electrodes are defined this device can act as a true device in circuit simulation. Once the devices were built with ATHENA, the complete devices can be simulated in ATLAS to provide specific characteristics such as the I_D versus V_{GS} curve. The threshold voltage (V_{TH}) can be extracted from that curve (Goel *et al*., 1995).

Table 1: Process parameters and their levels

Symbol	Process parameter	Unit	Level 1	Level 2	Level3
A	Halo implantation	atom cm^{-3}	3.37E13	3.38E13	339E13
B	S/D implantation	atom cm^{-3}	6.55E13	6.60E13	665E13
C	Oxide growth temperature	°C	815	820	825
D	Silicide anneal temperature	°C	900	910	950

Table 2: Experimental layout using $L_9(3^4)$ orthogonal array

	Process parameter level			
Exp. No.	A Halo implantation	B S/D implantation	C Oxide growth temprature	D Silicide anneal temprature
1	1	1	1	1
2	1	2	2	2
3	1	3	3	3
4	2	1	2	3
5	2	2	3	1
6	2	3	1	2
7	3	1	3	2
8	3	2	1	3
9	3	3	2	1

Taguchi orthogonal L9 array method: The paper optimizations of the PMOS device has been done by changing individual process parameters (factors) lay out by the ATHENA (Goel *et al*., 1995). The factors that were modified and examined include: the halo implantation, the S/D implantation, the oxide growth temperature and the silicide anneal temperature. The value of the process parameter at the different levels is listed in Table 1.

In this study, an $L_9(3^4)$ orthogonal array which has 9 experiments was used. The experimental layout for the process parameters using the $L_9(3^4)$ orthogonal array is shown in Table 2.

RESULTS AND DISCUSSION

The fabrication result of the first set experiment that has been done by using ATHENA module was discussed. The result obtained shows from fabrication process and electrical characteristics PMOS device. Beside that, this

Table 3: R_S values for PMOS device

	Poly sheet resistance Ω sq^{-1}			
Exp. No.	R_S 1	R_S 2	R_S 3	R_S 4
1	67.2935	66.9507	66.9594	66.9511
2	67.4951	67.5055	67.9441	66.9991
3	69.2623	67.7981	67.8228	67.7374
4	67.6923	67.7469	66.8321	67.3056
5	67.6283	67.6439	67.6300	67.6308
6	67.9754	67.9877	67.4916	68.0461
7	67.9456	67.4673	67.9453	67.8958
8	67.3109	67.7372	67.3000	67.3080
9	67.6645	67.6738	67.6256	67.6682

Table 4: I_{Leak} values for PMOS device

	Leakage current m A μm^{-1}			
Exp. No.	I_{Leak} 1	I_{Leak} 2	I_{Leak} 3	I_{Leak} 4
1	0.190395	0.194152	0.193816	0.193141
2	0.194186	0.192999	0.195172	0.192365
3	0.197700	0.188718	0.198404	0.200747
4	0.186751	0.185634	0.187389	0.175141
5	0.190183	0.181047	0.190658	0.190871
6	0.198321	0.199210	0.198642	0.186239
7	0.182663	0.173512	0.183115	0.185449
8	0.190538	0.191665	0.190949	0.190721
9	0.195878	0.194698	0.196771	0.193942

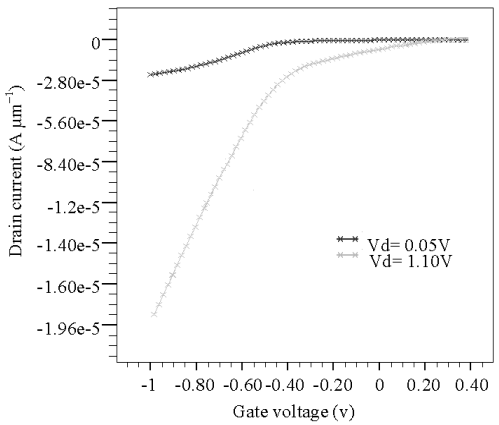

Fig. 1: Graph I_D-V_G for 45 nm PMOS Device

section also shows the optimization result of PMOS device by using Taguchi Method Approach.

45 nm transistor fabrication: Figure 1 shows the graph of I_D versus V_G at V_D = 0.05V and V_D = 1.1 V for both devices. The threshold voltage value is –0.14724 V. This value is still in range ±12.7% from the nominal value. The nominal value of threshold voltage for PMOS device is -0.15 V (http://www.itrs.net). At V_{TH} = -0.14724 V, the values of poly sheet resistance and leakage current are 67.29 and 0.190 mA μm^{-1}, respectively.

The results of R_S and I_{Leak} were analyzed and processed with Taguchi Method to get the optimal design. Then, the optimum values of the process parameter from Taguchi Method were then simulated in order to verify the predicted design.

Table 5: S/N ratios for PMOS device

	S/N ratios (dB)	
Experiment No.	Poly sheet resistance	Leakage current
1	-36.53	74.29
2	-36.58	74.26
3	-36.67	74.14
4	-36.57	74.71
5	-36.60	74.51
6	-36.63	74.17
7	-36.63	74.83
8	-36.58	74.38
9	-36.61	74.18

Analysis of effect process parameters to poly sheet resistance and leakage current: The experimental results of poly sheet resistance and leakage current for PMOS device using the L_9 orthogonal array are shown in Table 3 and 4.

After nine experiments of L_9 array have been done, the next step is to determine the required values for selected factors, which are halo implantation, S/D implantation, oxide growth temperature and silicide anneal temperature that gave the effect to a device. Poly sheet resistance and leakage current of the 45 nm devices belongs to the smaller-the-best quality characteristics.

The S/N Ratio, η of the smaller-the-best quality characteristics can be expressed as (Montgomery, 2005; Esme, 2009):

$$\eta = 10\text{Log}_{10}\left[\frac{1}{n}\sum\left(Y_1^2 + Y_2^2 + ... + Y_n^2\right)\right] \quad (1)$$

where, n is the number of tests and Y_i the experimental value of the poly sheet resistance and leakage current. By applying Eq. 1, the η for each device were calculated and given in Table 5. The effect of each process parameter on the S/N Ratio at different levels can be separated out because the experimental design is orthogonal. The S/N ratio for each level of the process parameters is summarized in Table 6. In addition, the total mean of the S/N ratio for the 9 experiments is also calculated and listed in Table 6.

Figure 2 and 3 show the S/N ratio graphs where the dashed line is the value of the total mean of the S/N ratio. Basically, the larger the S/N ratio, the quality characteristic of the poly sheet resistance and leakage current are better (Esme, 2009).

A better feel for the relative effect of the different process parameter on the poly sheet resistance (R_S) and leakage current (I_{Leak}) were obtained by decomposition of variance, which is called Analysis of Variance (ANOVA) (Abdullah *et al*., 2009). The relative importance of the

Table 6: S/N response for the threshold voltage in PMOS device

			S/N ratio (Smaller-the best)				
Parameter	Symbol	Process parameter	Level 1	Level 2	Level 3	Total mean S/N	Max-Min
R_S	A	Halo implant.	-36.59	-36.60	-36.60	-36.60	0.01
	B	S/D implant.	-36.58	-36.59	-36.64		0.06
	C	Oxide growth temp.	-36.58	-36.59	-36.63		0.05
	D	Silicide anneal temp.	-36.58	-36.62	-36.61		0.04
I_{leak}	A	Halo implant.	74.23	74.46	74.47	74.39	0.24
	B	S/D implant.	74.61	74.38	74.16		0.45
	C	Oxide growth temp.	74.28	74.39	74.49		0.21
	D	Silicide anneal temp.	74.33	74.42	74.41		0.09

Table 7: Results of ANOVA for R_S in PMOS device

Symbol	Process parameter	Degree of freedom	Sum of square	Mean square	F-value	Contribution (%)
A	Halo implant.	2	0	0	1	1
B	S/D implant.	2	0	0	23	46[a]
C	Oxide growth temp.	2	0	0	19	37[a]
D	Silicide anneal temp.	2	0	0	8	15

[a]At least 95% confidence

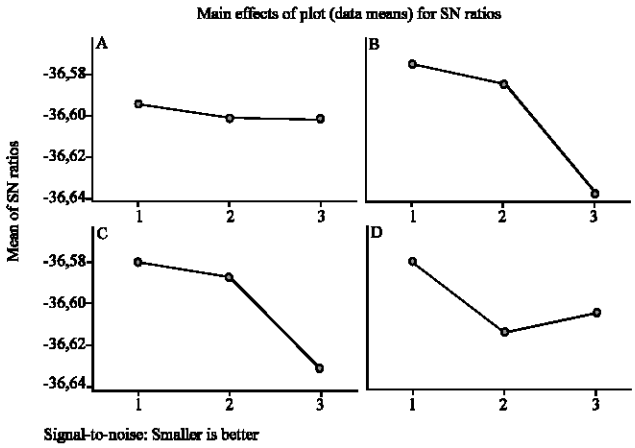

Fig. 2: S/N graph for poly sheet resistance in PMOS device

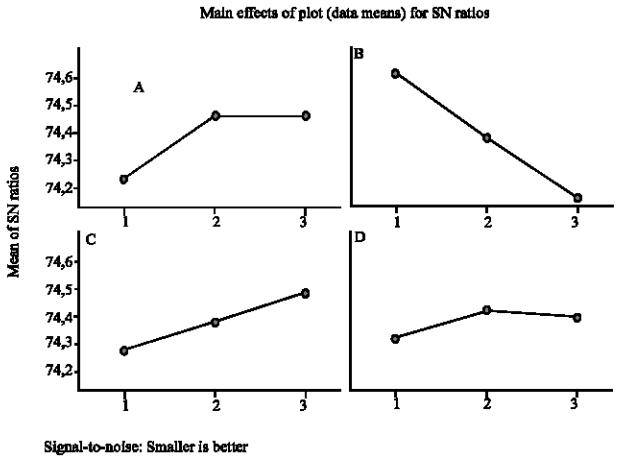

Fig. 3: S/N graph for leakage current in PMOS Device Analysis of Variance (ANOVA)

Table 8: Results of ANOVA for I_{Leak} in PMOS device

Symbol	Process parameter	Degree of freedom	Sum of square	Mean square	F-value	Contribution (%)
A	Halo implant.	2	0	0	11	22[a]
B	S/D implant.	2	0	0	31	61[a]
C	Oxide growth temp.	2	0	0	7	13
D	Silicide anneal temp.	2	0	0	2	3

[a]At least 95% confidence

Table 9: Results of the Confirmation Experiment

Process parameter settings	R_S Ω sq^{-1}		I_{Leak} mA μm^{-1}	
	Predicted	Observed	Predicted	Observed
$A_2B_3C_1D_2$ (Nominal)	67.842	67.975	0.1960	0.1983
$A_3B_1C_1D_1$ (Optimum)	67.220	67.533	0.1875	0.1850
Improvement (%)	0.92	0.65	4.34	6.70

process parameters with respect to the V_{TH} was investigated to determine more accurately the optimum combinations of the process parameters by using ANOVA. The results of ANOVA for the R_S and I_{Leak} in PMOS device are presented in Table 7 and 8, respectively. Statistically, F-test provides a decision at some confidence level as to whether these estimates are significantly different. Larger F-value indicates that the variation of the process parameter makes a big change on the performance. According to Table 7, the most effective process parameters with respect to poly sheet resistance are S/D implantation, oxide growth temperature, silicide anneal temperature and halo implantation. Percent factor effect indicates the relative power of a factor to reduce variation. For a factor with a high percent contribution, a small variance will have a great influence on the performance. Referring to Table 8, the most effective process parameters with respect to leakage current are S/D implantation, halo implantation, oxide growth temperature and silicide anneal temperature.

The percent factor effect on S/N ratio of the process parameters on the poly sheet resistance and leakage current are shown in Table 7 and 8, respectively. According to Table 7 and 8, S/D implantation was found to be the major factor affecting the poly sheet resistance (46%) and leakage current (61%).

Confirmation test : The confirmation experiment is the final step in the first interaction of the design of the experiment process. The purpose of the confirmation experiment is to validate the conclusions drawn during the analysis phase (Abdullah *et al*., 2009). Conducting a test with a specific combination of the factors and levels previously evaluated performs the confirmation experiment. After determining the optimum conditions and predicting the response under these conditions, a new experiment was designed and conducted with the optimum levels of the process parameters. The results of experimental confirmation using optimal process parameters and comparison of the predicted poly sheet resistance and leakage current with the actual poly sheet resistance and leakage current using the optimal process parameters are shown in Table 9. The improvement in percentage from the starting process parameters to the level of optimal process parameters is 0.65 and 6.70% for poly sheet resistance and leakage current , respectively. Therefore, the poly sheet resistance and leakage current are greatly improved by using the Taguchi method.

CONCLUSION

Taguchi method design is used to develop a systematic design of experiments. This design method gave 9 set experiments. It has many variants that can be applied to the modeling device and a lot of parameters can be used. Taguchi method already applied to get a robust design. It is proven on time saving and the result is good according to objective and desired of the project. It easily to do 9 experiments in comparison to 81 experiments that might develop from 4 process parameters for 3 levels. Then, the analysis of variance shows the process parameter of S/D implantation and oxide growth temperature are significant based on 95% confidence level towards poly sheet resistance and leakage current respond. So that the poly sheet resistance and leakage current decreased follows the S/D implantation doping and oxide growth temperature. Analysis of variance also proved the factors of S/D implantation and halo implantation is significant towards leakage current respond.

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